



SANYO Semiconductors DATA SHEET

LV24020LP — Bi-CMOS IC Ultra-compact FM tuner IC for mobile set

Overview

The LV24020LP is FM tuner IC's that requires absolutely no external components.

They incorporates not only the FM tuner functions as well in a compact VQLP package with dimensions of only 5mm×5mm×0.8mm.

These IC's are simply ideal for incorporating FM tuner functions into mobile phones and other small mobile set where space is always at a premium.

Functions

- FM FE
- FM IF
- MPX Stereo Decoder
- Tuning

Features

- No external components
- No alignments necessary
- Fully integrated low IF selectivity and demodulation
- Built in adjacent channel interference total reduction (no 114kHz, no 190kHz)
- Due to new tuning concept, the tuning is independent of the channel spacing
- Very high sensitivity due to integrated low noise RF input amplifier
- Very low power Standby mode. No power switch circuitry required
- MPX output for RDS application
- 3-wire bus interface (Data, Clock, NR-W)
- Digital AFC - Tuner locks to frequency after tuning sequence
- 8 level programmable Soft Mute
- 8 level programmable Stereo Blend
- In combination with the host, fast, low power operation of preset mode, manual search, automatic search and automatic preset store are possible
- Covers all Japanese, European and US bands

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LV24020LP

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	Analog block supply voltage	6.0	V
	V _{DD} max	Digital block supply voltage	5.0	V
Digital input voltage	V _{IN1} max	Clock, Data, NR_W	V _{DD} +0.3	V
	V _{IN2} max	External_clk_in	V _{DD} +0.3	V
Allowable power dissipation	P _d max	Ta ≤ 70°C	140	mW
Operating temperature	T _{opr}		-20 to +70	°C
Storage temperature	T _{stg}		-40 to +125	°C

Operating Condition at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}	Analog block supply voltage	3.0	V
	V _{DD}	Digital block supply voltage	3.0	V
Operating supply voltage range	V _{CC} op		2.7 to 5.0	V
	V _{DD} op		2.5 to 4.0	V
	V _{IO} op	Interface supply voltage	1.8 to 4.0	V

Note: Power supply voltage V_{IO} equal V_{DD}, or V_{IO} < V_{DD} (V_{IO} ≤ V_{DD})

Interface Conditions at Ta = -20 to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V _{DD}		2.5		4.0	V
Digital part input	V _{IH}	High level input voltage range	0.7V _{DD}		V _{DD}	V
	V _{IL}	Low level input voltage range	0		0.6	V
Digital part output	I _{OL}	Low level output current	2.0			mA
	V _{OL}	Low level output voltage I _{OL} =2mA			0.6	V
Clock input frequency	f _{clk}	3wire_bus (29pin) clock frequency			0.7	MHz
External clock frequency	f _{clk_ext}	CLK_IN (31pin) frequency	32k		14M	Hz

Note: CLK_IN (31pin) can input sign wave.

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Operating Characteristics at Ta = 25°C, VCC=3.0V, VDD=3.0V, VOL=14, Soft Mute/Stereo=off

VOL=14 –Block2 register09h Volume_Bit 3-0 = 0010

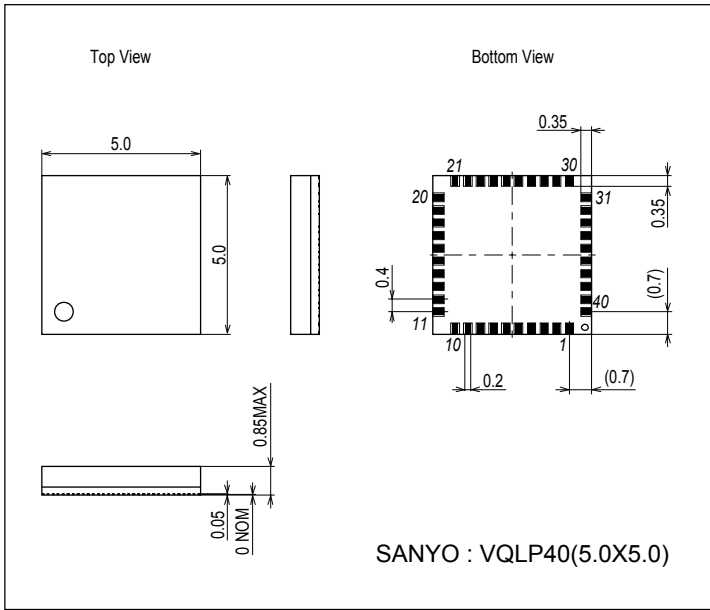
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operational supply current	ICCA	Analog Block at 60dBμ input The 23pin is measured		14	17	mA
	ICCD	Digital Block at 60dBμ input The 27, 40 pins are measured.	0.2	0.4	0.8	mA
Standby supply current	ICCA	Analog standby mode The 23 pin is measured.		3	30	μA
	ICCD	Digital standby mode The 27, 40 pins are measured.		3	30	μA
FM coverd frq	F_range		76		108	MHz
[FM receiving characteristics ; MONO]: fc=80MHz, fm=1kHz, 22.5kHzdev. soft_stereo, soft_mute, Buss, Treble are all OFF.						
Input limiting voltage	-3dB LS	V _{IN} =60dBμ standard for a -3dB input		13	19	dBμV EMF
Practical sensitivity	QS1	for 30dB signal to noise ratio input De-emphasis is 75μs SG open		10	16	dBμV EMF
Practical sensitivity	QS2	for 26dB signal to noise ratio input De-emphasis is 75μs SG close		1.25		μV
Demodulator output level	V _O	V _{IN} =60dBμ, 11pin output level	60	100	140	mV
Channel balance	CB	V _{IN} =60dBμ, ratio of 11pin to 12pin output level	-2	0	2	dB
Signal to noise ratio	S/N	V _{IN} =60dBμ, 11pin output level	48	58		dB
Total harmonic distortion 1 (MONO)	THD1	V _{IN} =60dBμ, 22.5kHzdev, 11pin output		0.4	1.5	%
Total harmonic distortion 2 (MONO)	THD2	V _{IN} =60dBμ, 75kHzdev, 11pin output		1.3	3	%
Field strength level	FS	Input level for FS1 to FS2	8	18	27	dBμ
Muting attenuation	Mute-Att	V _{IN} =60dBμ, 11pin output level	60	70		dB
[FM receiving characteristics ; STEREO]: fc=80MHz, fm=1kHz, V _{IN} =60dBμV, L+R=30% (22.5kHzdev), Pilot=10% (7.5kHzdev)						
Separation	SEP	L-mod, 11pin→12pin output level	20	35		dB
Total harmonic distortion (STEREO)	THD-ST	Main-mod (L+R), 11pin/12pin output, IHF_BPF		0.6	1.8	%

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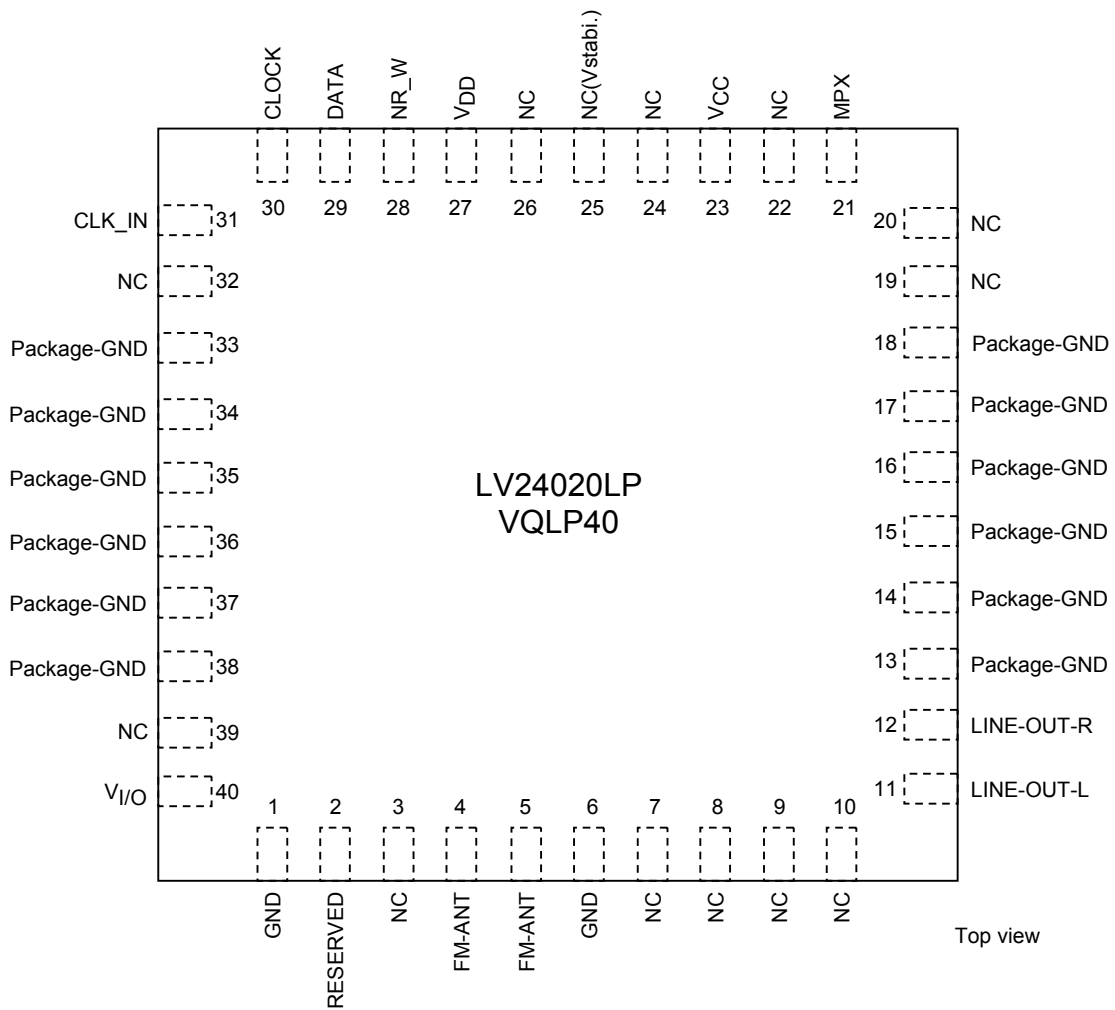
Package Dimensions

unit : mm (typ)

3302A



Pin Assignment



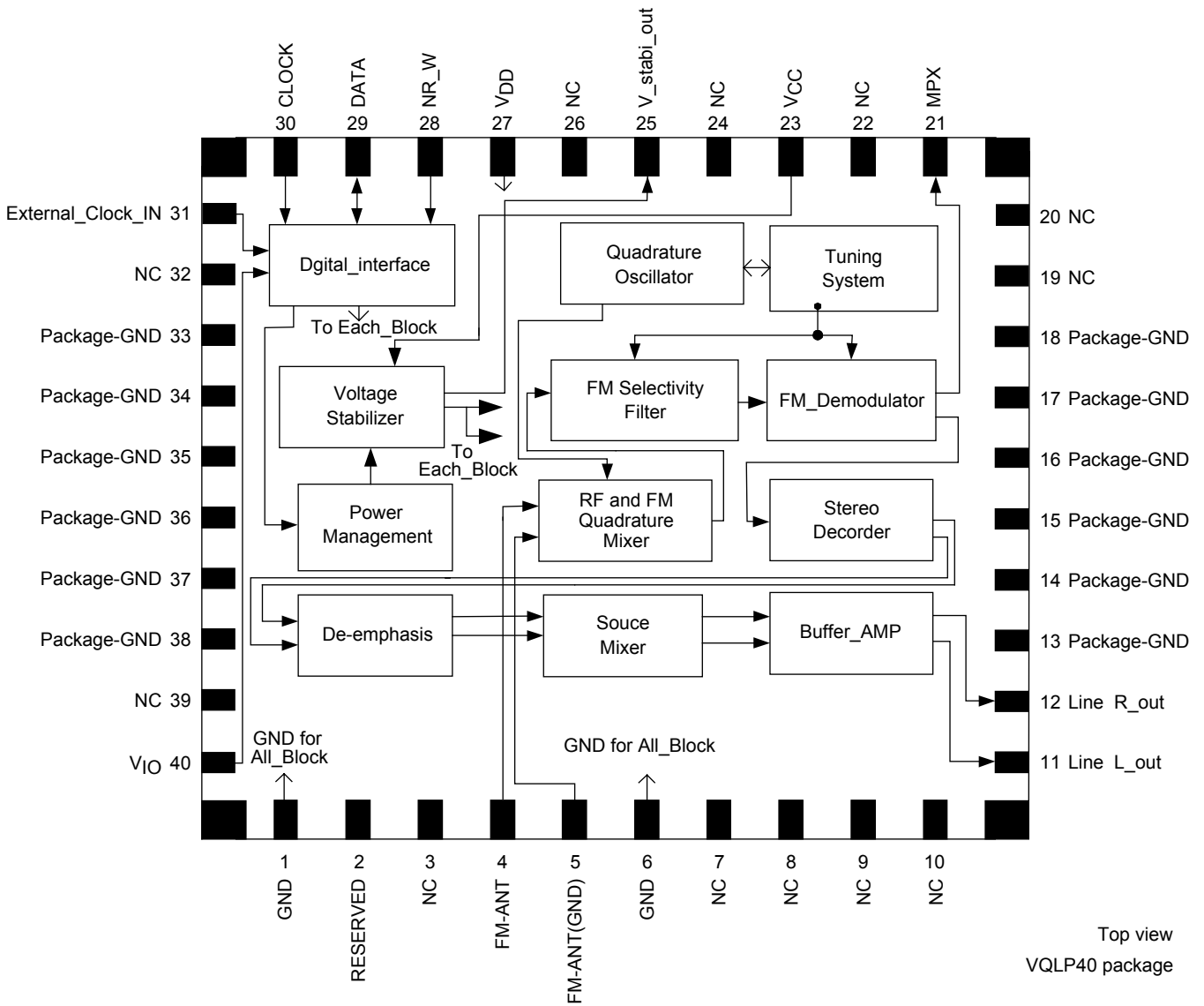
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VQLP40 package Pin Description

Pin	LV24020LP	Description	Remark	DC_bias
1	GND	GND (Analog and Digital GND)		
2	RESERVED		Do not connect	
3	NC			
4	FM-ANT1	Antenna input		
5	FM-ANT2	Antenna GND	Connect to GND	
6	GND	GND (Analog and Digital GND)		
7	NC			
8	NC			
9	NC			
10	NC			
11	LINE-OUT-L	Radio Lch Line-output		1.2V
12	LINE-OUT-R	Radio Rch Line-output		1.2V
13	Package-GND	GND for Package-shield		
14	Package-GND	GND for Package-shield		
15	Package-GND	GND for Package-shield		
16	Package-GND	GND for Package-shield		
17	Package-GND	GND for Package-shield		
18	Package-GND	GND for Package-shield		
19	NC			
20	NC			
21	MPX	MPX-signal output		V _{CC} -0.3V
22	NC			
23	V _{CC}	Analog supply voltage		
24	NC			
25	V _{stabi.}	Stabilizer voltage		2.7V
26	NC			
27	V _{DD}	Digital supply voltage		
28	NR_W	Digital interface Read/Write		
29	DATA	Digital interface DATA		
30	CLOCK	Digital interface Clock		
31	CLK_IN	Reference clock-source input for measurement	Connect to GND if not used	
32	NC			
33	Package-GND	GND for Package-shield		
34	Package-GND	GND for Package-shield		
35	Package-GND	GND for Package-shield		
36	Package-GND	GND for Package-shield		
37	Package-GND	GND for Package-shield		
38	Package-GND	GND for Package-shield		
39	NC			
40	V _{I/O}	Digital interface supply voltage		

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Block Diagram

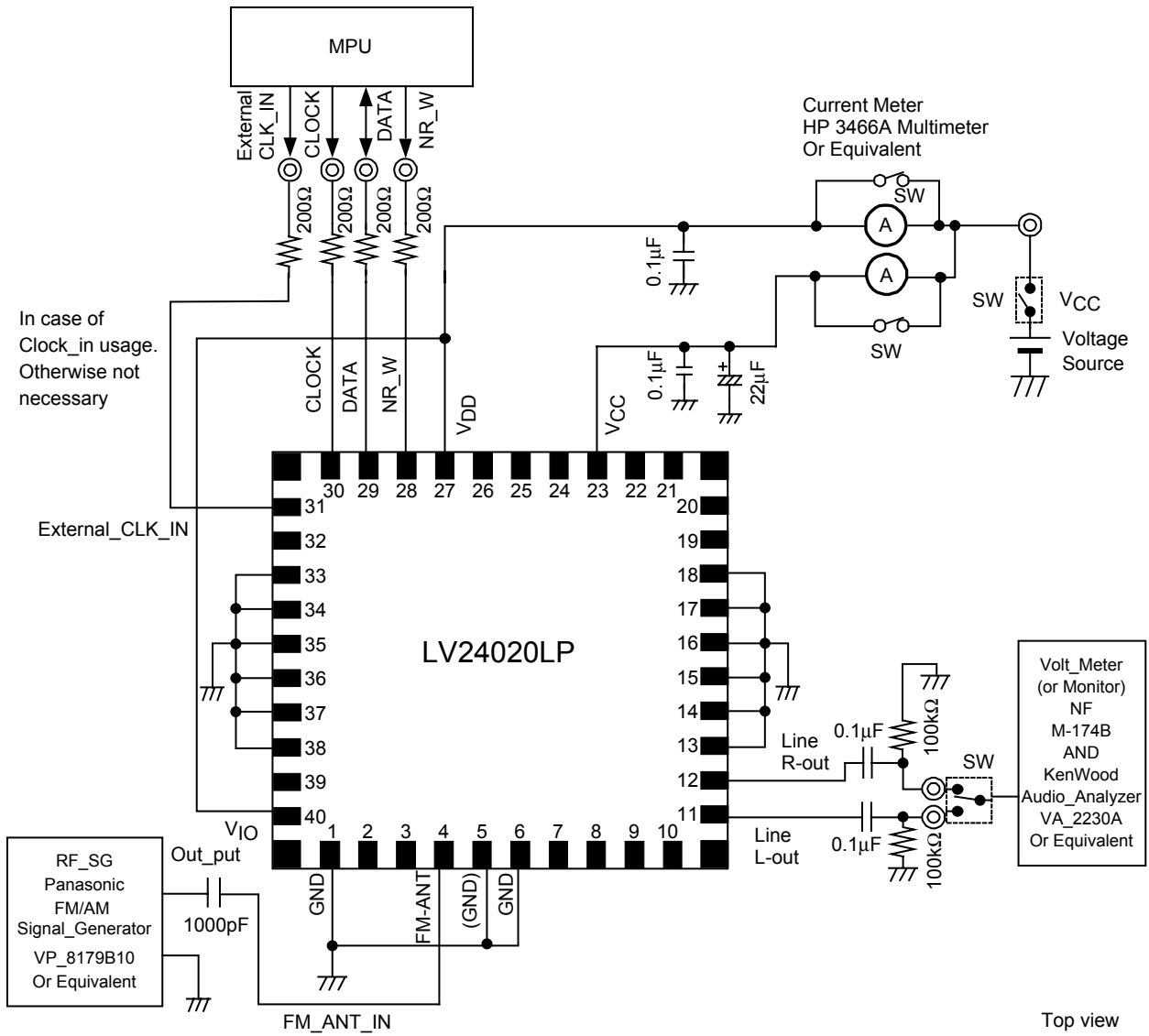


Top view
VQLP40 package

ILV000223

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Measurement Circuit

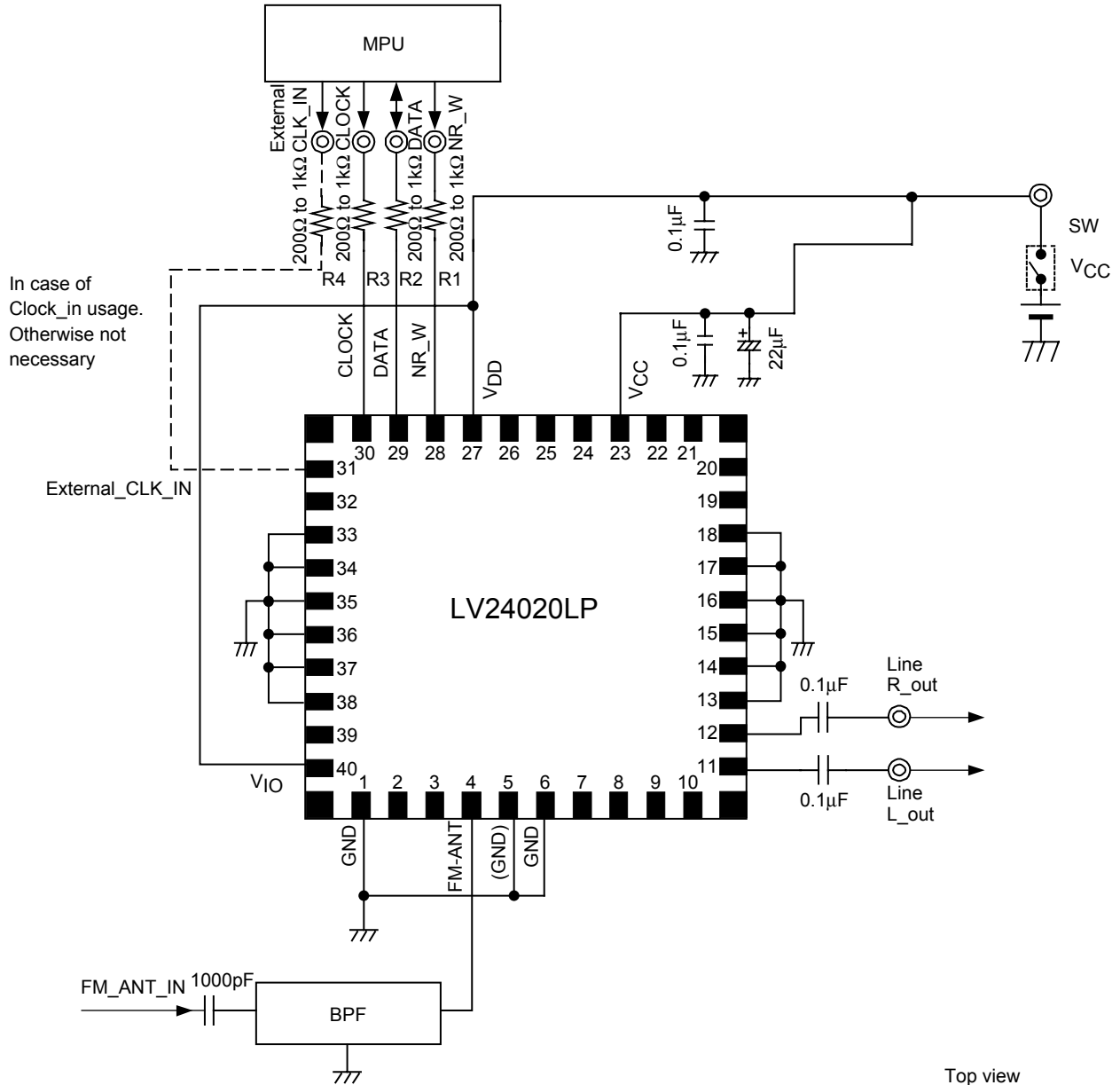


Top view
VQLP40 package

ILV000224

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Application Circuit



Top view
VQLP40 package

ILV000225

Note1: Vale of External Component is just reference. Please set most suitable value under Aactual_operation.

Note2: In case of necessary about BPF for FM_in, Please take Consideration of most suitable_value.

Note3: We recommend to put R1, R2, R3, R4 for interface between MPU and IC.

Note4: Please put Capacitor Between V_{DD} and GND also, put Capacitor Between V_{CC} and GND as shown on application.

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