

PJSDA05C-4

TVS ARRAY QUAD FOR ESD PROTECTION

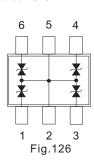
This Penta TVS Array has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5Vdc and below. This TVS array offers an integrated solution to protect up to 4 data lines where the board space is a premium.

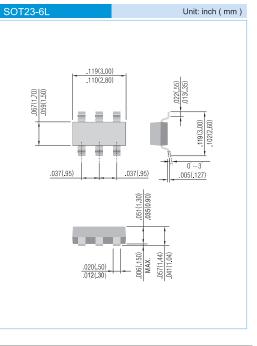
FEATURES

- 80W power dissipation (8/20µs waveform)
- \bullet Low leakage current,maximum of 1µA@5Vdc
- Very low clamping voltage
- IEC61000-4-2 ESD 15kV air, 8kV Contact Compliance
- In compliance with EU RoHS 2002/95/EC directives

MECHANICAL DATA

- Case: SOT23-6L molded plastic
- Terminals: Solder plated, solderable per MIL-STD-750, Method 2026
- Weight: 0.0005 ounce, 0.0141 gram
- Marking : QCG



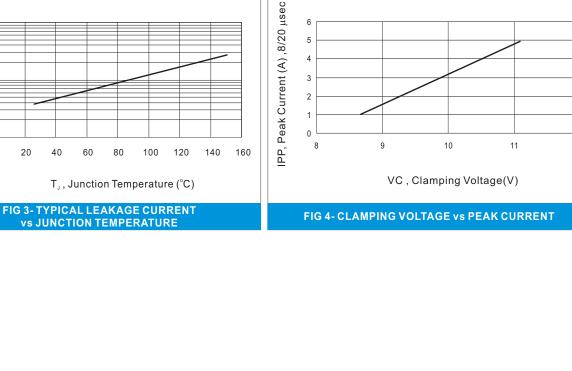


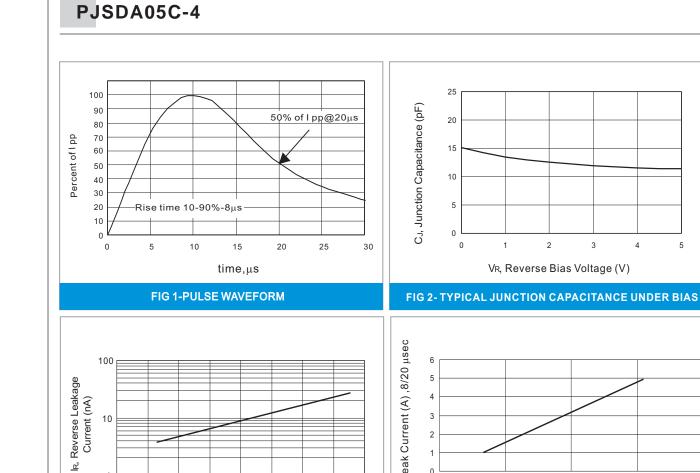
MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	Ррр	80	w
Peak Pulse Current (8/20µs Waveform)	I pp	5.0	A
ESD Voltage (HBM)	Vesd	>25	kV
Operating Temperature Range	ТJ	-55 to + 150	°C
Storage Temperature Range	Тѕтс	-55 to + 150	°C

ELECTRICAL CHARACTERISTICS TJ=25°C

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Reverse Stand-Off Voltage	Vrwm	-	-	-	5.0	V
Reverse Breakdown Voltage	Vbr	I BR=1mA	6.2	-	8.0	V
Reverse Leakage Current	IR	V _R =5V	-	-	1	μΑ
Clamping Voltage (8/20µs)	Vc	I PP=1A	-	-	12	V
Clamping Voltage (8/20µs)	Vc	I pp=4A	-	-	15	V
Off State Junction Capacitance	CJ	0Vdc Bias f=1MHz Between I/O pins and pin 2	-	15	17	pF
Off State Junction Capacitance	CJ	5Vdc Bias f=1MHz Between I/O pins and pin 2	-	7	10	pF





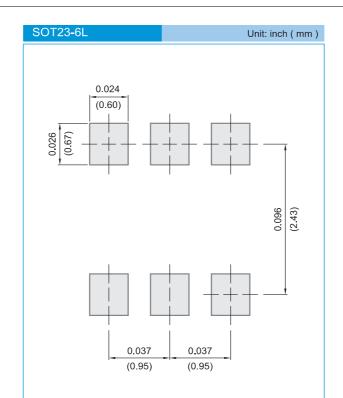






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MOUNTING PAD LAYOUT



ORDER INFORMATION

Packing information
T/R - 10K per 13" plastic Reel
T/R - 3K per 7" plastic Reel

LEGAL STATEMENT

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