CompactFlash Card

SST48CF008 / 016 / 024 / 032 / 048 / 064 / 096 / 128 / 192 / 256

Data Sheet

FEATURES:

- **CompactFlash Association specification standard**
- **8, 16, 24, 32, 48, 64, 96, 128, 192, and 256 MByte capacities**
- **Small Form Factor: 36.4 mm x 42.8 mm x 3.3 mm**
- **Supports 5.0-Volt and 3.3-Volt Read and Write**
  - 4.5-5.5V, 3.135-3.465V for commercial
- **PC Card ATA and True IDE interface**
  - 512 Bytes sector
  - ATA command set compatible
- **Low Power Consumption:**
  - Active mode: 35 mA/55 mA (3.3V/5.0V)(typical)
  - Sleep mode: 100 µA/150 µA (3.3V/5.0V)(typical)
- **Data Transfer Rate to/from Host**
  - 20 MB/s burst at 5.0V
  - 6.6 MB/s burst at 3.3V
- **High Performance**
  - Up to 1.4 MB/sec sustained write transfer rate (host to flash)
- **Controller Overhead Command to DRQ**
  - Less than 0.5 ms
- **Zero Data Retention Power**
  - Batteries not required for data storage
- **Start Up Time**
  - Sleep to Read: 200 ns
  - Sleep to Write: 200 ns
  - Reset to Ready: 50 ms typical, 400 ms Max.
- **Support for Commercial Temperature Range**
  - 0°C to +70°C for operating commercial
  - -25°C to +85°C non-operating (storage)
- **Extremely Rugged and Reliable**
  - Built-in ECC support corrects 3 random Bytes error per 512 Byte sector
  - 2000 G operating and non-operating shock
- **Intelligent ATA/IDE Controller**
  - Built-in microcontroller with intelligent firmware
  - 256 Bytes of attribute memory for storing CIS information
  - Supports multiple-sector Read/Write operation to enhance system performance
- **Power Management Unit**
  - Immediate disabling of unused circuitry

PRODUCT DESCRIPTION

SST's CompactFlash (CF) card is an ultra-small, low cost, high performance, removable flash memory data storage system. This technology is well suited for solid state mass storage portable applications offering new and expanded functionality while enabling smaller and lighter designs.

CompactFlash technology is widely used in a variety of consumer products such as portable computers, digital cameras, handheld data collection scanners, Personal Digital Assistants (PDAs), handy terminals, audio players, monitoring devices and set-top boxes.

SST's CompactFlash products provide complete PCMCIA-ATA functionality and compatibility. This is achieved because the 50-pin CF card can be easily slipped into a passive 68-pin Type II adapter card that fully meets PCMCIA electrical and mechanical interface specifications. SST's CompactFlash products are also fully compliant with CFA standards. The SST CF card is read and written to using a single power supply of 5.0V or 3.3V and is available in 8 to 256 MByte densities.

SST's CompactFlash cards contain additional attribute memory of 256 Bytes for storing the Card Information Structure (CIS) information. SST's CompactFlash card has built in microcontroller and file management firmware that communicates with ATA standard interfaces; therefore, the SST's CompactFlash cards do not require additional software for the host, such as Flash File System (FFS) and Memory Technology Driver (MTD).

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1.0 GENERAL DESCRIPTION

The SST's CompactFlash card contains a controller, embedded firmware storage and flash media in a match-book sized package with a 50-pin connector consisting of two rows of 25 female contacts each on 50 mil (1.27 mm) centers. Refer to Figure 1 for SST's CompactFlash card block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

1.1 Performance-optimized ATA Controller

The heart of a CompactFlash card is the ATA controller which translates standard IDE/ATA signals into flash media data and controls. SST's CompactFlash card contains a proprietary ATA controller that was specifically designed to attain high data throughput from host to flash. The following components contribute to the ATA controller's performance.

1.1.1 Microcontroller Unit (MCU)

The MCU translates IDE/ATA commands into data and control signals required for flash memory operation.

1.1.2 Internal Direct Memory Access (DMA) Control

The ATA controller inside SST's CompactFlash card uses DMA allowing instant data transfer to memory. This implementation eliminates controller overhead associated with traditional, firmware based, memory control, increasing data transfer rate.

1.1.3 Power Management Unit (PMU)

Power Management Unit controls the power consumption of the CompactFlash card. The PMU dramatically extends product battery life by putting the part of the circuitry that is not in operation into sleep mode.

1.1.4 SRAM Buffer

A key contributor to the ATA controller performance is a SRAM buffer. The buffer optimizes host's data writes to flash media.

1.1.5 Embedded Flash File System

Embedded Flash File System is an integral part of the SST's ATM controller. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media Writes and Reads.
2. Provides flash media wear leveling to spread the flash writes across all the memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.

1.1.6 Error Correction Code (ECC)

The ATA Controller contains ECC algorithm that corrects 3 bytes of error per 512 Byte sector.

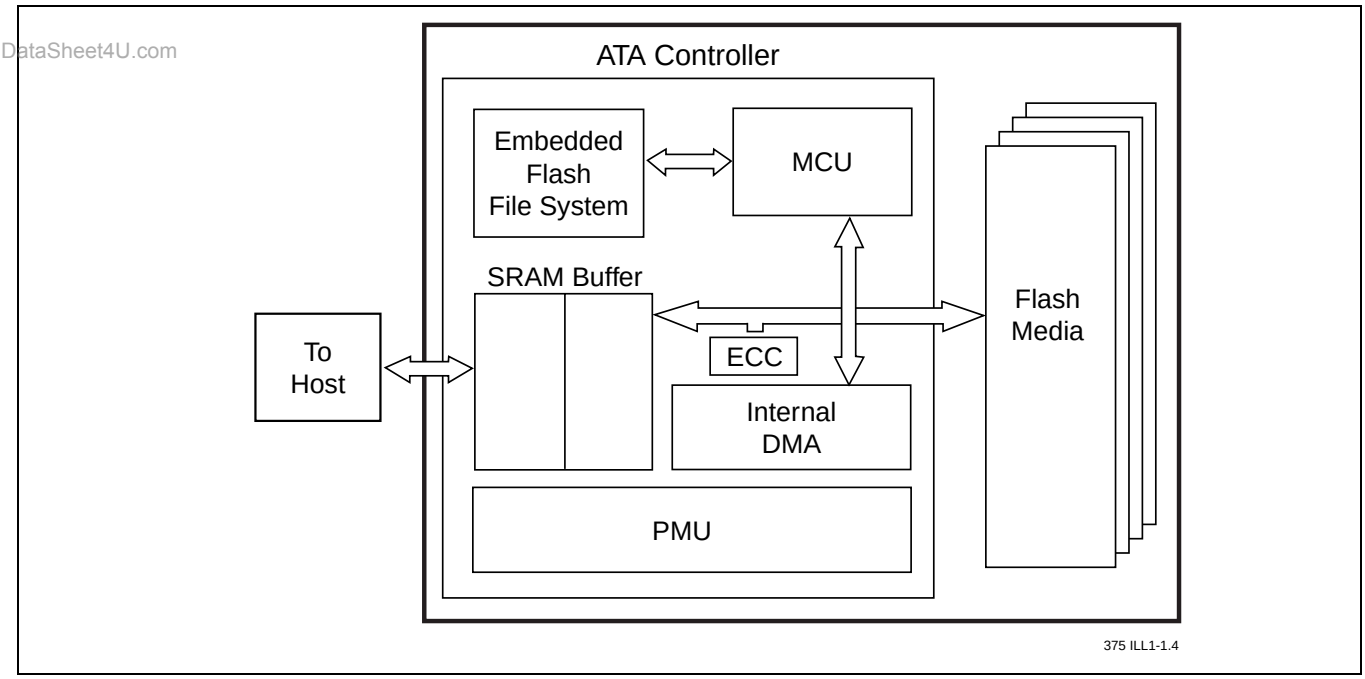

FIGURE 1: SST COMPACTFLASH BLOCK DIAGRAM

1.2 SST's CompactFlash Card Product Offering

The SST48CFxxx High CompactFlash product family is available in 8 to 256 MByte densities. The following table shows the specific capacity, default number of cylinder heads, sectors and cylinders for each product line.

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Model Number	Density	Total Bytes	Cylinders	Heads	Sectors
SST48CF008	8 MB	8,028,160	245	2	32
SST48CF016	16 MB	16,023,552	489	2	32
SST48CF024	24 MB	24,051,712	367	4	32
SST48CF032	32 MB	32,047,104	489	4	32
SST48CF048	48 MB	48,037,888	733	4	32
SST48CF064	64 MB	64,028,672	977	4	32
SST48CF096	96 MB	96,075,776	733	8	32
SST48CF128	128 MB	128,057,344	977	8	32
SST48CF192	192 MB	192,151,552	733	16	32
SST48CF256	256 MB	256,114,688	977	16	32

2.0 ELECTRICAL INTERFACE

2.0.1 Pin Assignment and Pin Type

The signal/pin assignments are listed in Table 2-1. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Section 2.3 defines the DC characteristics for all input and output type structures.

2.1 Electrical Description

The CompactFlash card functions in three basic modes: 1) PC Card ATA using I/O Mode, 2) PC Card ATA using Memory Mode and 3) True IDE Mode, which is compatible with most disk drives. The configuration of the CompactFlash card will be controlled using the standard PCMCIA configuration registers starting at address 200H in the Attribute Memory space of the storage card or for True IDE Mode, pin 9 being grounded.

Table 2-2 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the CompactFlash card sources are outputs. The CompactFlash card logic levels conform to those specified in the PCMCIA Release 2.1 and CFA Specification Rev. 1.4. As shown in Table 2-2, each signal has three possible operating modes: 1) PC Card Memory, 2) PC Card I/O and 3) True IDE. All outputs from the card are totem pole except the data bus signals which are bi-directional tri-state. Refer to Section 2.3 for definitions of Input and Output type.

2.2 Card Pin Assignment

TABLE 2-1: CARD PIN ASSIGNMENT (1 OF 2)

Pin No.	Memory card mode			I/O card mode			True IDE mode		
	Signal Name	Pin Type	I/O Type[1]	Signal Name	Pin Type	I/O Type[1]	Signal Name	Pin Type	I/O Type[1]
1	GND	-	GND	GND	-	GND	GND	-	GND
2	D_3	I/O	I2D, O2	D_3	I/O	I2D, O2	D_3	I/O	I2D, O2
3	D_4	I/O	I2D, O2	D_4	I/O	I2D, O2	D_4	I/O	I2D, O2
4	D_5	I/O	I2D, O2	D_5	I/O	I2D, O2	D_5	I/O	I2D, O2
5	D_6	I/O	I2D, O2	D_6	I/O	I2D, O2	D_6	I/O	I2D, O2
6	D_7	I/O	I2D, O2	D_7	I/O	I2D, O2	D_7	I/O	I2D, O2
7	-CE1	I	I3U	-CE1	I	I3U	-CS0	I	I3U
8	A10	I	I2D	A10	I	I2D	A10	I	I2D
9	-OE	I	I3U	-OE	I	I3U	-ATASEL	I	I3U
10	A_9	I	I2D	A_9	I	I2D	A_9	I	I2D
11	A_8	I	I2D	A_8	I	I2D	A_8	I	I2D
12	A_7	I	I2D	A_7	I	I2D	A_7	I	I2D
13	V_{DD}	-	-	V_{DD}	-	-	V_{DD}	-	-
14	A_6	I	I2D	A_6	I	I2D	A_6	I	I2D
15	A_5	I	I2D	A_5	I	I2D	A_5	I	I2D
16	A_4	I	I2D	A_4	I	I2D	A_4	I	I2D
17	A_3	I	I2D	A_3	I	I2D	A_3	I	I2D
18	A_2	I	I2D	A_2	I	I2D	A_2	I	I2D
19	A_1	I	I2D	A_1	I	I2D	A_1	I	I2D
20	A_0	I	I2D	A_0	I	I2D	A_0	I	I2D
21	D_0	I/O	I2D, O2	D_0	I/O	I2D, O2	D_0	I/O	I2D, O2
22	D_1	I/O	I2D, O2	D_1	I/O	I2D, O2	D_1	I/O	I2D, O2
23	D_2	I/O	I2D, O2	D_2	I/O	I2D, O2	D_2	I/O	I2D, O2
24	WP	O	O2	-IOIS16	O	O2	-IOIS16	O	O2
25	-CD2	O	Ground	-CD2	O	Ground	-CD2	O	Ground
26	-CD1	O	Ground	-CD1	O	Ground	-CD1	O	Ground
27	D_{11}	I/O	I2D, O2	D_{11}	I/O	I2D, O2	D_{11}	I/O	I2D, O2
28	D_{12}	I/O	I2D, O2	D_{12}	I/O	I2D, O2	D_{12}	I/O	I2D, O2
29	D_{13}	I/O	I2D, O2	D_{13}	I/O	I2D, O2	D_{13}	I/O	I2D, O2
30	D_{14}	I/O	I2D, O2	D_{14}	I/O	I2D, O2	D_{14}	I/O	I2D, O2
31	D_{15}	I/O	I2D, O2	D_{15}	I/O	I2D, O2	D_{15}	I/O	I2D, O2
32	-CE2	I	I3U	-CE2	I	I3U	-CS1	I	I3U
33	-VS1	O	Ground	-VS1	O	Ground	-VS1	O	Ground
34	-IORD	I	I3U	-IORD	I	I3U	-IORD	I	I3U
35	-IOWR	I	I3U	-IOWR	I	I3U	-IOWR	I	I3U
36	-WE	I	I3U	-WE	I	I3U	-WE	I	I3U
37	RDY/-BSY	O	O1	-IREQ	O	O1	INTRQ	O	O1
38	V_{DD}	-	-	V_{DD}	-	-	V_{DD}	-	-
39	-CSEL	I	I2U	-CSEL	I	I2U	-CSEL	I	I2U
40	-VS2	O	open	-VS2	O	open	-VS2	O	open

TABLE 2-1: CARD PIN ASSIGNMENT (CONTINUED) (2 OF 2)

Pin No.	Memory card mode			I/O card mode			True IDE mode		
	Signal Name	Pin Type	I/O Type[1]	Signal Name	Pin Type	I/O Type[1]	Signal Name	Pin Type	I/O Type[1]
41	RESET	I	I4U	RESET	I	I4U	-RESET	I	I4U
42	-WAIT	O	O1	-WAIT	O	O1	IORDY	O	O1
43	-INPACK	O	O1	-INPACK	O	O1	-INPACK	O	O1
44	-REG	I	I3U	-REG	I	I3U	-REG	I	I3U
45	BVD2	O	I2U, O1	-SPKR	O	I2U, O1	-DASP	O	I2U, O1
46	BVD1	O	I2U, O1	-STSCHG	O	I2U, O1	-PDIAG	O	I2U, O1
47	D_8	I/O	I2D, O2	D_8	I/O	I2D, O2	D_8	I/O	I2D, O2
48	D_9	I/O	I2D, O2	D_9	I/O	I2D, O2	D_9	I/O	I2D, O2
49	D_{10}	I/O	I2D, O2	D_{10}	I/O	I2D, O2	D_{10}	I/O	I2D, O2
50	GND	-	GND	GND	-	GND	GND	-	GND

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1. Please refer to Sections 2.3.1 to 2.3.4 for detail.

TABLE 2-2: SIGNAL DESCRIPTION (1 OF 4)

Symbol	Type[1]	Pin	Name and Functions
A_{10} - A_0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash card, the memory mapped port address registers within the CompactFlash card, a byte in the card's information structure and its configuration control and status registers.
A_{10} - A_0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal
A_2 - A_0 (True IDE Mode	I	18,19,20	In True IDE Mode only A[2:0] are used to select the one of eight (True IDE Mode) registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode)			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
Status Changed -PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash card. They are used by the host to determine that the CompactFlash card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the Odd Byte of the word. -CE1 accesses the Even Byte or the Odd Byte of the word depending on A_0 and -CE2. A multiplexing scheme based on A_0, -CE1, -CE2 allows 8 bit hosts to access all data on D_0-D_7. See Tables 2-11, 2-13, 2-16, 2-17, and 2-18.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.

TABLE 2-2: SIGNAL DESCRIPTION (CONTINUED) (2 OF 4)

Symbol	Type[1]	Pin	Name and Functions
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in Byte-Mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
GND (PC Card Memory Mode)	-	1,50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
-INPACK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the CompactFlash Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash card and the CPU.
-INPACK (True IDE Mode)			In True IDE Mode this output signal is not used and should not be connected at the host.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash card controller registers when the CompactFlash card is configured to use the I/O interface.
-IOWR (True IDE Mode)			The clocking will occur on the negative to positive edge of the signal (trailing edge). In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

TABLE 2-2: SIGNAL DESCRIPTION (CONTINUED) (3 OF 4)

Symbol	Type[1]	Pin	Name and Functions
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/-BSY PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the CompactFlash Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the CompactFlash card has completed its power up or reset function. No access of any type should be made to the CompactFlash card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash Card has been powered up with +RESET continuously disconnected or asserted.
-IREQ PC Card I/O Mode)			I/O Operation - After the CompactFlash card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory Attribute Memory Select accesses. High for Common Memory, Low for Attribute Memory.
-REG PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to V_{DD} by the host.
RESET (PC Card Memory Mode)	I	41	When the pin is high, this signal Resets the CompactFlash Card. The CompactFlash card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
V_{DD} (PC Card Memory Mode)	-	13,38	+5.0V, +3.3V power.
V_{DD} (PC Card I/O Mode)			This signal is the same for all modes.
V_{DD} (True IDE Mode)			This signal is the same for all modes.

TABLE 2-2: SIGNAL DESCRIPTION (CONTINUED) (4 OF 4)

Symbol	Type[1]	Pin	Name and Functions
-VS1 -VS2 (PC Card Memory Mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded so that the CompactFlash card CIS can be read at 3.3V and -VS2 is reserved by PCMCIA for a secondary voltage.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.
-WAIT (PC Card Memory Mode)	O	42	The -WAIT signal is driven low by the CompactFlash
			Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode)			In True IDE Mode this output signal may be used as IORDY.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to V_{DD} by the host.
WP (PC Card Memory Mode) Write Protect	O	24	Memory Mode - The CompactFlash card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation - When the CompactFlash card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or Odd Byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

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1. I = Input
   0 = Output

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2.3 Electrical Specification

The following table defines all D.C. Characteristics for the SST CompactFlash card product family.

Unless otherwise stated, conditions are:

Non operating (storage) temperature range -25°C to +85°C

V_{DD} = 4.5-5.5V

V_{DD} = 3.135-3.465V

Ta = 0°C to +70°C

ABSOLUTE MAXIMUM CONDITIONS

Parameter	Symbol	Conditions
Input Power	V_{DD}	-0.3V min. to 6.5V Max
Voltage on any pin except V_{DD} with respect to GND	V	-0.5V min. to V_{DD} + 0.5V Max

INPUT POWER

Voltage	Maximum Average RMS Active Current	Maximum Average RMS Sleep Current	Measurement Method
3.135-3.465V	75 mA	200 µA	3.3V at 25°C[1]
4.5-5.5V	100 mA	300 µA	5.0V at 25°C[1]

1. Current measurement is accomplished by connecting an amp meter (set to the 2 amp scale range) in series with the V_{DD} supply to the CompactFlash card. Current measurements are to be taken while looping on a data transfer command with a sector count of 128. Current consumption values for both Read and Write commands are not to exceed the Maximum Average RMS Current specified in this table

CompactFlash products shall operate correctly in both voltage ranges as shown in the table above. To comply with this specification, current requirements must not exceed the maximum limit.

2.3.1 Input Leakage Current

In the table below, x refers to the characteristics described in Section 2.3.2. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
IxZ	Input Leakage Current	IL	$V_{IH} = V_{DD}$ / V_{IL} = GND	-1		1	µA
IxU	Pull Up Resistor	RPU1	V_{DD} = 5.0V	50k		500k	Ohm
IxD	Pull Down Resistor	RPD1	V_{DD} = 5.0V	50k		500k	Ohm

2.3.2 Input Characteristics

Type	Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
			V_{DD} = 3.3V			V_{DD} = 5.0V			
1	Input Voltage	V_{IH}	2.4			2.4			Volts
	CMOS	V_{IL}			0.6			0.8	
2	Input Voltage	V_{IH}	2.0			2.7			Volts
	CMOS	V_{IL}			0.8			0.8	
3	Input Voltage	V_{TH}		2.0			2.4		Volts
	CMOS Schmitt Trigger	V_{TL}		0.5			0.8		
4	Input Voltage CMOS	V_{TH}		1.8			2.4		Volts
	Schmitt Trigger	V_{TL}		0.9			0.8		

2.3.3 Output Drive Type

All output drive type are CMOS level.

2.3.4 Output Drive Characteristics

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
O1	Output Voltage	V_{OH}	I_{OH} = -4 mA	V_{DD} -0.8V			Volts
		V_{OL}	I_{OL} = 4 mA			GND +0.4V	
O2	Output Voltage	V_{OH}	I_{OH} = -8 mA	V_{DD} -0.8V			Volts
		V_{OL}	I_{OL} = 8 mA			GND +0.4V	

2.3.5 Interface/Bus Timing

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, a direct mapped I/O transfer and a memory access. The two timing sequences are explained in detail in the PCMCIA PC Card Standard. SST's CompactFlash card conforms to the timing in that reference document.

2.3.6 Attribute Memory Read Timing Specification

The Attribute Memory access time is defined as 100 ns. Detailed timing specifications are shown in Table 2-3.

TABLE 2-3: ATTRIBUTE MEMORY READ TIMING

Speed Version			100 ns	
Item	**Symbol**	**IEEE Symbol**	**Min[1]**	**Max[1]**
Read Cycle Time	tc(R)	tAVAV	100	
Address Access Time	ta(A)	tAVQV		100
Card Enable Access Time	ta(CE)	tELQV		100
Output Enable Access Time	ta(OE)	tGLQV		50
Output Disable Time from CE	tdis(CE)	tEHQZ		50
Output Disable Time from OE	tdis(OE)	tGHQZ		50
Address Setup Time	tsu(A)	tAVGL	10	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

T2-3.1 375

1. All times are in nanoseconds. D_{OUT} signifies data provided by the CompactFlash card to the system. The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.
All AC specifications are guaranteed by design.

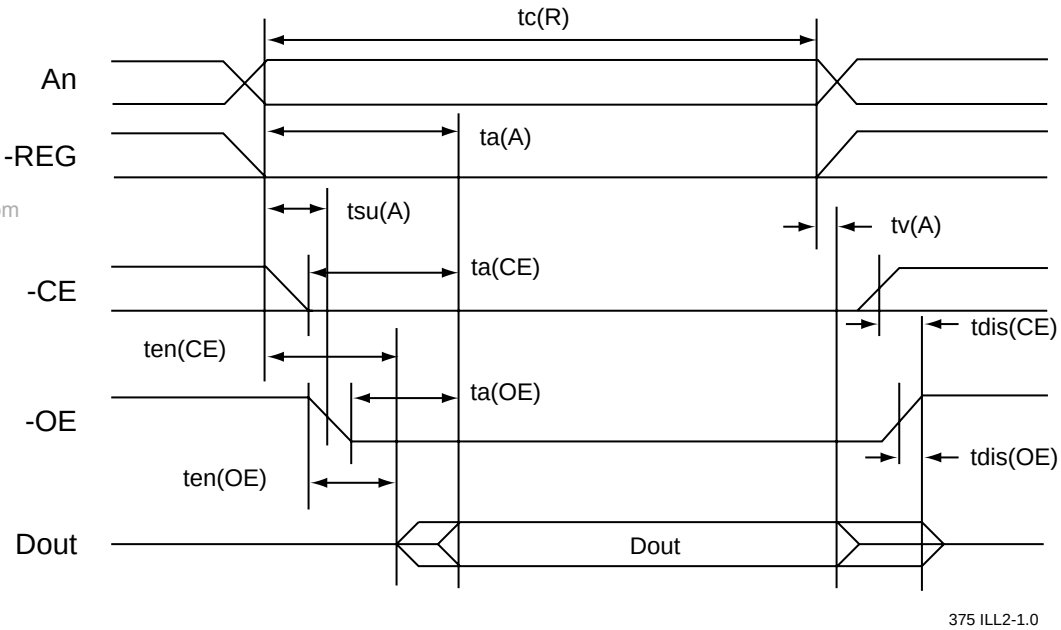

FIGURE 2-1: ATTRIBUTE MEMORY READ TIMING DIAGRAM

2.3.7 Configuration Register (Attribute Memory) Write Timing specification

The Card Configuration write access time is defined as 100 ns. Detailed timing specifications are shown in Table 2-4.

TABLE 2-4: CONFIGURATION REGISTER (ATTRIBUTE MEMORY) WRITE TIMING

Speed Version			100 ns	
Item	**Symbol**	**IEEE Symbol**	**Min[1]**	**Max[1]**
Write Cycle Time	tc(W)	tAVAV	100	
Write Pulse Width	tw(WE)	tWLWH	60	
Address Setup Time	tsu(A)	tAVWL	10	
Write Recovery Time	trec(WE)	tWMAX	15	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	40	
Data Hold Time	th(D)	tWMDX	15	

T2-4.1 375

1. All times are in nanoseconds. D_{IN} signifies data provided by the system to the CompactFlash card. All AC specifications are guaranteed by design.

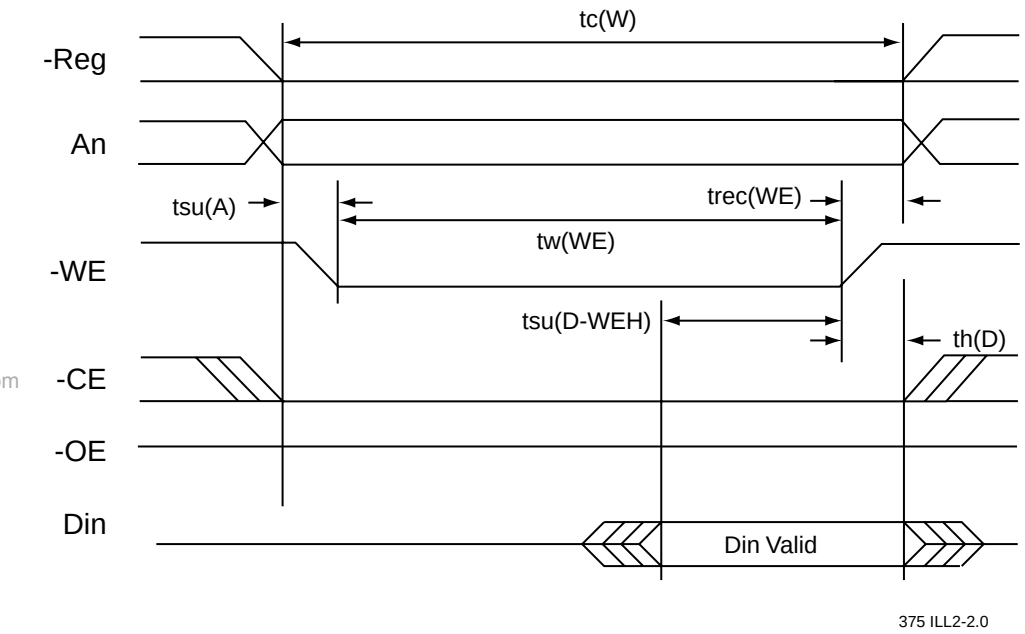

FIGURE 2-2: CONFIGURATION REGISTER (ATTRIBUTE MEMORY) WRITE TIMING DIAGRAM

2.3.8 Common Memory Read Timing Specification

TABLE 2-5: COMMON MEMORY READ TIMING

Item	Symbol	IEEE Symbol	Min[1] ns	Max[1] ns
Output Enable Access Time	ta(OE)	tGLQV		50
Output Disable Time from OE	tdis(OE)	tGHQZ		50
Address Setup Time	tsu(A)	tAVGL	10	
Address Hold Time	th(A)	tGHAX	15	
CE Setup before OE	tsu(CE)	tELGL	0	
CE Hold following OE	th(CE)	tGHEH	15	

T2-5.1 375

1. All times are in nanoseconds.
   All AC specifications are guaranteed by design.

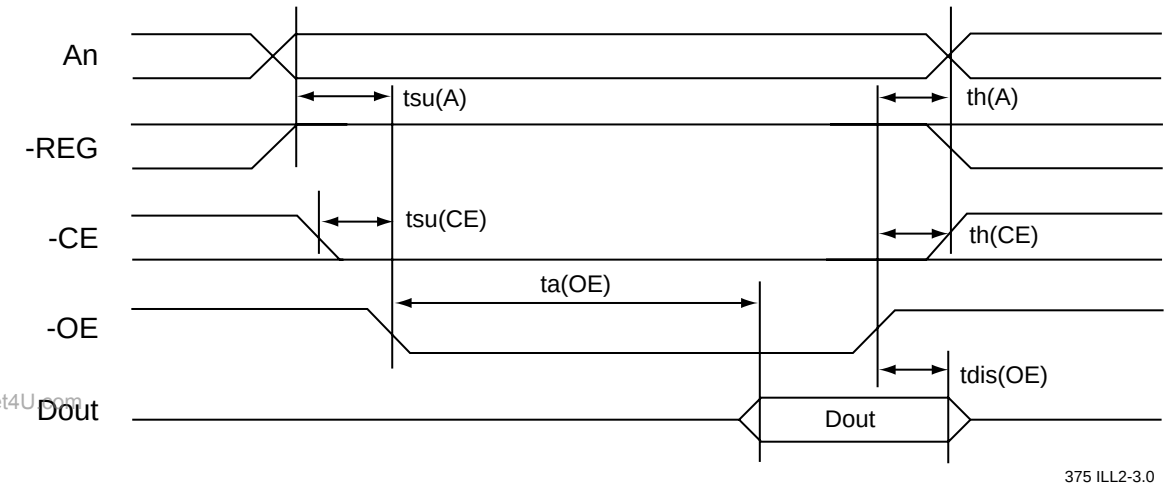

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FIGURE 2-3: COMMON MEMORY READ TIMING DIAGRAM

2.3.9 Common Memory Write Timing Specification

TABLE 2-6: COMMON MEMORY WRITE TIMING

Item	Symbol	IEEE Symbol	Min[1] ns	Max[1] ns
Data Setup before WE	tsu(D-WEH)	tDVWH	40	
Data Hold following WE	th(D)	tWMDX	15	
WE Pulse Width	tw(WE)	tWLWH	60	
Address Setup Time	tsu(A)	tAVWL	10	
CE Setup before WE	tsu(CE)	tELWL	0	
Write Recovery Time	trec(WE)	tWMAX	15	
Address Hold Time	th(A)	tGHAX	15	
CE Hold following WE	th(CE)	tGHEH	15	

T2-6.1 375

1. All times are in nanoseconds.
   All AC specifications are guaranteed by design.

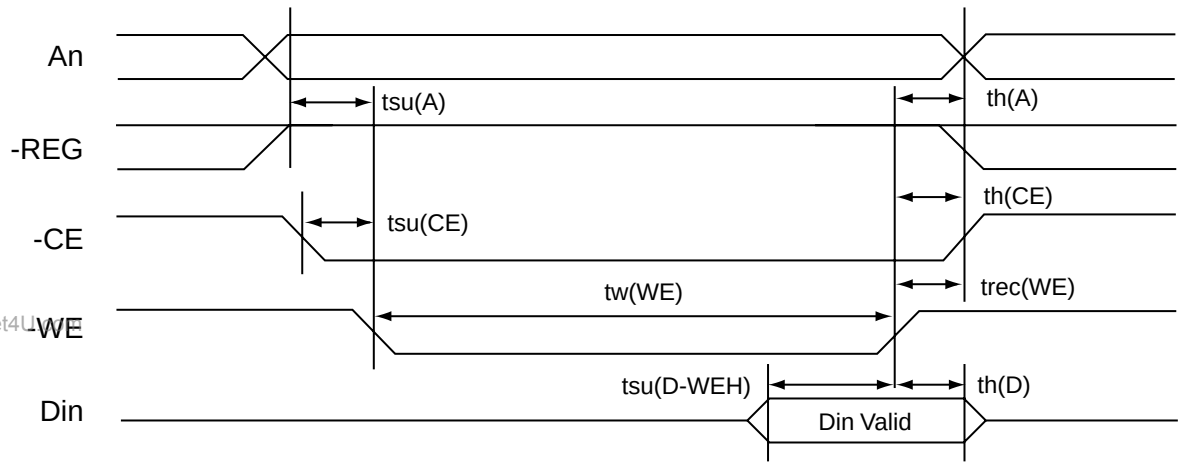

FIGURE 2-4: COMMON MEMORY WRITE TIMING DIAGRAM

2.3.10 I/O Input (Read) Timing Specification

TABLE 2-7: I/O READ TIMING

Item	Symbol	IEEE Symbol	Min[1]	Max[1]
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

T2-7.1 375

1. All times are in nanoseconds.

Note: The maximum load on -INPACK and -IOIS16 is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.

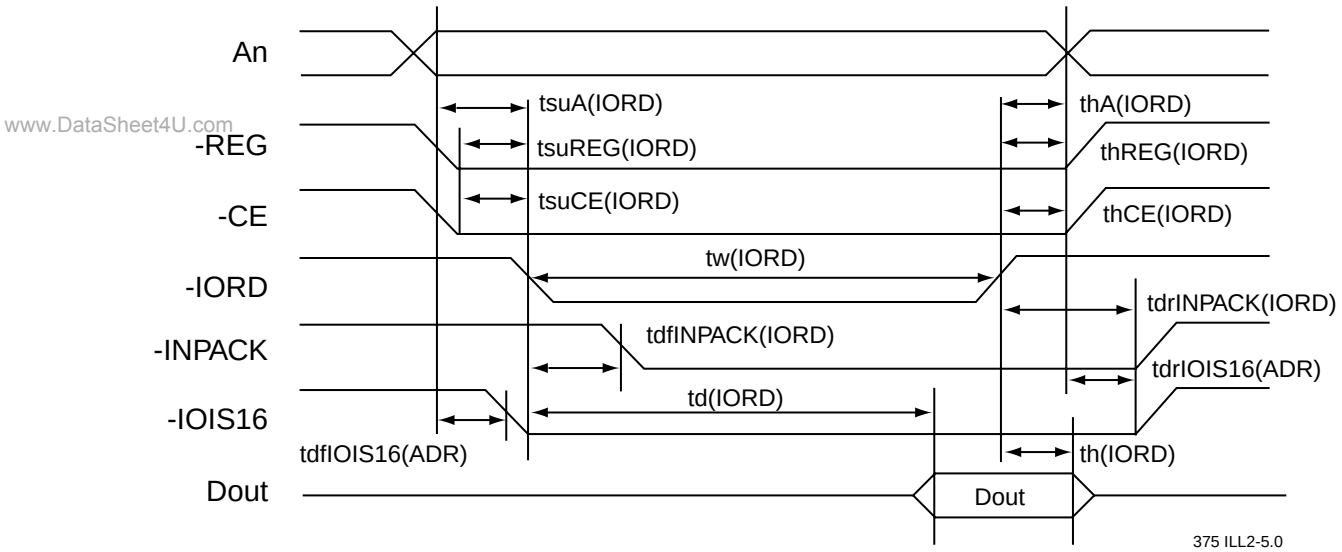

FIGURE 2-5: I/O READ TIMING DIAGRAM

2.3.11 I/O Output (Write) Timing Specification

TABLE 2-8: I/O WRITE TIMING

Item	Symbol	IEEE Symbol	Min[1]	Max[1]
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

T2-8.1 375

1. All times are in nanoseconds.

Note: The maximum load on -INPACK, and -IOIS16 is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.

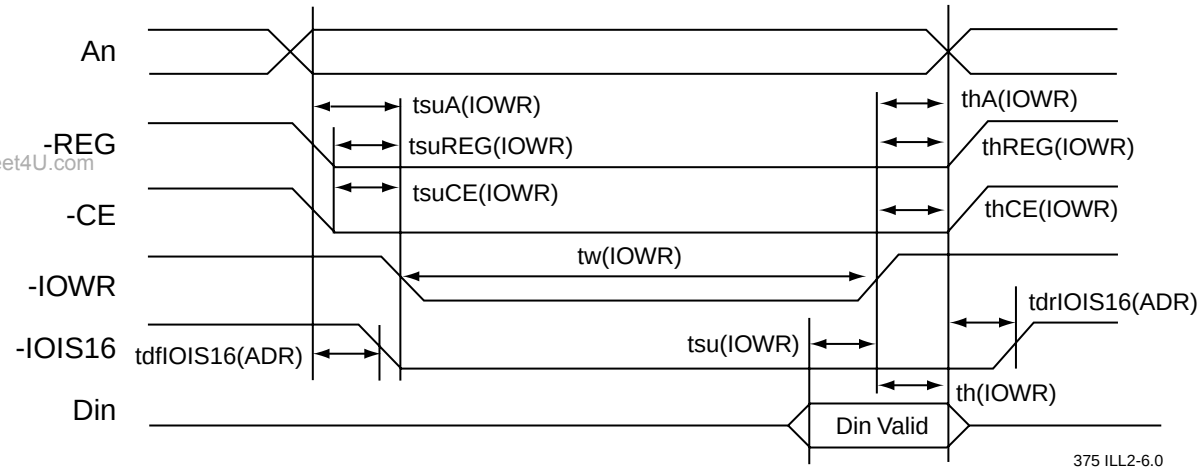

FIGURE 2-6: I/O WRITE TIMING DIAGRAM

2.3.12 True IDE Mode I/O Input (Read) Timing Specification

TABLE 2-9: TRUE IDE MODE I/O READ TIMING DIAGRAM

Item	Symbol	IEEE Symbol	Min[1]	Max[1]
Data Delay after IORD	td(IORD)	tIGLQV		50
Data Hold following IORD	th(IORD)	tIGHQX	5	
IORD Width Time	tw(IORD)	tIGLIGH	70	
Address Setup before IORD	tsuA(IORD)	tAVIGL	25	
Address Hold following IORD	thA(IORD)	tIGHAX	10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	10	
CE Hold following IORD	thCE(IORD)	tIGHEH	5	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		20
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		20

T2-9.2 375

1. All times are in nanoseconds.

Note: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.

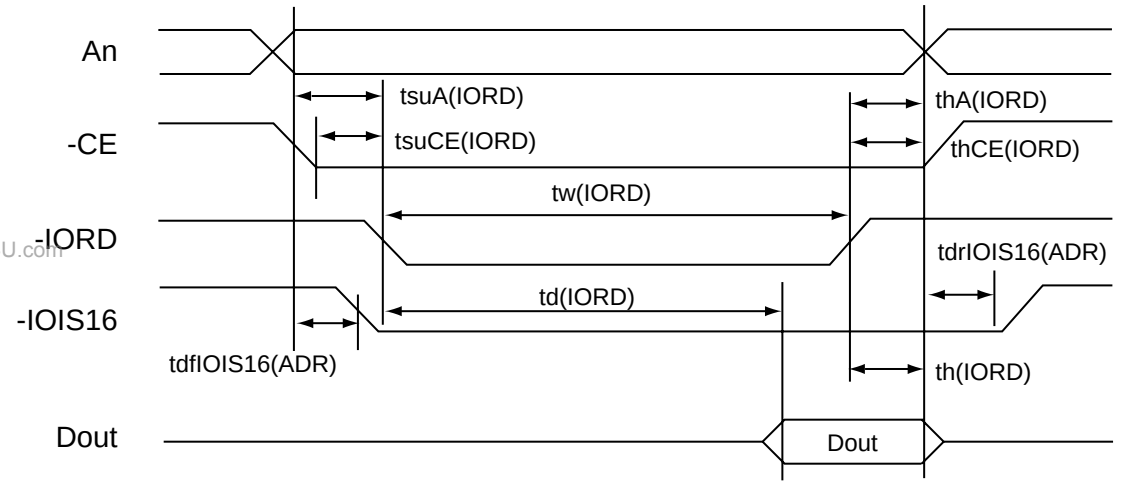

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FIGURE 2-7: TRUE IDE MODE I/O READ TIMING DIAGRAM

2.3.13 True IDE Mode I/O Output (Write) Timing Specification

TABLE 2-10: TRUE IDE MODE I/O WRITE TIMING

Item	Symbol	IEEE Symbol	Min[1]	Max[1]
Data Setup before IOWR	tsu(IOWR)	tDVIWH	20	
Data Hold following IOWR	th(IOWR)	tlWHDX	10	
IOWR Width Time	tw(IOWR)	tlWLIWH	70	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	25	
Address Hold following IOWR	thA(IOWR)	tlWHAX	10	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	10	
CE Hold following IOWR	thCE(IOWR)	tlWHEH	5	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		20
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		20

T2-10.2 375

1. All times are in nanoseconds.

Note: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.

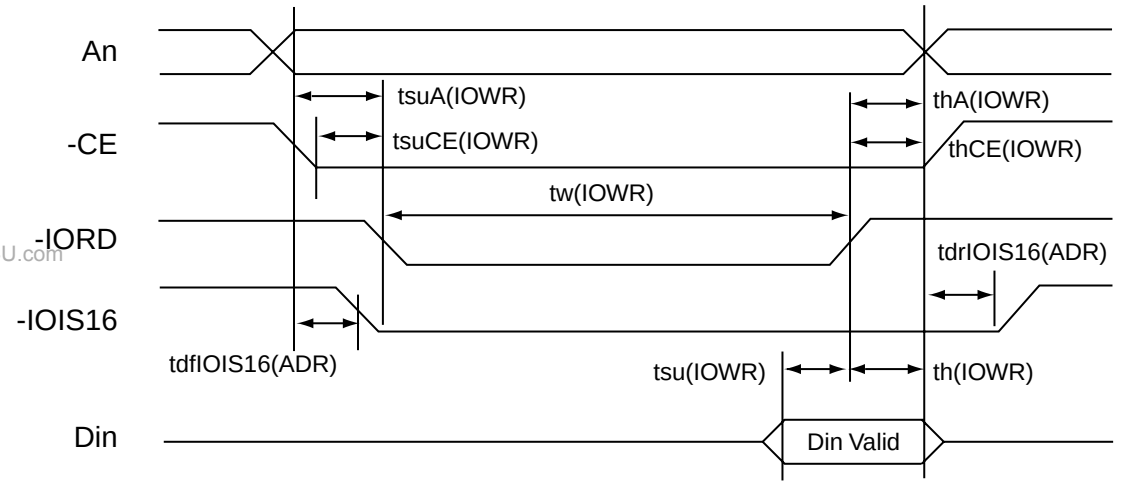

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FIGURE 2-8: True IDE Mode I/O Write Timing Diagram

2.4 Card Configuration

The CompactFlash cards are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

TABLE 2-11: REGISTERS AND MEMORY SPACE DECODING

-CE2	-CE1	-REG	-OE	-WE	A_{10}	A_9	A_8-A_4	A_3	A_2	A_1	A_0	Selected Space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit D_7-D_0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit D_{15}-D_8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 bit D_{15}-D_0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit D_7-D_0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit D_{15}-D_8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 bit D_{15}-D_0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

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TABLE 2-12: CONFIGURATION REGISTERS DECODING

-CE2	-CE1	-REG	-OE	-WE	A_{10}	A_9	A_8-A_4	A_3	A_2	A_1	A_0	Selected Register
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

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Note: The location of the card configuration registers should always be read from the CIS locations 0000H to 0198H. No writes should be performed to the CompactFlash card attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

2.4.1 Attribute Memory Function

Attribute memory is a space where CompactFlash card identification and configuration information are stored, and is limited to 8-bit wide accesses only at even addresses. The card configuration registers are also located here.

For the Attribute Memory Read function, signals -REG and -OE must be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the Even Byte and Odd Byte address, but only the Even Byte data is valid during the Attribute Memory access. Refer to Table 2-13 below for signal states and bus validity for the Attribute Memory function.

TABLE 2-13: ATTRIBUTE MEMORY FUNCTION

Function Mode	-REG	-CE2	-CE1	A_{10}	A_9	A_0	-OE	-WE	D_{15}-D_8	D_7-D_0
Standby Mode	X	V_{IH}	V_{IH}	X	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
Write Byte Access Configuration (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
Read Word Access CIS (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	Don't Care	Even Byte

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Note: The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

2.4.2 Configuration Option Register (Address 200H in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET — Soft Reset - Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the CompactFlash card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the CompactFlash card in the same un-configured Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevlREQ — This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5 — Conf0 Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the CompactFlash card as shown below.
Note: Conf5 and Conf4 are reserved and must be written as (0).

TABLE 2-14: CARD CONFIGURATIONS

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, any 16 Byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0H-1F7H/3F6H-3F7H
0	0	0	0	1	1	I/O Mapped, 170H-177H/376H-377H

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2.4.3 Card Configuration and Status Register (Address 202H in Attribute Memory)

The Card Configuration and Status Register contains information about the card's condition.

CARD CONFIGURATION AND STATUS REGISTER ORGANIZATION

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed — Indicates that one or both of the Pin Replacement register CRdy or CWProt bits are set to one (1). When the Changed bit is set, Pin 46 (-STSCHG) is held low if the SigChg bit is a One (1) and the CompactFlash card is configured for the I/O interface.

SigChg — This bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the CompactFlash card is configured for I/O

IOis8 — The host sets this bit to a one (1) if the CompactFlash card is to be configured in an 8-bit I/O Mode. The CompactFlash card is always configured for both 8- and 16-bit I/O, so this bit is ignored.

PwrDwn — This bit indicates whether the host requests the CompactFlash card to be in the power saving or active mode. When the bit is one (1), the CompactFlash card enters a power down mode. When zero (0), the host is requesting the CompactFlash card to enter the active mode. The PCMCIA Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The CompactFlash card automatically powers down when it is idle and powers back up when it receives a command.

Int — This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

2.4.4 Pin Replacement Register (Address 204H in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	Rdy/-Bsy	0
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	X

CRdy/-Bsy — This bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

CWProt — This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

Rdy/-Bsy — This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

MRdy/-Bsy — This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

X — This bit is ignored by the CompactFlash card.

TABLE 2-15: PIN REPLACEMENT CHANGED BIT/MASK BIT VALUES

Initial Value of (C) Status	Written by Host		Final "C" Bit	Comments
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

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2.4.5 Socket and Copy Register (Address 206H in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

SOCKET AND COPY REGISTER ORGANIZATION:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	Rdy/-Bsy	0
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	X

Reserved — This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive # — This bit indicates the drive number of the card for twin card configuration. Twin card configuration is currently not supported.

X — The socket number is ignored by the CompactFlash card.

2.5 I/O Transfer Function

2.5.1 I/O Function

The I/O transfer to or from the CompactFlash card can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash card. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash card, the system must generate a pair of 8-bit references to access the word's Even Byte and Odd Byte. The CompactFlash card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash card responds.

TABLE 2-16: I/O FUNCTION

Function Code	-REG	-CE2	-CE1	A_0	-IORD	-IOWR	D_{15}-D_8	D_7-D_0
Standby Mode	X	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Byte Input Access (8 bits)	V_{IL} V_{IL}	V_{IH} V_{IH}	V_{IL} V_{IL}	V_{IL} V_{IH}	V_{IL} V_{IL}	V_{IH} V_{IH}	High Z High Z	Even Byte Odd Byte
Byte Output Access (8 bits)	V_{IL} V_{IL}	V_{IH} V_{IH}	V_{IL} V_{IL}	V_{IL} V_{IH}	V_{IH} V_{IH}	V_{IL} V_{IL}	Don't Care Don't Care	Even Byte Odd Byte
Word Input Access (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Odd Byte	Even Byte
Word Output Access (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Odd Byte	Even Byte
I/O Read Inhibit	V_{IH}	X	X	X	V_{IL}	V_{IH}	Don't Care	Don't Care
I/O Write Inhibit	V_{IH}	X	X	X	V_{IH}	V_{IL}	High Z	High Z
High Byte Input Only (8 bits)	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	Odd Byte	High Z
High Byte Output Only (8 bits)	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	Odd Byte	Don't Care

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2.6 Common Memory Transfer Function

2.6.1 Common Memory Function

The Common Memory Transfer to or from the CompactFlash card can be either 8 or 16 bits.
The CompactFlash card permits both 8 and 16 bit accesses to all of its Common Memory addresses.

TABLE 2-17: COMMON MEMORY FUNCTION

Function Code	-REG	-CE2	-CE1	A_0	-OE	-WE	D_{15}-D_8	D_7-D_0
Standby Mode	X	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Byte Read Access (8 bits)	V_{IH} V_{IH}	V_{IH} V_{IH}	V_{IL} V_{IL}	V_{IL} V_{IH}	V_{IL} V_{IL}	V_{IH} V_{IH}	High Z High Z	Even Byte Odd Byte
Byte-Write Access (8 bits)	V_{IH} V_{IH}	V_{IH} V_{IH}	V_{IL} V_{IL}	V_{IL} V_{IH}	V_{IH} V_{IH}	V_{IL} V_{IL}	Don't Care Don't Care	Even Byte Odd Byte
Word Read Access (16 bits)	V_{IH}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Odd Byte	Even Byte
Word-Write Access (16 bits)	V_{IH}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	Odd Byte	Even Byte
Odd Byte Read Only (8 bits)	V_{IH}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	Odd Byte	High Z
Odd Byte-Write Only (8 bits)	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	Odd Byte	Don't Care

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2.7 True IDE Mode I/O Transfer Function

2.7.1 True IDE Mode I/O Function

The CompactFlash card can be configured in a True IDE Mode of operation. The CompactFlash card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. In this True IDE Mode the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode no Memory or Attribute Registers are accessible to the host. CompactFlash cards permit 8 bit data accesses if the user issues a Set Feature Command to put the device in 8 bit Mode.

Note: Removing and reinserting the CompactFlash card while the host computer's power is on will reconfigure the CompactFlash to PC Card ATA mode from the original True IDE Mode. To configure the CompactFlash card in True IDE Mode, the 50-pin socket must be power cycled with the CompactFlash card inserted and -OE (output enable) asserted.

Table 2-18 defines the function of the operations for the True IDE Mode.

TABLE 2-18: TRUE IDE MODE I/O FUNCTION

Function Code	-CE2	-CE1	A_0-A_2	-IORD	-IOWR	D_{15}-D_8	D_7-D_0
Invalid Mode	V_{IL}	V_{IL}	X	X	X	High Z	High Z
Standby Mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	Don't Care	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	Odd Byte In	Even Byte In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Odd Byte Out	Even Byte Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	Don't Care	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out
Drive Address	V_{IL}	V_{IH}	7H	V_{IL}	V_{IH}	High Z	Data Out

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3.0 SOFTWARE INTERFACE

3.1 CF-ATA Drive Register Set Definition and Protocol

The CompactFlash card can be configured as a high performance I/O device through:

1. Standard PC-AT disk I/O address spaces 1F0H-1F7H, 3F6H-3F7H (primary); 170H-177H, 376H-377H (secondary) with IRQ 14 (or other available IRQ).
2. Any system decoded 16 Byte I/O block using any available IRQ.
3. Memory space.

The communication to or from the CompactFlash card is done using the Task File registers which provide all the necessary registers for control and status information. The PCMCIA interface connects peripherals to the host using four register mapping methods. The following is a detailed description of these methods:

TABLE 3-1: I/O CONFIGURATIONS

Standard Configurations			
Config Index	**I/O or Memory**	**Address**	**Description**
0	Memory	0H-FH, 400H-7FFH	Memory Mapped
1	I/O	XX0H-XXFH	I/O Mapped 16 Contiguous Registers
2	I/O	1F0H-1F7H, 3F6H-3F7H	Primary I/O Mapped
3	I/O	170H-177H, 376H-377H	Secondary I/O Mapped

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3.1.1 I/O Primary and Secondary Address Configurations

TABLE 3-2: PRIMARY AND SECONDARY I/O DECODING

-REG	A_9-A_4	A_3	A_2	A_1	A_0	-IORD=0	-IOWR=0	Note
0	1F(17)H	0	0	0	0	Even RD Data	Even WR Data	1,2
0	1F(17)H	0	0	0	1	Error Register	Features	1,2
0	1F(17)H	0	0	1	0	Sector Count	Sector Count	
0	1F(17)H	0	0	1	1	Sector No.	Sector No.	
0	1F(17)H	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)H	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)H	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)H	0	1	1	1	Status	Command	
0	3F(37)H	0	1	1	0	Alt Status	Device Control	
0	3F(37)H	0	1	1	1	Drive Address	Reserved	

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1. Register 0 is accessed with -CE1 low and -CE2 low (and A_0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D_{15}-D_0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers which lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the Even Byte of the word and the second byte accessed is the Odd Byte of the equivalent word access.
2. A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

Note: Address lines which are not indicated are ignored by the CompactFlash card for accessing all the registers in this table.

3.1.2 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CompactFlash card, the registers are accessed in the block of I/O space decoded by the system as follows:

TABLE 3-3: CONTIGUOUS I/O DECODING

-REG	A_3	A_2	A_1	A_0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

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1. Register 0 is accessed with -CE1 low and -CE2 low (and A_0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the Even Byte of the word and the second byte accessed is the Odd Byte of the equivalent word access. A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9, and D are non-overlapping duplicates of the registers at offset 0 and 1.
   Register 8 is equivalent to register 0, while register 9 accesses the Odd Byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred Odd Byte then Even Byte.

   Repeated byte accesses to register 8 or 0 will access consecutive (Even then Odd) Bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (Even then Odd) Bytes from the data buffer. Byte accesses to register 9 access only the Odd Byte of the data.

Note: Address lines which are not indicated are ignored by the CompactFlash card for accessing all the registers in this table.

3.1.3 Memory Mapped Addressing

When the CompactFlash card registers are accessed via memory references, the registers appear in the common memory space window: 0-2 KByte as follows:

TABLE 3-4: MEMORY MAPPED DECODING

-REG	A_{10}	A_9-A_4	A_3	A_2	A_1	A_0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1,2
1	0	X	0	0	0	1	1	Error	Features	1,2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

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1. Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the Even Byte of the word and the second byte accessed is the Odd Byte of the equivalent word access.
   A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
   Register 8 is equivalent to register 0, while register 9 accesses the Odd Byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred Odd Byte then Even Byte.

   Repeated byte accesses to register 8 or 0 will access consecutive (Even then Odd) Bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (Even then Odd) Bytes from the data buffer. Byte accesses to register 9 access only the Odd Byte of the data.

3. Accesses to even addresses between 400H and 7FFH access register 8. Accesses to odd addresses between 400H and 7FFH access register 9. This 1 KByte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.

   Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

   Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the CompactFlash card.

   A word access to address at offset 8 will provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high-order byte of the data bus.

3.1.4 True IDE Mode Addressing

When the CompactFlash Card is configured in the True IDE Mode, the I/O decoding is as follows:

TABLE 3-5: TRUE IDE MODE I/O DECODING

-CE2	-CE1	A_2	A_1	A_0	-IORD=0	-IOWR=0
1	0	0	0	0	RD Data	WR Data
1	0	0	0	1	Error Register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control
0	1	1	1	1	Drive Address	Reserved

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3.1.5 CF-ATA Registers

The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the “task file.”

Note: In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted) and an I/O cycle is being performed.

3.1.5.1 Data Register (Address - 1F0H[170H];Offset 0,8,9)

The Data Register is a 16 bit register, and it is used to transfer data blocks between the CompactFlash card data buffer and the Host. This register overlaps the Error Register. The table below describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

Note: Because of the overlapped registers, access to the 1F1H, 171H or offset 1 are not defined for word (-CE2=0 and -CE1=0) operations. These accesses are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and DH have no restrictions on the operations that can be performed by the socket.

Data Register	CE2-	CE1-	A_0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	D_{15}-D_0
Even Data Register	1	0	0	0,8	D_7-D_0
Odd Data Register	1	0	1	9	D_7-D_0
Odd Data Register	0	1	X	8,9	D_{15}-D_8
Error / Feature Register	1	0	1	1, DH	D_7-D_0
Error / Feature Register	0	1	X	1	D_{15}-D_8
Error / Feature Register	0	0	X	DH	D_{15}-D_8

3.1.5.2 Error Register (Address - 1F1H[171H]; Offset 1, 0DH Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -CE2 low and -CE1 high.

Bit 7 (BBK) This bit is set when a Bad Block is detected.

Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.

Bit 5 This bit is 0.

Bit 4 (IDNF) The requested sector ID is in error or cannot be found.

Bit 3 This bit is 0.

Bit 2 (Abort) This bit is set if the command has been aborted because of a CompactFlash card status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

Bit 1 This bit is 0.

Bit 0 (AMNF) This bit is set in case of a general error.

3.1.5.3 Feature Register (Address - 1F1H[171H]; Offset 1, 0DH Write Only)

This register provides information regarding features of the CompactFlash card that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high.

3.1.5.4 Sector Count Register (Address - 1F2H[172H]; Offset 2)

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

3.1.5.5 Sector Number (LBA 7-0) Register (Address - 1F3H[173H]; Offset 3)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash card data access for the subsequent command.

3.1.5.6 Cylinder Low (LBA 15-8) Register (Address - 1F4H[174H]; Offset 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of then Logical Block Address.

3.1.5.7 Cylinder High (LBA 23-16) Register (Address - 1F5H[175H]; Offset 5)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -CE2 low and -CE1 high.

3.1.5.8 Drive/Head (LBA 27-24) Register (Address 1F6H[176H]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.

Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

LBA7-LBA0: Sector Number Register D7-D0.

LBA15-LBA8: Cylinder Low Register D7-D0.

LBA23-LBA16: Cylinder High Register D7-D0.

LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5 This bit is set to 1.

Bit 4 (DRV) DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. The CompactFlash card is set to be Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.

Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

3.1.5.9 Status & Alternate Status Registers (Address 1F7H[177H]&3F6H[376H]; Offsets 7 & E)

These registers return the CompactFlash card status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the CompactFlash card has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing CompactFlash card operations. This bit is cleared at power up and remains cleared until the CompactFlash card is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the CompactFlash card is ready.

Bit 3 (DRQ) The Data Request is set when the CompactFlash card requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is recommended that media access commands such as Read Sectors and Write Sectors) that end with an error condition should have the address of the first sector in error in the command block registers.

3.1.5.10 Device Control Register (Address - 3F6H[376H]; Offset E)

This register is used to control the CompactFlash card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is an X (don't care).

Bit 6 This bit is an X (don't care).

Bit 5 This bit is an X (don't care).

Bit 4 This bit is an X (don't care).

Bit 3 This bit is ignored by the CompactFlash card.

Bit 2 (SW Rst) This bit is set to 1 in order to force the CompactFlash card to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration Registers (4.3.2 to 4.3.5) as a hardware Reset does. The Card remains in Reset until this bit is reset to '0.'

Bit1(-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the CompactFlash card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.

Bit0 This bit is ignored by the CompactFlash card.

3.1.5.11 Card (Drive) Address Register (Address3F7H[377H]; Offset F)

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is don't care.

Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the CompactFlash card. Following are some possible solutions to this problem for the PCMCIA implementation:

1. Locate the CompactFlash card at a non-conflicting address, i.e. Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses.

2. Do not install a Floppy and a CompactFlash card in the system at the same time.

3. Implement a socket adapter which can be programmed to (conditionally) tri-state D7 of I/0 address 3F7H/377H when a CompactFlash card is installed and conversely to tri-state D6- D0 of I/O address 3F7H/377H when a floppy controller is installed.

4. Do not use the CompactFlash Card's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0H-1F7H, 3F6H (or 170H-177H, 176H) to the CompactFlash card or b) if provided use an additional Primary/Secondary configuration in the CompactFlash card which does not respond to accesses to I/O locations 3F7H and 377H. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.

Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.

Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

3.2 CF-ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the CompactFlash cards. Commands are issued to the CompactFlash card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 3-6) of command acceptance, all dependent on the host not issuing commands unless the CompactFlash card is not busy (BSY=0).

3.2.1 CF-ATA Command Set

Table 3-6 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

TABLE 3-6: CF-ATA COMMAND SET

Class	Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
1	Check Power Mode	E5H or 98H	-	-	-	-	D	-
1	Execute Drive Diagnostic	90H	-	-	-	-	D	-
1	Erase Sector(s)	C0H	-	Y[7]	Y	Y	Y[8]	Y
2	Format Track	50H	-	Y	-	Y	Y	Y
1	Identify Drive	ECH	-	-	-	-	D	-
1	Idle	E3H or 97H	-	Y	-	-	D	-
1	Idle Immediate	E1H or 95H	-	-	-	-	D	-
1	Initialize Drive Parameters	91H	-	Y	-	-	Y	-
1	Read Buffer	E4H	-	-	-	-	D	-
1	Read Long Sector	22H or 23H	-	-	Y	Y	Y	Y
1	Read Multiple	C4H	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
1	Recalibrate	1XH	-	-	-	-	D	-
1	Request Sense	03H	-	-	-	-	D	-
1	Seek	7XH	-	-	Y	Y	Y	Y
1	Set Features	EFH	Y	-	-	-	D	-
1	Set Multiple Mode	C6H	-	Y	-	-	D	-
1	Set Sleep Mode	E6H or 99H	-	-	-	-	D	-
1	Stand By	E2H or 96H	-	-	-	-	D	-
1	Stand By Immediate	E0H or 94H	-	-	-	-	D	-
1	Translate Sector	87H	-	Y	Y	Y	Y	Y
1	Wear Level	F5H	-	-	-	-	Y	-
2	Write Buffer	E8H	-	-	-	-	D	-
2	Write Long Sector	32H or 33H	-	-	Y	Y	Y	Y
3	Write Multiple	C5H	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDH	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38H	-	Y	Y	Y	Y	Y
3	Write Verify	3CH	-	Y	Y	Y	Y	Y

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1. FR = Features Register
2. SC = Sector Count Register
3. SN = Sector Number Register
4. CY = Cylinder Registers
5. DH = Card/Drive/Head Register
6. LBA = Logical Block Address Mode Supported (see command descriptions for use).
7. Y = The register contains a valid parameter for this command.
8. For the Drive/Head Register: Y means both the CompactFlash card and head parameters are used;
   D - only the CompactFlash card parameter is valid and not the head parameter.

3.2.1.1 Check Power Mode - 98H or E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E5H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode.

Because SST CompactFlash card can recover from sleep in 200ms, idle mode is never enabled.

CompactFlash card sets BSY, sets the Sector Count Register to 00H, clears BSY and generates an interrupt.

3.2.1.2 Execute Drive Diagnostic - 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command performs the internal diagnostic tests implemented by the CompactFlash card.

If in PCMCIA configuration this command runs only on the CompactFlash card which is addressed by the Drive/Head register when the diagnostic command is issued. This is because PCMCIA card interface does not allows for direct inter-drive communication (such as the ATA PDIAG and DASP signals). If in True IDE Mode the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown in Table 3-7 are returned in the Error Register at the end of the command.

TABLE 3-7: DIAGNOSTIC CODES

Code	Error Type
01H	No Error Detected
02H	Formatter Device Error
03H	Sector Buffer Error
04H	ECC Circuitry Error
05H	Controlling Microprocessor Error
8XH	Slave Error in True IDE Mode

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3.2.1.3 Erase Sector(s) - C0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

3.2.1.4 Format Track - 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFH or 00H). To remain host backward compatible, the CompactFlash card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

3.2.1.5 Identify Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify Drive command enables the host to receive parameter information from the CompactFlash card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 3-8. All reserved bits or words are zero. Table 3-8 is the definition for each field in the Identify Drive Information.

TABLE 3-8: IDENTIFY DRIVE INFORMATION

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848AH	2	General configuration bit-significant information
1	XXXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	XXXXH	2	Number of unformatted bytes per track
5	XXXXH	2	Number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7-8	XXXXH	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000H	2	Vendor Unique
10-19	aaaa	20	Serial number in ASCII. Big Endian Byte Order in Word
20	0002H	2	Buffer type
21	XXXXH	2	Buffer size in 512 Byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII. Big Endian Byte Order in Word
47	000XH	2	Maximum number of sectors on Read/Write Multiple command
48	0000H	2	Reserved
49	0200H	2	Capabilities
50	0000H	2	Reserved
51	0X00H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	000XH	2	Translation parameters are valid
54	XXXXH	2	Current numbers of cylinders
55	XXXXH	2	Current numbers of heads
56	XXXXH	2	Current sectors per track
57-58	XXXXH	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010XH	2	Multiple sector setting
60-61	XXXXH	4	Total number of sectors addressable in LBA Mode
62-63	0000H	4	Reserved (DMA data transfer is not supported in CompactFlash)
64	00XXH	2	Advanced PIO Transfer Mode Supported
65-66	0000H	4	Reserved
67	XXXXH	2	Minimum PIO transfer cycle time without flow control
68	XXXXH	2	Minimum PIO transfer cycle time with IORDY flow control
69-127	0000H	138	Reserved
128-159	0000H	64	Vendor unique bytes
160-255	0000H	192	Reserved

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3.2.1.5.1 General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

3.2.1.5.2 Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

3.2.1.5.3 Default Number of Heads

This field contains the number of translated heads in the default translation mode.

3.2.1.5.4 Number of Unformatted Bytes per Track

This field contains the number of unformatted bytes per translated track in the default translation mode.

3.2.1.5.5 Number of Unformatted Bytes per Sector

This field contains the number of unformatted bytes per sector in the default translation mode.

3.2.1.5.6 Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

3.2.1.5.7 Number of Sectors per Card

This field contains the number of sectors per CompactFlash card. This double word value is also the first invalid address in LBA translation mode.

3.2.1.5.8 Memory Card Serial Number

The contents of this field are right justified and padded with spaces (20H).

3.2.1.5.9 Buffer Type

This field defines the buffer capability:

0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the CompactFlash card.

3.2.1.5.10 Buffer Size

This field defines the buffer capacity in 512 Byte increments. SST's CompactFlash card has up to 8 sector data buffer for host interface.

3.2.1.5.11 ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands.

3.2.1.5.12 Firmware Revision

This field contains the revision of the firmware for this product.

3.2.1.5.13 Model Number

This field contains the model number for this product and is left justified and padded with spaces (20H).

3.2.1.5.14 Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands. SST's CompactFlash card can support up to 2 sectors for Read Multiple or Write Multiple Commands.

3.2.1.5.15 Capabilities

Bit 13: Standby Timer	Set to 0, forces sleep mode when host is inactive.
Bit 11: IORDY Support	Set to 0, indicates that this device may support IORDY operation.
Bit 9: LBA support	Set to 1, SST's CompactFlash supports LBA mode addressing.
Bit 8: DMA Support	This bit is set to 0. DMA mode is not supported.

3.2.1.5.16 PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer.

3.2.1.5.17 Translation Parameters Valid

If bit 0 is 1, it indicates that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 is 1, it indicates that words 64 to 70 are valid to support PIO Mode-4.

3.2.1.5.18 Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

3.2.1.5.19 Current Capacity

This field contains the product of the current cylinders times heads times sectors.

3.2.1.5.20 Multiple Sector Setting

This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for R/W Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that R/W Multiple commands are not valid.

3.2.1.5.21 Advanced PIO Data Transfer Mode

CompactFlash supports up to PIO Mode-4.

3.2.1.5.22 Minimum PIO Transfer Cycle Time Without Flow Control

The CompactFlash minimum cycle time is 120 ns.

3.2.1.5.23 Minimum PIO Transfer Cycle Time With IORDY

The CompactFlash minimum cycle time is 120 ns, e.g., PIO Mode-4.

3.2.1.5.24 Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the CompactFlash card in LBA mode only.

3.2.1.6 Idle - 97H or E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the CompactFlash card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

3.2.1.7 Idle Immediate - 95H or E1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95H or E1H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the CompactFlash card to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

3.2.1.8 Initialize Drive Parameters - 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

3.2.1.9 Read Buffer - E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Buffer command enables the host to read the current contents of the CompactFlash Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

3.2.1.10 Read Multiple - C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the SST CompactFlash card can support up to a block count of 1 as indicated in the Identify Drive Command information.

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = remainder(sector count/block count)

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

3.2.1.11 Read Long Sector - 22H or 23H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22H or 23H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 Bytes of data instead of 512 Bytes. During a Read Long command, the CompactFlash card does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 Bytes of data transferred in Word-Mode followed by 4 Bytes of ECC data transferred in Byte-Mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

3.2.1.12 Read Sector(s) - 20H or 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H or 21H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the CompactFlash card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

3.2.1.13 Read Verify Sector(s) - 40H or 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash card sets BSY.

When the requested sectors have been verified, the CompactFlash card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

3.2.1.14 Recalibrate - 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the CompactFlash card and is provided for compatibility purposes.

3.2.1.15 Request Sense - 03H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03H							
C/D/H (6)	1	X	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests extended error information for the previous command. Table 3-9 defines the valid extended error codes for the CompactFlash card Series product. The extended error code is returned to the host in the Error Register.

TABLE 3-9: EXTENDED ERROR CODES

Extended Error Code	Description
00H	No Error Detected
01H	Self Test OK (No Error)
09H	Miscellaneous Error
20H	Invalid Command
21H	Invalid Address (Requested Head or Sector Invalid)
2FH	Address Overflow (Address Too Large)
35H, 36H	Supply or generated Voltage Out of Tolerance
11H	Uncorrectable ECC Error
18H	Corrected ECC Error
05H, 30-34H, 37H, 3EH	Self Test or Diagnostic Failed
10H, 14H	ID Not Found
3AH	Spare Sectors Exhausted
1FH	Data Transfer Error / Aborted Command
0CH, 38H, 3BH, 3CH, 3FH	Corrupted Media Format
03H	Write / Erase Failed

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3.2.1.16 Seek - 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the CompactFlash card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

3.2.1.17 Set Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)		X		Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 3-10 defines all features that are supported.

TABLE 3-10: FEATURES SUPPORTED

Feature	Operation
01H	Enable 8-bit data transfers.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
9AH	NOP- accepted for compatibility.
BBH	4 Bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

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Features 01H and 81H are used to enable and clear 8-bit data transfer modes in True IDE Mode. If the 01H feature command is issued all data transfers will occur on the low order D7-D0 data bus and the IOIS16 signal will not be asserted for data register accesses.

Features 55H and BBH are the default features for the CompactFlash card; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Features 66H and CCH can be used to enable and disable whether the Power On Reset (POR) Defaults will be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

3.2.1.18 Set Multiple Mode - C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the CompactFlash card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the CompactFlash card sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

3.2.1.19 Set Sleep Mode- 99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99H or E6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the CompactFlash card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

3.2.1.20 Standby - 96H or E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96H or E2H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the CompactFlash card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

3.2.1.21 Standby Immediate - 94H or E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94H or E0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the CompactFlash card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

3.2.1.22 Translate Sector - 87H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 Byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector. Table 3-11 represents the information in the buffer. Please note that this command is unique to the CompactFlash card.

TABLE 3-11: TRANSLATE SECTOR INFORMATION

Address	Information
00H-01H	Cylinder MSB (00), Cylinder LSB (01)
02H	Head
03H	Sector
04H-06H	LBA MSB (04) - LSB (06)
07H-12H	Reserved
13H	Erased Flag (FFH) = Erased; 00H = Not Erased
14H - 17H	Reserved
18H-1AH	Hot Count MSB (18) - LSB (1A)[1]
1BH-1FFH	Reserved

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1. A value of 0 indicates Hot Count is not supported.

3.2.1.23 Wear Level - F5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5H							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00H indicating Wear Level is not needed.

3.2.1.24 Write Buffer - E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

The Write Buffer command enables the host to overwrite contents of the CompactFlash Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 Bytes.

3.2.1.25 Write Long Sector - 32H or 33H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32H or 33H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is similar to the Write Sector(s) command except that it writes 516 Bytes instead of 512 Bytes. Only single sector Write Long operations are supported. The transfer consists of 512 Bytes of data transferred in Word-Mode followed by 4 Bytes of ECC transferred in Byte-Mode. Because of the unique nature of the solid-state CompactFlash card, the 4 Bytes of ECC transferred by the host may be used by the CompactFlash card. The CompactFlash card may discard these 4 Bytes and write the sector with valid ECC data. This command has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

3.2.1.26 Write Multiple Command - C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the SST CompactFlash card can support up to a block count of 1 as indicated in the Identify Drive Command information

This command is similar to the Write Sectors command. The CompactFlash card sets BSY within 400 ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = remainder(sector count/block count)

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

3.2.1.27 Write Multiple without Erase - CDH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDH							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued.

3.2.1.28 Write Sector(s) - 30H or 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H or 31H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash card sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

3.2.1.29 Write Sector(s) without Erase - 38H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the CompactFlash card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

3.2.1.30 Write Verify - 3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command.

3.2.2 Error Posting

The following table summarizes the valid status and error value for all the CF-ATA Command set.

TABLE 3-12: ERROR AND STATUS REGISTER

	Error Register					Status Register				
Command	**BBK**	**UNC**	**IDNF**	**ABRT**	**AMNF**	**DRDY**	**DWF**	**DSC**	**CORR**	**ERR**
Check Power Mode				V		V	V	V		V
Execute Drive Diagnostic[1]						V		V		V
Erase Sector(s)	V		V	V	V	V	V	V		V
Format Track			V	V	V	V	V	V		V
Identify Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Drive Parameters						V		V		V
Read Buffer				V		V	V	V		V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request Sense				V		V		V		V
Seek			V	V		V	V	V		V
Set Features				V		V	V	V		V
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Stand By				V		V	V	V		V
Stand By Immediate				V		V	V	V		V
Translate Sector	V		V	V	V	V	V	V		V
Wear Level	V	V	V	V	V	V	V	V		V
Write Buffer				V		V	V	V		V
Write Long Sector	V		V	V	V	V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V
Write Multiple w/o Erase	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Sector(s) w/o Erase	V		V	V	V	V	V	V		V
Write Verify	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

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1. See Table 3-7

Note: V = valid on this command

Data Sheet

4.0 APPENDIX

4.1 Differences between CF-ATA and PC Card-ATA/True IDE

This section details differences between CF-ATA vs. PC Card ATA and the differences between CF-ATA vs. True IDE.

4.1.1 Electrical Differences

4.1.1.1 TTL Compatibility

CF is not TTL compatible, it is a purely CMOS interface. Refer to section 2.3.2 of this specification.

4.1.1.2 Pull Up Resistor Input Leakage Current

The minimum pull up resistor input leakage current is 50K ohms rather than the 10K ohms stated in the PCMCIA specification.

4.1.2 Functional Differences

4.1.2.1 Additional Set Features Codes in CF-ATA

The following Set Features codes are not PC Card ATA or True IDE, but provide additional functionality in CF-ATA.

- 69H, Accepted for backward compatibility
- 96H, Accepted for backward compatibility
- 97H, Accepted for backward compatibility
- 9AH, Set the host current source capability

4.1.2.2 Additional Commands in CF-ATA

The following commands are not standard PC Card ATA commands, but provide additional functionality in CF-ATA.

The command codes for the commands below are defined as vendor unique in PC Card ATA/True IDE.

- C0H, Erase Sectors
- 87H, Translate Sector
- F5H, Wear Level

The command codes for the commands below are defined as reserved in PC Card ATA/True IDE:

- 03H, Request Sense
- 38H, Write Without Erase
- CDH, Write Multiple Without Erase

4.1.2.3 Idle Timer

The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in PC Card ATA/True IDE.

4.1.2.4 Recovery from Sleep Mode

For CF devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.

5.0 PHYSICAL DIMENSIONS

TABLE 5-1: TYPE I COMPACTFLASH STORAGE CARD PHYSICAL SPECIFICATIONS

Length:	36.4 ± 0.15 mm (1.433 ±.006 in.)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in.)
Thickness: (Including Label Area)	3.3 mm ± 0.10 mm (.130 ± .004in.)

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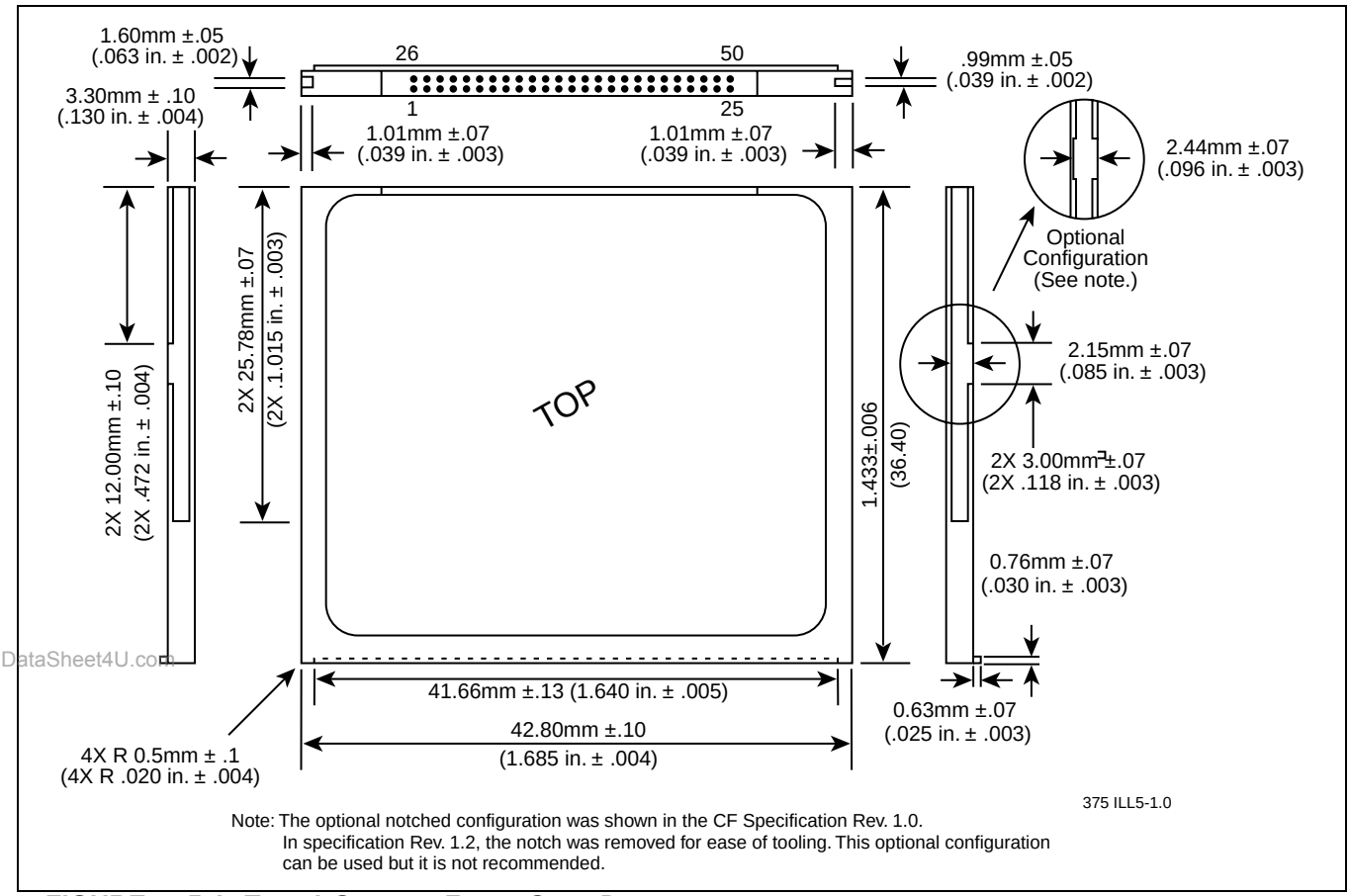
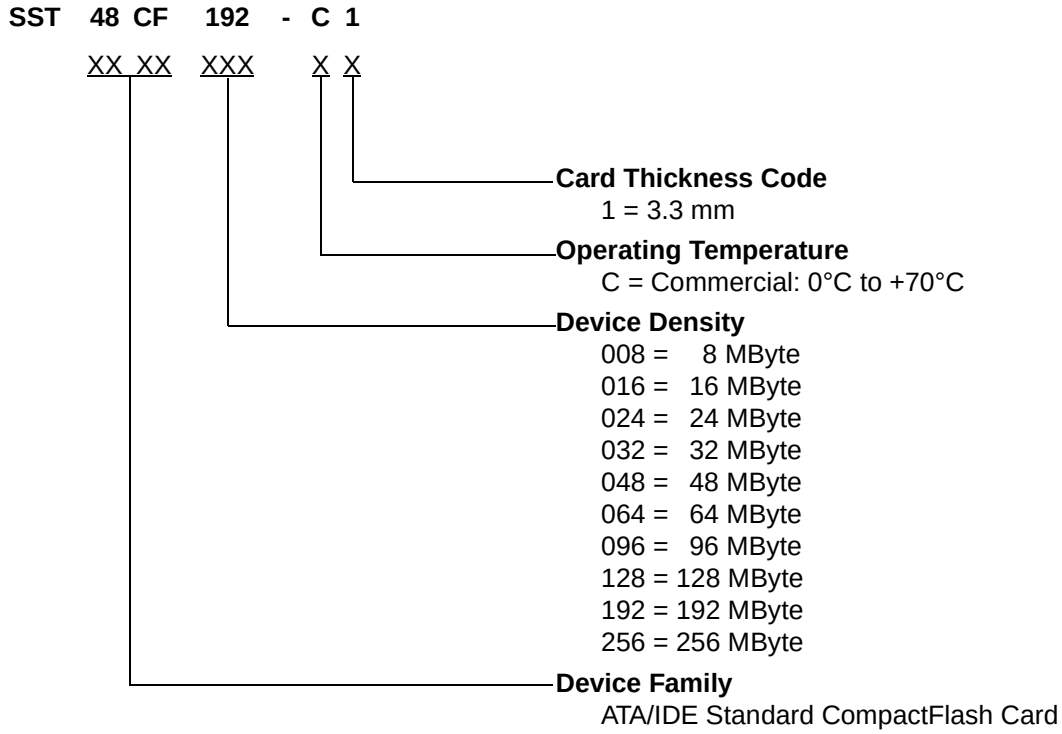


Note: The optional notched configuration was shown in the CF Specification Rev. 1.0.
In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

FIGURE 5-1: TYPE 1 COMPACTFLASH CARD DIMENSIONS

6.0 PRODUCT ORDERING INFORMATION



6.1 Valid combinations

SST48CF008-C1

SST48CF016-C1
SST48CF024-C1
SST48CF032-C1
SST48CF048-C1
SST48CF064-C1
SST48CF096-C1
SST48CF128-C1
SST48CF192-C1
SST48CF256-C1

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

7.0 LIMITED WARRANTY

SST warrants all products against non-conformances in materials and workmanship for a period of one year from the delivery date of subject products. SST's liability is limited to replacing or repairing the product if it has been paid for. SST's warranties will not be affected by rendering of technical advice in connection with the order of products furnished hereunder. Except as expressly provided above, SST makes no warranties, express or implied, including without limitation any warranty of merchantability or fitness for a particular purpose. In no event shall SST be liable for any incidental or consequential damages with respect to the products purchased hereunder. SST reserves the right to discontinue production or change specifications or change prices at any time and without notice.

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7.1 Life Support Policy

SST's products are not authorized for use as critical component in life support devices or systems. Life support devices or systems are devices or systems that, (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, or the affect its safety or effectiveness.

8.0 PATENT PROTECTION

SST products are protected by assigned U.S. and foreign patents.

9.0 PCMCIA STANDARD

CompactFlash memory cards are fully electrically compatible with the PCMCIA specifications listed below. These specifications may be obtained from:

PCMCIA
2635 North First St. Ste. 209
San Jose, CA 95131 USA

Phone: 408-433-2273
Fax: 408-433-9558

1. PCMCIA PC Card Standard, March 1997
2. PCMCIA PC Card ATA Specification, March 1997

10.0 COMPACTFLASH SPECIFICATION

CompactFlash memory Cards are fully compatible with the CompactFlash Specification published by the CompactFlash Association. Contact the CompactFlash Association for more information.

CompactFlash Association
P.O. Box 51537
Palo Alto, CA 94303 USA

Phone: 415-843-1220
Fax: 415-493-1871
www.compactflash.org

11.0 RELATED DOCUMENTS

American National Standard X3.221 AT Attachment for Interface for Disk Drives Document

This document can be ordered from Global Engineering Documents by calling: 1-800-854-7179