TOYOCOM

Crystal Clock Oscillator

TFG-756DVX7

FULL DIP Double-Sealed VCXO

Features

- CMOS logic output
- DIP-14 pin package compatible
- Hermetically double-sealed metal package
- Voltage controlled oscillator

Absolute Maximum Ratings

Parameter	Symbol	Rating
Supply voltage	V_{CC}	-0.5 to +7.0 V
Input voltage	V_{IN}	-0.5 to V_{CC}+0.5 V
Output voltage	V_O	-0.5 to V_{CC}+0.5 V
Output current	I_O	±20 mA
Storage temperature	T_{stg}	-40 to +85 °C

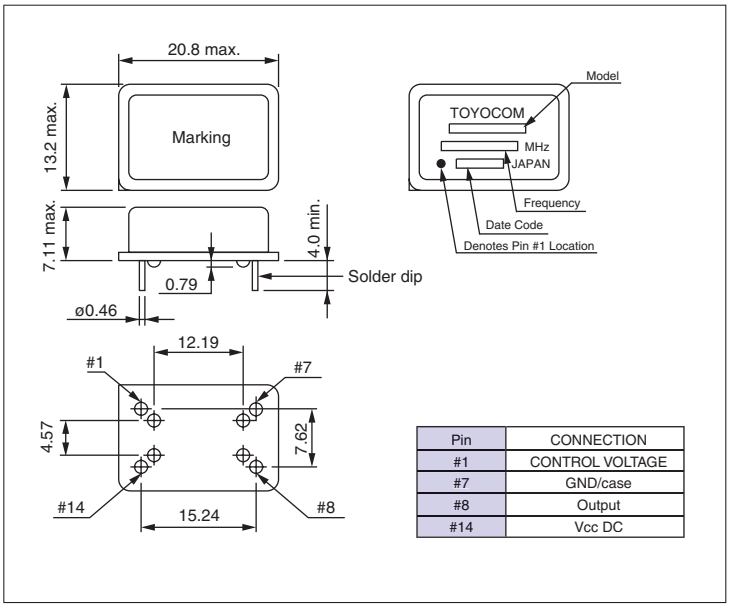
Specifications

Parameter		TFG-756DVX7	Conditions
Frequency	fo	40 to 100 MHz	
Frequency Stability	Δf/fo	±50 ppm max.	(*1)
Pullability		±150 ppm min.	at Vcont=0 to +5.0V, Ref=+2.5 V
Control Voltage Range	Vcont	+2.5 V ±2.5V	DC, Pin #1
Operating Temperature	Topr	0 °C to +70 °C	
Supply Voltage	Vcc	+5.0 V ±5%	DC, Pin #14
Supply Current	Icc	See Table A (max.)	Vcc=+5.25V
Output Voltage	V_{OH} V_{OL}	V_{OH}=Vcc-0.5 V min. / V_{OL}=+0.5 V max.	I_{OH}=-4mA Pin #8 I_{OL}=+4mA
Symmetry	SYM	40 to 60 %	at 50% Vcc
Rise/Fall time	tr/tf	See Table A (max.)	at 20% to 80% Vcc
Load Capacitance	C_L	30 pF max.	
Start-up time	tst	4 ms max.	

*1 Inclusive of calibration tolerance at +25°C, operating temperature, operating voltage range.

*2 Rise time (0 to +4.75V) of Vcc >150µs

Package Outlines [Dimensions in mm]



Pin	CONNECTION
#1	CONTROL VOLTAGE
#7	GND/case
#8	Output
#14	Vcc DC

Table A

Freq. (MHz)	40 ≤ fo fo ≤ 60	60 < fo fo ≤ 100
Icc (mA)	50	60
tr,tf (ns)	4	3

Test Circuit

See Test Circuit page TEST-7