

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13							

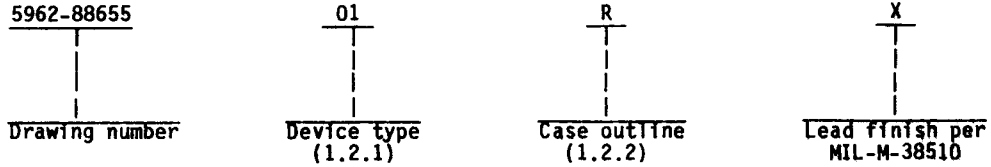
<p>PMIC N/A</p> <p>STANDARDIZED MILITARY DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p>AMSC N/A</p>	<p>PREPARED BY <i>Larry T. Gaudin</i></p> <p>CHECKED BY <i>Ray Monin</i></p> <p>APPROVED BY <i>[Signature]</i></p> <p>DRAWING APPROVAL DATE 30 MAY 1989</p> <p>REVISION LEVEL</p>	<p style="text-align: center;">DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</p> <p>MICROCIRCUIT, DIGITAL, FAST, CMOS, OCTAL D-TYPE, FLIP-FLOP, MONOLITHIC SILICON</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">SIZE A</td> <td style="width: 30%;">CAGE CODE 67268</td> <td style="width: 55%;">5962-88655</td> </tr> <tr> <td colspan="2" style="text-align: center;">SHEET 1 OF</td> <td style="text-align: center;">13</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-88655	SHEET 1 OF		13
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DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT534	Octal D-type flip-flops, with three-state outputs
02	54FCT534A	Octal D-type flip-flops, with three-state outputs

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range - - - - -	-0.5 V dc to +6.0 V dc
Input voltage range - - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
Output voltage range - - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC input diode current (I_{IK}) - - - - -	-20 mA
DC output diode current (I_{OK}) - - - - -	-50 mA
DC output current - - - - -	±100 mA
Maximum power dissipation (P_D) 2/ - - - - -	500 mW
Thermal resistance, junction-to-case (θ_{JC}) - - - - -	See MIL-M-38510, appendix C
Storage temperature range - - - - -	-65°C to +150°C
Junction temperature (T_J) - - - - -	+175°C
Lead temperature (soldering, 10 seconds) - - - - -	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) - - - - -	+4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL}) - - - - -	0.8 V dc
Minimum high level input voltage (V_{IH}) - - - - -	2.0 V dc
Case operating temperature range (T_C) - - - - -	-55°C to +125°C

1/ All voltages referenced to GND.

2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS} .

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 5.0 V _{dc} ±10% unless other specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, V _{IL} = 0.8 V, V _{IH} = 2.0 V	I _{OH} = -300 μA	1, 2, 3	A11	4.3	V
			I _{OH} = -12 mA	1, 2, 3	A11	2.4	V
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IL} = 0.8 V, V _{IH} = 2.0 V	I _{OL} = 300 μA	1, 2, 3	A11		0.2 V
			I _{OL} = 32 mA	1, 2, 3	A11		0.5 V
Input clamp voltage	V _{IK}	V _{CC} = 4.5 V, I _{IN} = -18 mA	1	A11		-1.2	V
High level input current	I _{IH}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	1, 2, 3	A11		5.0	μA
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _{IN} = GND	1, 2, 3	A11		-5.0	μA
High impedance output current	I _{OZH}	V _{CC} = 5.5 V, V _{OUT} = 5.5 V	1, 2, 3	A11		10	μA
Low impedance output current	I _{OZL}	V _{CC} = 5.5 V, V _{OUT} = GND	1, 2, 3	A11		-10	μA
Short circuit output current	I _{OS}	V _{CC} = 5.5 V <u>1/</u> V _{OUT} = 0.0 V	1, 2, 3	A11	-60		mA
Quiescent power supply current (CMOS inputs)	I _{CCQ}	V _{IN} ≤ 0.2 V or V _{IN} ≥ 5.3 V, V _{CC} = 5.5 V, f _I = f _{CP} = 0 MHz	1, 2, 3	A11		1.5	mA
Power supply current (TTL inputs high)	ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V <u>2/</u>	1, 2, 3	A11		2.0	mA
Dynamic power supply current	I _{CCD}	V _{CC} = 5.5 V, outputs open V _{IN} ≥ 5.3 V or V _{IN} ≤ 0.2 V, OE = GND one bit toggling: 50% duty cycle	<u>3/</u>	A11		0.4	mA/MHz
Total power supply current <u>4/</u>	I _{CC}	V _{IN} > 5.3 V or V _{IN} < 0.2 V, V _{CC} = 5.5 V, f _{CP} = 10 MHz, outputs open, one bit toggling: 50% duty cycle f _I = 5 MHz, OE = GND	1, 2, 3	A11		5.5	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 5.0 V dc ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Total power supply current 4/	I _{CC}	V _{IN} = 3.4 V or V _{IN} = GND, V _{CC} = 5.5 V, f _{CP} = 10 MHz, outputs open, one bit toggling: 50% duty cycle f _I = 5 MHz, OE = GND	1, 2, 3	A11		6.0	mA
Functional tests		See 4.3.1d	7, 8	A11			
Input capacitance	C _{IN}	See 4.3.1c	4	A11		10	pF
Output capacitance	C _{OUT}	See 4.3.1c	4	A11		12	pF
Propagation delay time, CP to On	t _{PLH} , t _{PHL}	V _{CC} = 5.0 V C _L = 50 pF R _L = 500Ω See figure 3	9, 10, 11	01	1.5	11.0	ns
				02	1.5	7.2	
Output enable time	t _{PZH} , t _{PZL}	See figure 3 5/	9,10,11	01	1.5	14.0	ns
				02	1.5	7.5	
Output disable time	t _{PHZ} , t _{PLZ}		9, 10, 11	01	1.5	8.0	ns
				02	1.5	6.5	
Setup time Dn to CP	t _s	V _{CC} = 5.0 V C _L = 50 pF R _L = 500Ω See figure 3	9, 10, 11	01	2.5		ns
				02	2.0		
Hold time Dn to CP	t _h		9, 10, 11	01	2.5		ns
				02	1.5		
CP pulse width (high or low)	t _{PW}		9, 10, 11	01	7.0		ns
				02	6.0		

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed one second.

2/ TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

$$4/ I_{CC} = I_{CCQ} + (\Delta I_{CC} \times D_H \times N_T) + (I_{CCD}(f_I \times N_I + f_{CP}/2))$$

where: D_H = Duty cycle for TTL inputs high
 N_T = Number of TTL inputs at D_H
 f_I = Input frequency in MHz
 N_I = Number of inputs at f_I
 f_{CP} = clock frequency in MHz

5/ The minimum limits are guaranteed, if not tested, to the limits specified in table I.

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Device type	01 and 02
Package	R, S and 2
Terminal number	Terminal symbol
1	OE
2	DO
3	D0
4	D1
5	O1
6	O2
7	D2
8	D3
9	O3
10	GND
11	CP
12	O4
13	D4
14	D5
15	O5
16	O6
17	D6
18	D7
19	O7
20	VCC

FIGURE 1. Terminal connections.

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Device types 01 and 02				
Function	Inputs			Outputs
	\overline{OE}	CP	D_n	\overline{O}_n
HI-Z	H	L	X	Z
	H	H	X	Z
Load Register	L		L	H
	L		H	L
	H		L	Z
	H		H	Z


H = High voltage level
 L = Low voltage level
 X = Irrelevant
 Z = High impedance state
 = Low-to-high transition

FIGURE 2. Truth table.

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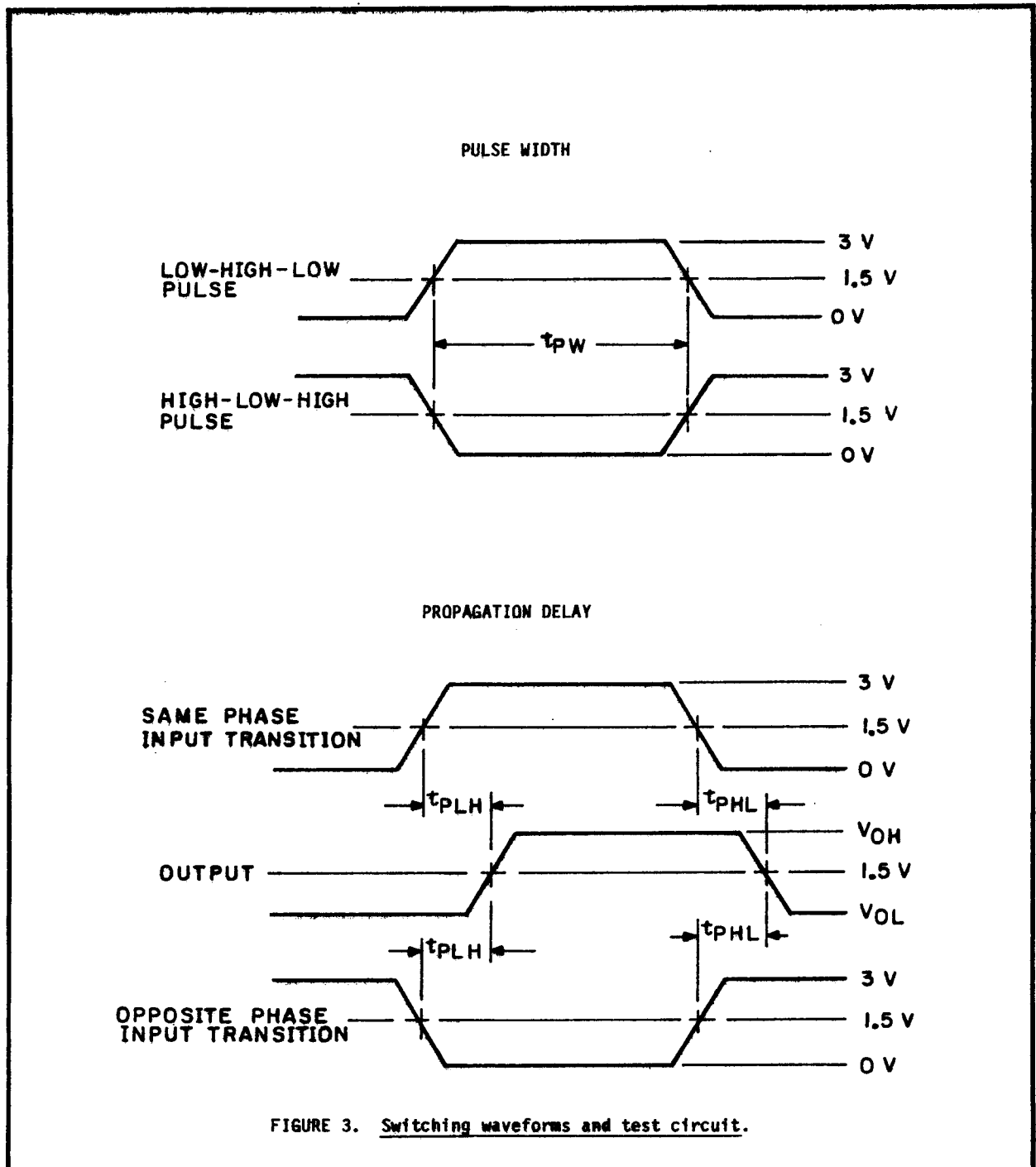


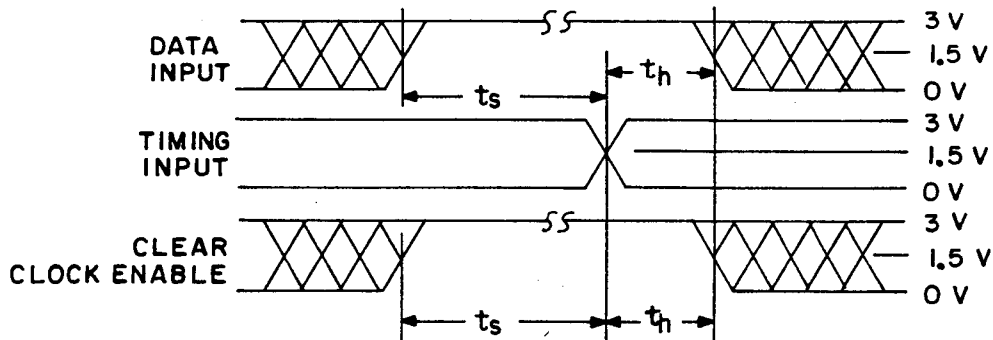
FIGURE 3. Switching waveforms and test circuit.

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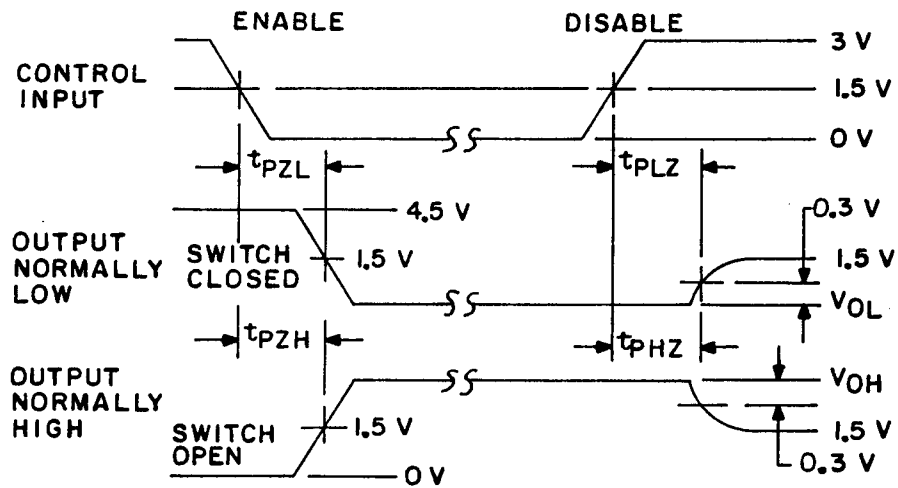
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SETUP AND HOLD TIMES



ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input control enable - low and input control disable - high.
2. Pulse generator for all pulses: $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

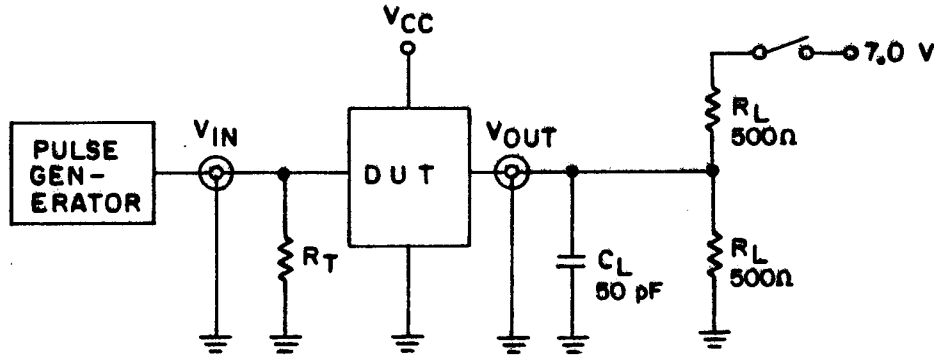
FIGURE 3. Switching waveforms and test circuit - Continued.

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TEST CIRCUITS FOR THREE-STATE OUTPUTS



Test	Switch
t_{PLZ}	Closed
t_{pZL}	Closed
All other	Open

NOTES:

- C_L includes probe and jig capacitance.
- R_T should be equal to Z_{out} of the pulse generator.
- Pulse generator for all pulses: $PRR \leq 1.0$ MHz; $Z_{out} \leq 50\Omega$,
 $t_r = t_f = 2.5$ ns.

FIGURE 3. Switching waveforms and test circuit - Continued.

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3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on five devices with zero failures.
- d. Subgroups 7 and 8 tests shall verify the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,4,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number ^{1/}
5962-8865501RX	61772 75569	IDT54FCT534DB P54PCT534DMB
5962-8865501SX	61772	IDT54FCT534EB
5962-88655012X	61772 75569	IDT54FCT534LB P54PCT534LMB
5962-8865502RX	61772 75569	IDT54FCT534ADB P54PCT534ADMB
5962-8865502SX	61772	IDT54FCT534AEB
5962-88655022X	61772 75569	IDT54FCT534ALB P54PCT534ALMB

^{1/} Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

Vendor name and address

61772

Integrated Device Technology
3236 Scott Boulevard
Santa Clara, CA 95052

75569

Performance Semiconductor Corporation
610 E. Weddle Drive
Sunnyvale, CA 94089

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