Austin Semiconductor, Inc.

SSRAM
AS5SS256K18

256K x 18 SSRAM
Synchronous Burst SRAM,
Flow-Through

FEATURES
- Fast access times: 8, 10, and 15ns
- Fast clock speed: 113, 100, and 66 MHz
- Fast clock and OE\ access times
- Single +3.3V +0.3V/-0.165V power supply (V_{DD})
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRTIE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Interally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down
- Low capacitive bus loading
- Operating Temperature Ranges:
  - Military -55°C to +125°C
  - Industrial -40°C to +85°C

OPTIONS — MARKING

- Timing
  - 7.5ns/8ns/113 MHz — -8*
  - 8.5ns/10ns/100 MHz — -9
  - 10ns/15ns/66 MHz — -10
- Packages
  - 100-pin TQFP — DQ No. 1001
- Operating Temperature Ranges:
  - Military -55°C to +125°C — IT
  - Industrial -45°C to +85°C — XT

**available as IT only.*

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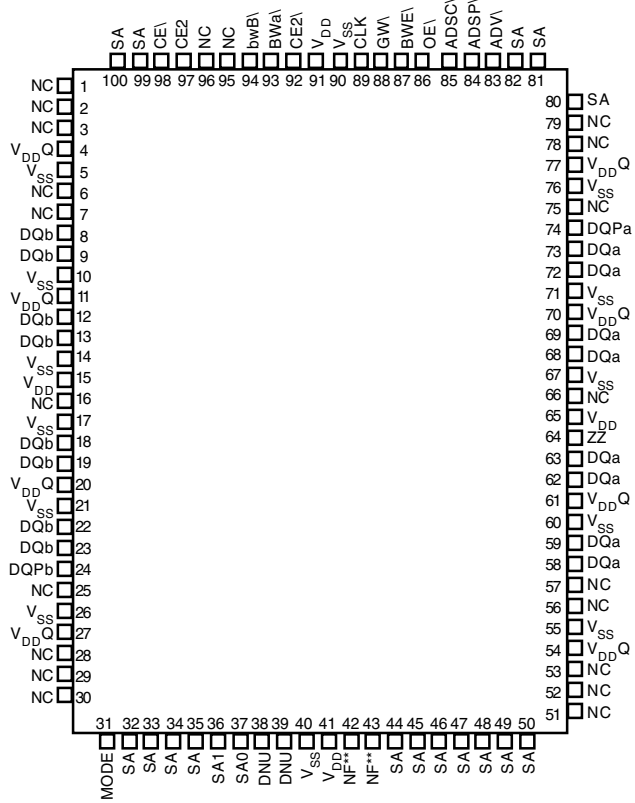
PIN ASSIGNMENT
(Top View)

100-pin TQFP



***pins 42,43 reserved for future address expansion for 8Mb, 16Mb densities.*

GENERAL DESCRIPTION

The Austin Semiconductor, Inc. Synchronous Burst SRAM family employs high-speed, low power CMOS designs that are fabricated using an advanced CMOS process.

ASI's 4Mb Synchronous Burst SRAMs integrate a 256K x 18, SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE\), two additional chip enables for easy depth expansion (CE2\, CE2), burst control inputs (ADSC\, ADSP\, ADV\), byte write enables (BWx\) and global write (GW\).

Asynchronous inputs include the output enable (OE\), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE\, is also asynchronous. WRITE cycles can be from one to two bytes wide, as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP\) or address status controller (ADSC\) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV\).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on this x18 device BWa\ controls DQa pins and DQPa; BWb\ controls DQb pins and DQPb. GW\ LOW causes all bytes to be written. Parity bits are available on this device.

ASI's 4Mb Synchronous Burst SRAMs operate from a +3.3V V_{DD} power supply, and all inputs and outputs are TTL-compatible. The device is ideally suited for 486, Pentium®, and PowerPC systems and those systems that benefit from a wide synchronous data bus.

PIN DESCRIPTIONS

PIN NUMBERS	SYM	TYPE	DESCRIPTION
37, 36, 32-35, 44-50, 80-82, 99, 100	SA0, SA1, SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94	BWa\ BWb\	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enables is LOW for a WRITE cycle and HIGH for a READ cycle. BWa\ controls DQa pins and DQPa; BWb\ controls DQb pins and DQPb.
87	BWE\	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
88	GW\	Input	Global Write: This active LOW input allows a full 18-bit WRITE to occur independent of the BWE\ and BWx\ lines and must meet the setup and hold times around the rising edge of CLK.
89	CLK	Input	Clock: This signal registers the addresses, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	CE\	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and Conditions the internal use of ADSP\. CE\ is sampled only when a new external address is loaded.
92	CE2\	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
86	OE\	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
83	ADV\	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during WRITE cycle, ADV\ must be HIGH at the rising edge of the first clock after an ADSP\ cycle is initiated.
84	ADSP\	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC\, but dependent upon CE\, CE2, and CE2\. ADSP\ is ignored if CE\ is HIGH. Power-down state is entered if CE2 if LOW or CE2\ is HIGH.
85	ADSC\	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE\ is LOW. ADSC\ is also used to place the chip into power-down state when CE\ is HIGH.
31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
(a) 58, 59, 62, 63, 68, 69, 72, 73 (b) 8, 9, 12,13, 18, 19, 22, 23	DQa DQb	Input/ Output	SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins. Input data must meet setup and hold times around the rising edge of CLK.
74, 24	NC/DQPa NC/DQPb	NC/ I/O	No Connect/Parity Data I/Os: Byte "a" is DQPa pins; Byte "b" is DQPb pins.
15, 41,65, 91	VDD	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	VDDQ	Supply	Isolated Output Buffer Supply: See DC Electrical Characterics and Operating Conditions for range.
5, 10, 14, 17, 21, 26, 40, 55, 60, 67 71, 76, 90	VSS	Supply	Ground: GND
38, 39	DNU	---	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1-3, 6, 7, 16,25, 28-30, 51-53, 56,57, 66, 75, 78, 79, 95, 96	NC	-----	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.
42, 43	NF		No Function: These pins are internally connected to the die and will have the capacitance of input pins. It is allowable to leave these pins unconnected or driven by signals.

INTERLEAVED BURST ADDRESS TABLE (MODE=NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X…X00	X…X01	X…X10	X…X11
X…X01	X…X00	X…X11	X…X10
X…X10	X…X11	X…X00	X…X01
X…X11	X…X10	X…X01	X…X00

LINEAR BURST ADDRESS TABLE (MODE=LOW)

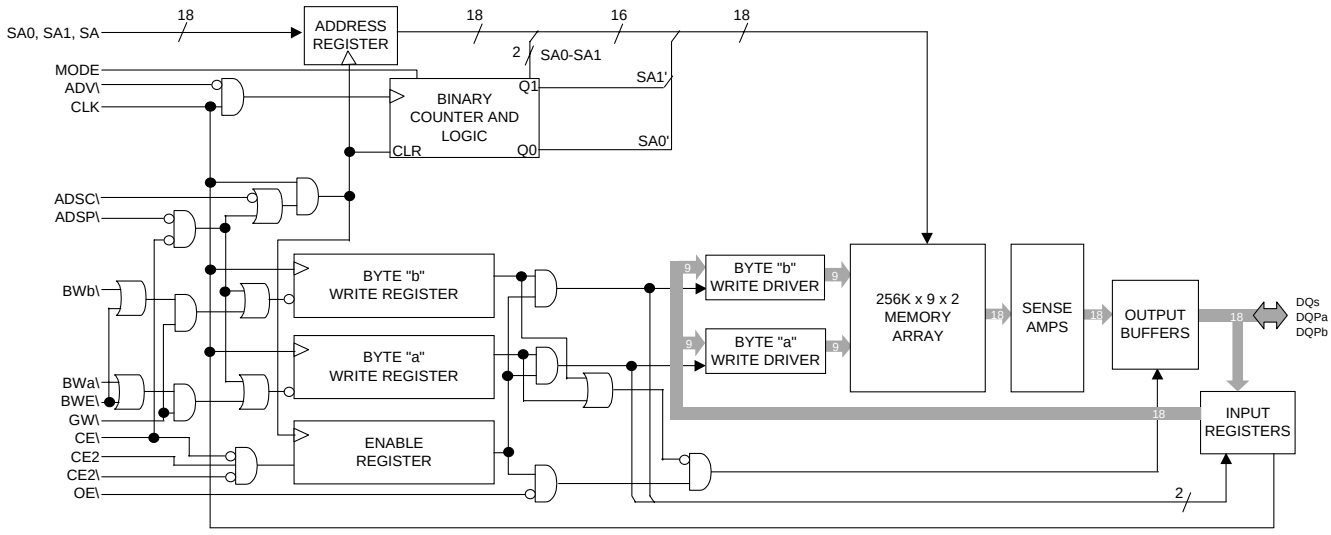
FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X…X00	X…X01	X…X10	X…X11
X…X01	X…X10	X…X11	X…X00
X…X10	X…X11	X…X00	X…X01
X…X11	X…X00	X…X01	X…X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS

FUNCTION	GW\	BWE\	BWa\	BWb\
READ	H	H	X	X
READ	H	L	H	H
WRITE Byte "a"	H	L	L	H
WRITE Byte "b"	H	L	H	L
WRITE All Bytes	H	L	L	L
WRITE All Bytes	L	X	X	X

NOTE: Using BWE\ and BWa\ through BWb\, any one or more bytes may be written.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

TRUTH TABLE

OPERATION	ADDRESS USED	CE\	CE2\	CE2	ZZ	ADSP\	ADSC\	ADV\	WRITE\	OE\	CLK	DQ
DESELECT Cycle, Power-Down	NONE	H	X	X	L	X	L	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	NONE	L	X	L	L	L	X	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	NONE	L	H	X	L	L	X	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	NONE	L	X	L	L	H	L	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	NONE	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-Down	NONE	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	EXTERNAL	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	EXTERNAL	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	EXTERNAL	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	EXTERNAL	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	EXTERNAL	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	NEXT	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	NEXT	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	NEXT	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	NEXT	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	NEXT	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	NEXT	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	CURRENT	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	CURRENT	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	CURRENT	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	CURRENT	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	CURRENT	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	CURRENT	H	X	X	L	X	H	H	L	X	L-H	D

NOTES:
1. X means "Don't Care." \ means active LOW. H means logic HIGH. L means logic LOW.
2. For WRITE\, L means any one or more byte write enable signals (BWa\, BWb\) and BWE\ are LOW or GW\ is LOW. WRITE\ = H for a ll BWx\, BWE\, GW\ HIGH.
3. BWa\ enables WRITEs to DQas and DQPa. BWb\ enables WRITEs to DQbs and DQPb.
4. All inputs except OE\ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, OE\ must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP\ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE\ LOW or GW\ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS}.....-0.5V to +4.6V
Voltage on $V_{DD}Q$ Supply Relative to V_{SS}.....-0.5V to +4.6V
Storage Temperature (plastic) .....-55°C to +125°C
Max Junction Temperature**.....+150°C
Short Circuit Output Current.....100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

($-55^oC \le T_A \le +125^oC$ and $-40^oC \le T_A \le +85^oC$; V_{DD} = +3.3V +0.3V/-0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{DD} +0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	($0V \le V_{IN} \le V_{DD}$)	IL_I	-2	2	µA	3
Output Leakage Current	Output(s) disabled; $0V \le V_{IN} \le V_{DD}$	IL_O	-2	2	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4	--	V	1, 4
Output Low Voltage	I_{OL} = 8.0 mA	V_{OL}	--	0.5	V	1, 4
Supply Voltage		V_{DD}	3.135	3.6	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	3.135	3.6	V	1, 5

CAPACITANCE

DESCRIPTION	CONDITIONS	SYM	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1MHz; V_{DD} = 3.3V	C_I	4	pF	6
Input/Output Capacitance (DQ)		C_O	5	pF	6
Address Capacitance		C_A	3.5	pF	6
Clock Capacitance		C_{CK}	3.5	pF	6

THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYM	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	θ_{JA}	46	°C/W	6
Thermal Resistance (Junction to Top of Case)		θ_{JC}	2.8	°C/W	6

NOTES:

1. All voltages referenced to VSS (GND)
2. Overshoot: $V_{IH} \le +4.6V$ for $t \le {}^tKC/2$ for $I \le 20mA$
   Undershoot: $V_{IL} \ge -0.7V$ for $t \le {}^tKC/2$ for $I \le 20mA$
   Power-up: $V_{IH} \le +3.6V$ and $V_{DD} < 3.135V$ for $t \le 200ms$
3. MODE pin has an internal pull-up, and input leakage = ±10µA.
4. The load used for V_{OH}, V_{OL} testing is shown in Figure 2 for 3.3V I/O. AC load current is higher then the stated DC values.
5. $V_{DD}Q$ should never exceed V_{DD}. V_{DD} and $V_{DD}Q$ can be connected together, for 3.3V I/O operation only.
6. This parameter is sampled.

I_{DD} ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(-55°C ≤ T_A ≤ +125°C and -40°C≤T_A≤+85°C; V_{DD} = +3.3V +0.3V/-0.165V unless otherwise noted)

			MAX				
PARAMETER	**CONDITIONS**	**SYM**	**-8**	**-9**	**-10**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ t_{KC} (MIN); V_{DD} = MAX; Outputs Open	I_{DD}	375	325	250	mA	2, 3, 4
Power Supply Current: Idle	Device selected; V_{DD} = MAX; ADSC\, ADSP\, ADV\, GW\, BWx\ ≥ V_{IH}; All inputs ≤ V_{SS} +0.2 or ≥ V_{DD}Q -0.2; Cycle time ≥ ^tKC (MIN); Outputs Open	I_{DD1}	100	85	65	mA	2, 3, 4
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ Vss +0.2 or ≥ V_{DD}Q -0.2; All inputs static; CLK frequency =0	I_{SB2}	10	10	10	mA	3, 4
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	25	25	25	mA	3, 4
Clock Running	Device deselected; V_{DD} = MAX; ASDP\, ADV\, GW\, BWx\ ≥ V_{IH}; All inputs ≤ V_{SS} +0.2 or > V_{DD}Q -0.2; Cycle time ≥ ^tKC (MIN)	I_{SB4}	100	85	65	mA	3, 4

NOTES:

1. V_{DD}Q = +3.3V +0.3V/-0.165V for 3.3V I/O configuration.
2. I_{DD} is specified with no output current and increases with faster cycle times. I_{DD}Q increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
4. Typical values are measured at 3.3V, 25°C and 15ns cycle time.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 1) -55°C ≤ T_A ≤ +125°C and -40°C≤T_A≤+85°C; V_{DD} = +3.3V +0.3V/-0.165V unless otherwise noted)

DESCRIPTION	SYMBOL	-8		-9		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
CLOCK									
Clock cycle time	t_{KC}	8.8		10		15		ns	
Clock frequency	t_{KF}		113		100		66	MHz	
Clock HIGH time	t_{KH}	2.5		3.0		4.0		ns	2
Clock LOW time	t_{KL}	2.5		3.0		4.0		ns	2
OUTPUT TIMES									
Clock to output valid	t_{KQ}		7.5		8.5		10	ns	
Clock to output invalid	t_{KQX}	1.5		3.0		3.0		ns	3
Clock to output in Low-Z	t_{KQLZ}	1.5		3.0		3.0		ns	3, 4, 5
Clock to output in High-Z	t_{KQHZ}		4.2		5.0		5.0	ns	3, 4, 5
OE\ to output valid	t_{OEQ}		4.2		5.0		5.0	ns	6
OE\ to output in Low-Z	t_{OELZ}	0		0		0		ns	3, 4, 5
OE\ to output in High-Z	t_{OEHZ}		4.2		5.0		5.0	ns	3, 4, 5
SETUP TIMES									
Address	t_{AS}	1.5		1.8		2.0		ns	7, 8
Address status (ADSC\, ADSP\)	t_{ADSS}	1.5		1.8		2.0		ns	7, 8
Address advance (ADV\)	t_{AAS}	1.5		1.8		2.0		ns	7, 8
Byte write enables (BWa\-BWb\, GW\, BWE\)	t_{WS}	1.5		1.8		2.0		ns	7, 8
Data-in	t_{DS}	1.5		1.8		2.0		ns	7, 8
Chip enable (CE\)	t_{CES}	1.5		1.8		2.0		ns	7, 8
HOLD TIMES									
Address	t_{AH}	0.5		0.5		0.5		ns	7, 8
Address status (ADSC\, ADSP\)	t_{ADSH}	0.5		0.5		0.5		ns	7, 8
Address advance (ADV\)	t_{AAH}	0.5		0.5		0.5		ns	7, 8
Byte write enables (BWa\-BWb\, GW\, BWE\)	t_{WH}	0.5		0.5		0.5		ns	7, 8
Data-in	t_{DH}	0.5		0.5		0.5		ns	7, 8
Chip enable (CE\)	t_{CEH}	0.5		0.5		0.5		ns	7, 8

NOTES:

1. Test conditions as specified with the output loading shown in Figure 1 for 3.3V I/O (VDDQ = +3.3V +0.3V/-0.165V) unless otherwise noted.
2. Measured as HIGH above V_{IH} and LOW below V_{IL}.
3. This parameter is measured with the output loading shown in Figure 2 for 3.3V I/O.
4. This parameter is sampled.
5. Transition is measured ±500mV from steady state voltage.
6. OE\ is a "Don't Care" when a byte write enable is sampled LOW.
7. A READ cycle is defined by byte write enables all HIGH or ADSP\ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and ADSP\ HIGH for the required setup and hold times.
8. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP\ or ADSC\ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP\ or ADSC\ is LOW to remain enabled.

AC TEST CONDITIONS

Input pulse levels	$V_{IH} = (V_{DD}/2.2) + 1.5V$
	$V_{IL} = (V_{DD}/2.2) - 1.5V$
Input rise and fall times	1ns
Input timing reference levels	$V_{DD}/2.2$
Output reference levels	$V_{DD}Q/2.2$
Output load	See Figures 1 and 2

LOAD DERATING CURVES

ASI's 256K x 18 Synchronous Burst SRAM timing is dependent upon the capacitive loading on the outputs.

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time t_{ZZ} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not quaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

OUTPUT LOADS

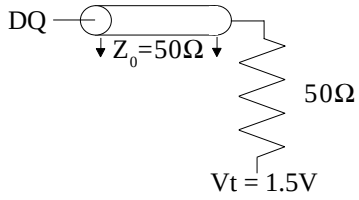


Fig. 1 OUTPUT LOAD EQUIVALENT

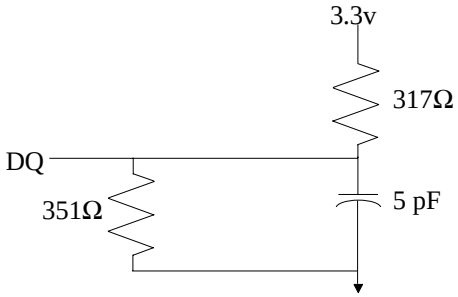


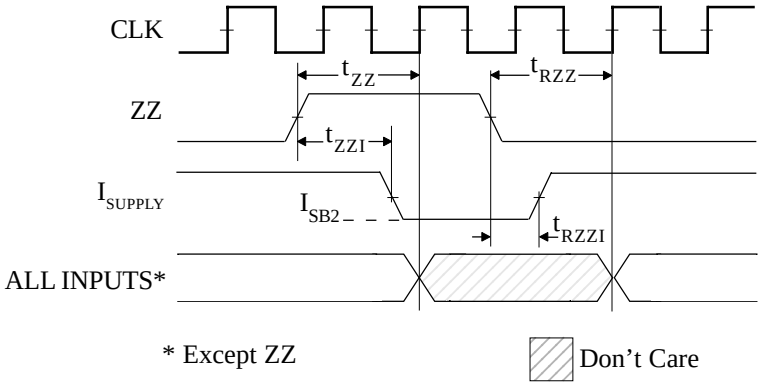
Fig. 2 OUTPUT LOAD EQUIVALENT

SNOOZE MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{SB2Z}		10	mA	
ZZ active to input ignored		t_{ZZ}		t_{KC}	ns	1
ZZ inactive to input sampled		t_{RZZ}	t_{KC}		ns	1
ZZ active to snooze current		t_{ZZI}		t_{KC}	ns	1
ZZ inactive to exit snooze current		t_{RZZI}	0		ns	1

NOTE: 1. This parameter is sampled.

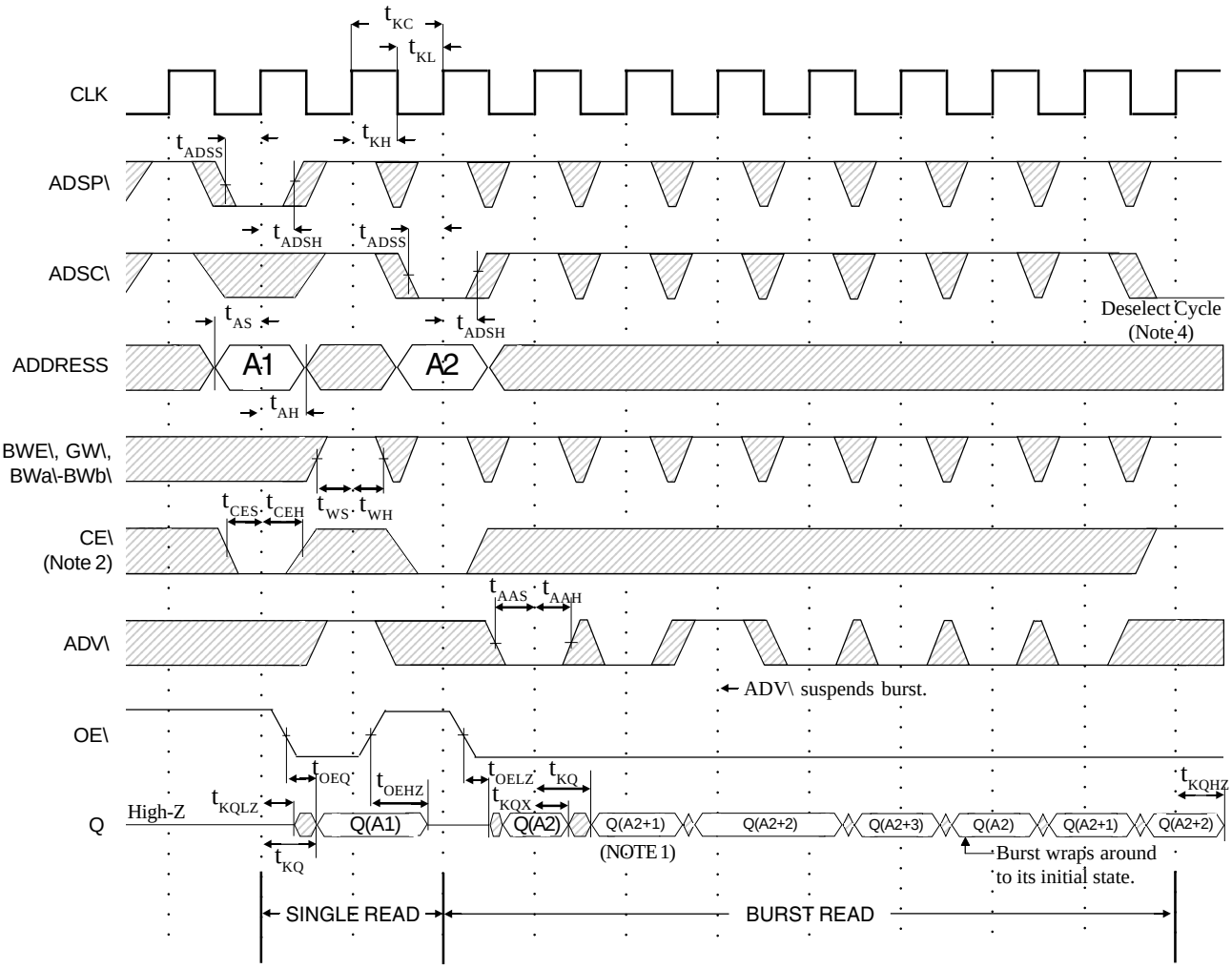
SNOOZE MODE WAVEFORM



* Except ZZ

Don't Care

READ TIMING



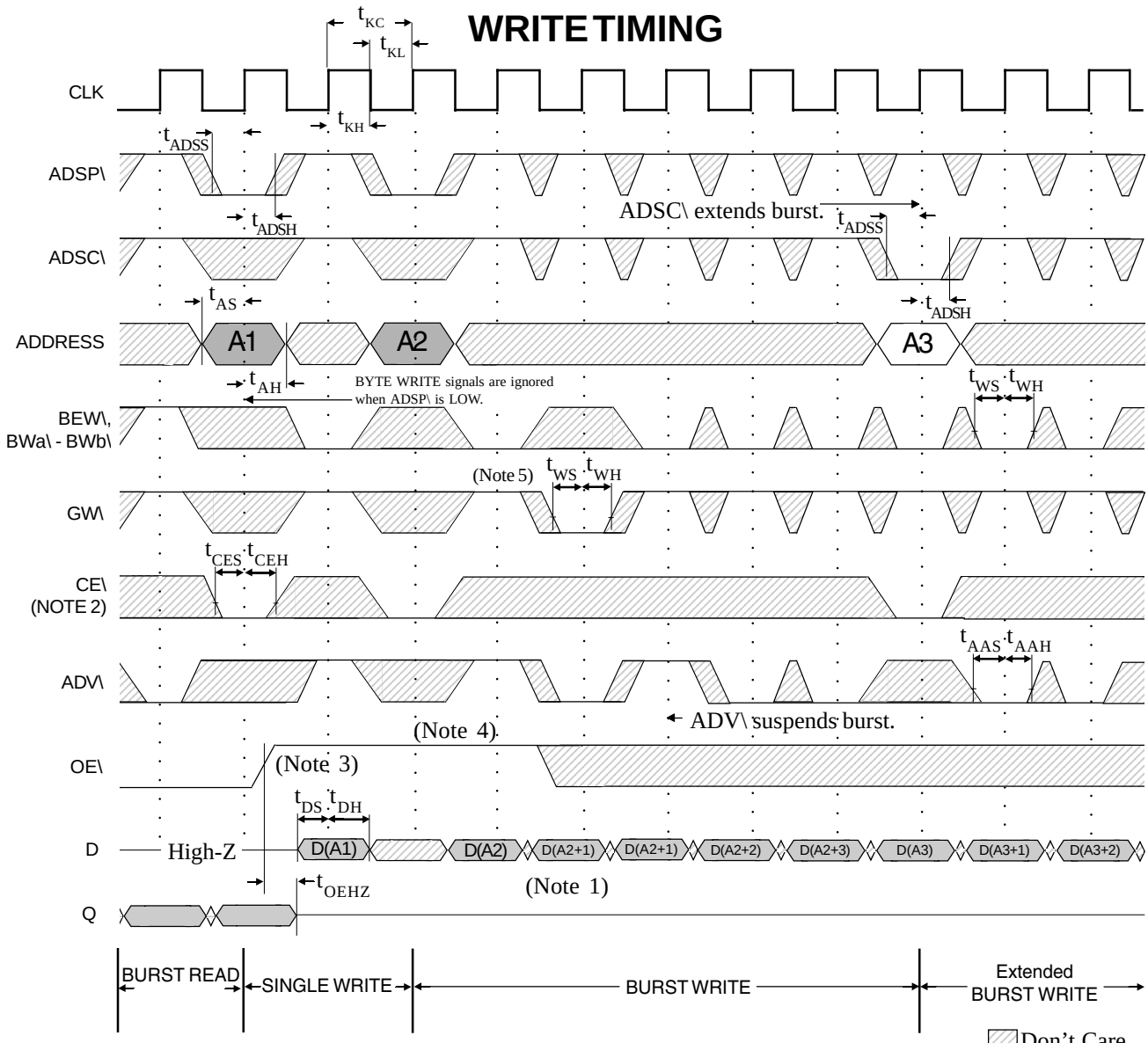
READ TIMING PARAMETERS

	-8		-9		-10		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{KC}	8.8		10		15		ns
t_{KF}		113		100		66	MHz
t_{KH}	2.5		3.0		4.0		ns
t_{KL}	2.5		3.0		4.0		ns
t_{KQ}		7.5		8.5		10	ns
t_{KQX}	1.5		3.0		3.0		ns
t_{KQLZ}	1.5		3.0		3.0		ns
t_{KQHZ}		4.2		5.0		5.0	ns
t_{OEQ}		4.2		5.0		5.0	ns
t_{OELZ}	0		0		0		ns
t_{OEHZ}		4.2		5.0		5.0	ns

	-8		-9		-10		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{AS}	1.5		1.8		2.0		ns
t_{ADSS}	1.5		1.8		2.0		ns
t_{AAS}	1.5		1.8		2.0		ns
t_{WS}	1.5		1.8		2.0		ns
t_{CES}	1.5		1.8		2.0		ns
t_{AH}	0.5		0.5		0.5		ns
t_{ADSH}	0.5		0.5		0.5		ns
t_{AAH}	0.5		0.5		0.5		ns
t_{WH}	0.5		0.5		0.5		ns
t_{CEH}	0.5		0.5		0.5		ns

NOTE:
1. Q(A2) referes to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. CE2\ and CE2 have timing identical to CE\. On this diagram, when CE\ is LOW, CE2\ is LOW and CE2 is HIGH. When CE\ is HIGH, CE2\ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence.
4. Outputs are disabled t_{KQHZ} after deselect.

WRITE TIMING



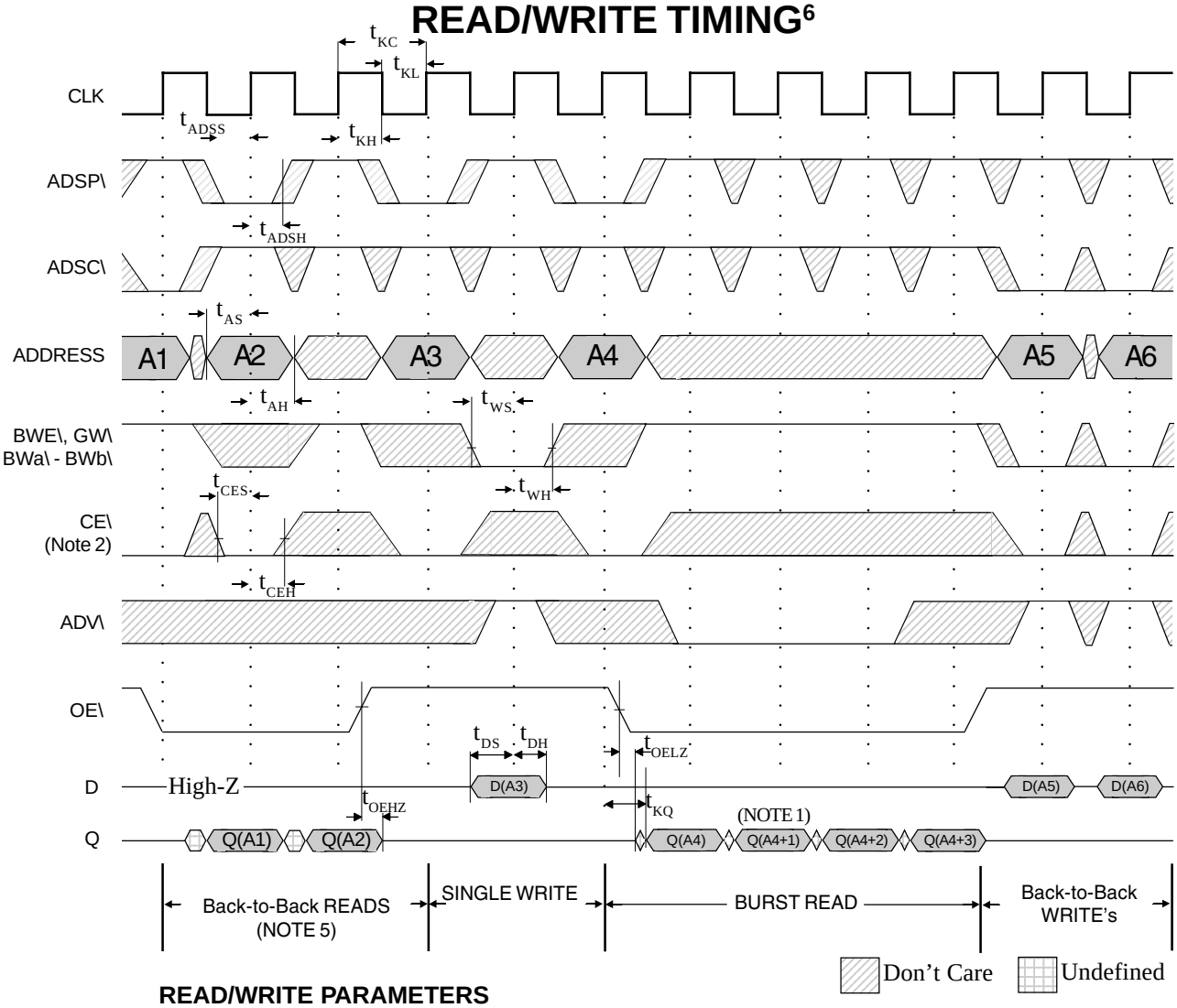
WRITE TIMING PARAMETERS

SYM	-8 MIN	-8 MAX	-9 MIN	-9 MAX	-10 MIN	-10 MAX	UNITS
t_{KC}	8.8		10		15		ns
t_{KF}		113		100		66	MHz
t_{KH}	2.5		3.0		4.0		ns
t_{KL}	2.5		3.0		4.0		ns
t_{OEHZ}		4.2		5.0		5.0	ns
t_{AS}	1.5		1.8		2.0		ns
t_{ADSS}	1.5		1.8		2.0		ns
t_{AAS}	1.5		1.8		2.0		ns
t_{WS}	1.5		1.8		2.0		ns

SYM	-8 MIN	-8 MAX	-9 MIN	-9 MAX	-10 MIN	-10 MAX	UNITS
t_{DS}	1.5		1.8		2.0		ns
t_{CES}	1.5		1.8		2.0		ns
t_{AH}	0.5		0.5		0.5		ns
t_{ADSH}	0.5		0.5		0.5		ns
t_{AAH}	0.5		0.5		0.5		ns
t_{WH}	0.5		0.5		0.5		ns
t_{DH}	0.5		0.5		0.5		ns
t_{CEH}	0.5		0.5		0.5		ns

NOTE:
1. D(A2) refers to output from address A2. D(A2+1) refres to output from the next internal burst address following A2.
2. CE2\ and CE2 have timing identical to CE\. On this diagram, when CE\ is LOW, CE2\ is LOW and CE2 is HIGH. When CE\ is HIGH, CE2\ is HIGH and CE2 is LOW.
3. OE\ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. ADV\ must be HIGH to permit a WRITE to the loaded address.
5. Full-width WRITE can be initiated by GW\ LOW; or GW\ HIGH and BWE\, BWa\ and BWb\ LOW.

READ/WRITE TIMING[6]



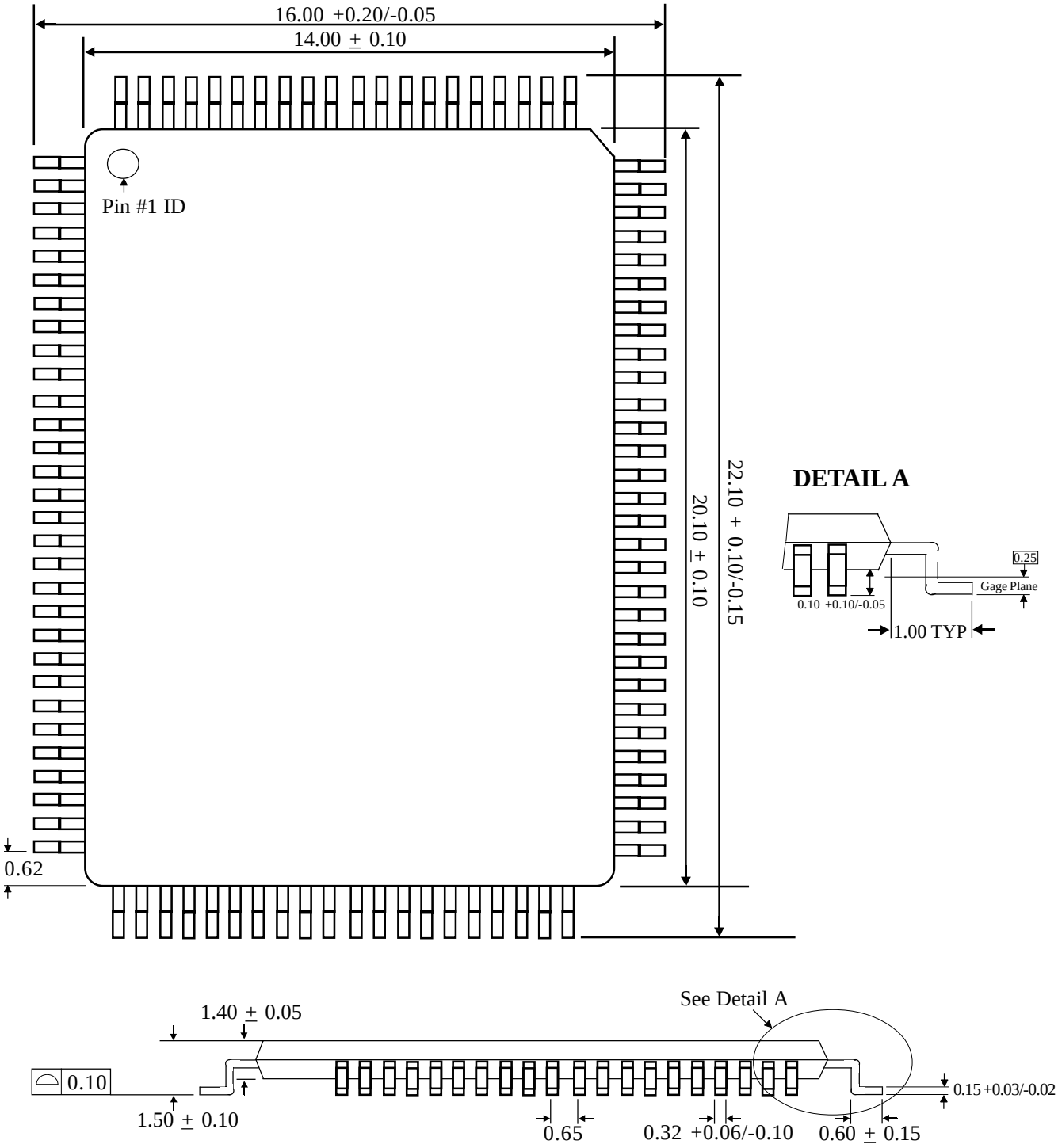
READ/WRITE PARAMETERS

SYM	-8 MIN	-8 MAX	-9 MIN	-9 MAX	-10 MIN	-10 MAX	UNITS
t_{KC}	8.8		10		15		ns
t_{KF}		113		100		66	MHz
t_{KH}	2.5		3.0		4.0		ns
t_{KL}	2.5		3.0		4.0		ns
t_{KQ}		7.5		8.5		10	ns
t_{OELZ}	0		0		0		ns
t_{OEHZ}		3.5		4.2		5.0	ns
t_{AS}	1.5		1.8		2.0		ns
t_{ADSS}	1.5		1.8		2.0		ns

SYM	-8 MIN	-8 MAX	-9 MIN	-9 MAX	-10 MIN	-10 MAX	UNITS
t_{WS}	1.5		1.8		2.0		ns
t_{DS}	1.5		1.8		2.0		ns
t_{CES}	1.5		1.8		2.0		ns
t_{AH}	0.5		0.5		0.5		ns
t_{ADSH}	0.5		0.5		0.5		ns
t_{WH}	0.5		0.5		0.5		ns
t_{DH}	0.5		0.5		0.5		ns
t_{CEH}	0.5		0.5		0.5		ns

NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. CE2\ and CE2 have timing identical to CE\. On this diagram, when CE\ is LOW, CE2\ is LOW and CE2 is HIGH. When CE\ is HIGH, CE2\ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP\, ADSC\, or ADV\ cycle is performed.
4. GW\ is HIGH.
5. Back-to-back READs may be controlled by either ADSP\ or ADSC\.
6. Timing is shown assuming that the device was not enabled before entering into this sequence.

MECHANICAL DEFINITIONS
ASI Case #1001 (Package Designator DQ)



NOTE: 1. All dimensions in Millimeters (MAX/MIN) or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protursion is 0.25mm per side.

ORDERING INFORMATION

EXAMPLE: AS5SS256K18DQ-8/IT

Device Number	Package Type	Speed ns	Process
AS5SS256K18	DQ	-8	IT only
AS5SS256K18	DQ	-9	/*
AS5SS256K18	DQ	-10	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C