EPSON

E0C33A104

32-bit Single Chip Microcomputer

- 32-bit E0C33000 RISC Core
- Multiplication and Accumulation Instruction
- 10-bit ADC, 8-bit DAC
- High-speed DMA, Intelligent DMA
- Twin-clock Oscillator

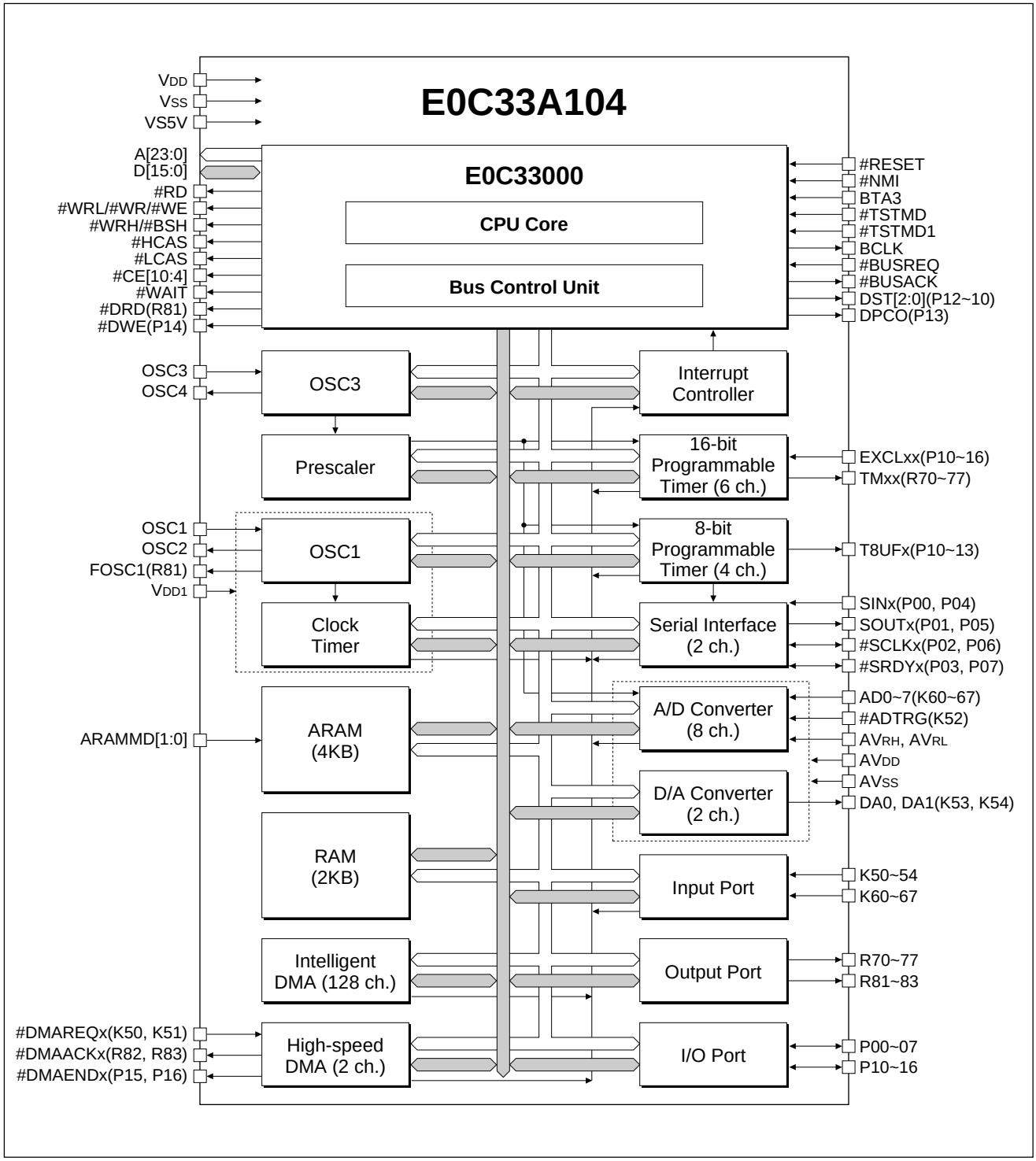
■ DESCRIPTION

The E0C33A104 is a CMOS 32-bit microcomputer composed of a CMOS 32-bit RISC core, RAM, DMA controller, timers and other circuits. The E0C33A104 features high-speed operation and low current consumption, and is suitable for various portable equipment. The E0C33A104 also contains A/D and D/A converters and MAC (multiplication and accumulation) instruction is available, which makes it possible to realize digital signal processing such as voice synthesis systems without any DSP chips.

■ FEATURES

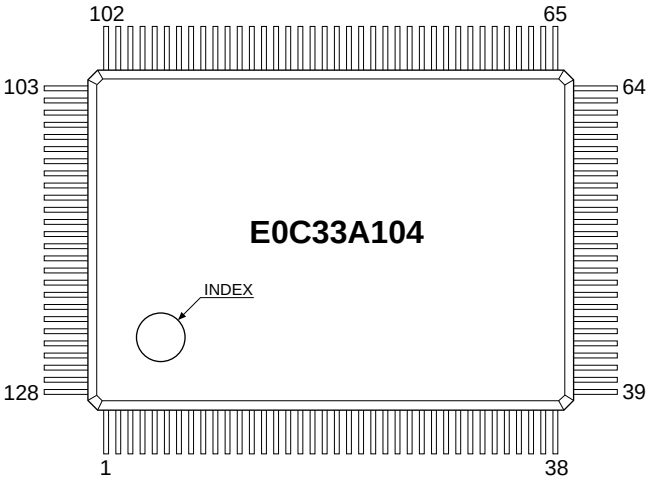
- CMOS LSI 32-bit parallel processing ..... E0C33000 RISC core
- Main clock ..... 33MHz/5V (Max.), 20MHz/3V (Max.)
  Crystal/Ceramic oscillator
- Sub clock ..... 32.768kHz (Typ.) Crystal oscillator
- Instruction set ..... 16-bit fixed size, 105 instructions with high linearity
  Multiplication and accumulation instruction
  (MAC instruction, 2 cycles)
- Built-in RAM capacity ..... Data RAM : 2,048 bytes
  Instruction RAM : 4,096 bytes, usable for data RAM
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 4 channels and 16 bits × 6 channels
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 2 channels
  Clock synchronization type and asynchronization type are selectable.
  Usable as an infrared ray (IrDA) interface.
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- 8-bit D/A converter ..... 2 output channels
- High-speed DMA ..... 2 channels
- Intelligent DMA ..... 128 channels
- General-purpose input, output and I/O ports .. 13-bit input port/11-bit output port/15-bit I/O port
  Terminals are shared with the inputs and outputs of built-in peripheral circuits.
- Interrupt controller ..... External interrupts : 6 types
  Internal interrupts : 17 systems, 39 types
- External bus interface ..... 24-bit address bus and 16-bit data bus
  DRAM and burst ROM may be connected directly.
- Shipping form QFP5-128pin/QFP15-128pin
- Supply voltage ..... 5V±10%/3.3V±0.3V
- Current consumption ..... 12µA (32.768kHz, HALT mode)

■ BLOCK DIAGRAM



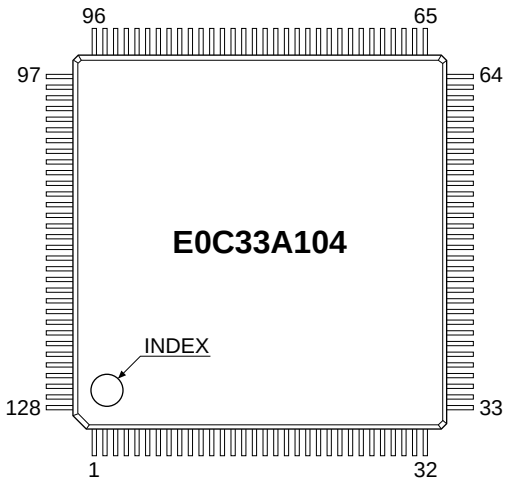
■ PIN LAYOUT

QFP5-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	#CE5/#CE15	33	OSC1	65	P03/#SRDY0	97	D1
2	#CE6	34	V_{DD1}	66	P04/SIN1	98	D0
3	#CE7/#RAS0/#CE13/#RAS2	35	K52/#ADTRG	67	P05/SOUT1	99	#WAIT
4	#CE8/#RAS1/#CE14/#RAS3	36	R70/TM00	68	P06/#SCLK1	100	ARAMMD1
5	#CE9/#CE17	37	R71/TM01	69	P07/#SRDY1	101	ARAMMD0
6	#CE10	38	R72/TM10	70	A7	102	#BUSACK
7	VS5V	39	R73/TM11	71	A6	103	#BUSREQ
8	#NMI	40	R74/TM21	72	A5	104	BCLK
9	V_{SS}	41	R75/TM31	73	A4	105	#HCAS
10	#TSTMD	42	R76/TM41	74	A3	106	#LCAS
11	#RESET	43	R77/TM51	75	A2	107	#WRH/#BSH
12	V_{DD}	44	V_{SS}	76	A1	108	#WRL/#WR/#WE
13	V_{SS}	45	V_{DD}	77	A0/#BSL	109	#RD
14	OSC4	46	P10/EXCL00/T8UF0/DST0	78	D15	110	V_{DD}
15	OSC3	47	P11/EXCL01/T8UF1/DST1	79	V_{SS}	111	A8
16	AV_{RH}	48	P12/EXCL10/T8UF2/DST2	80	D14	112	A9
17	AV_{RL}	49	P13/EXCL20/T8UF3/DPCO	81	D13	113	A10
18	AV_{SS}	50	P14/EXCL30/#BUSGET/#DWE	82	D12	114	A11
19	K67/AD7	51	P15/EXCL40/#DMAEND0	83	D11	115	A12
20	K66/AD6	52	P16/EXCL50/#DMAEND1	84	D10	116	A13
21	K65/AD5	53	BTA3	85	D9	117	A14
22	K64/AD4	54	K51/#DMAREQ1	86	D8	118	A15
23	K63/AD3	55	R83/#DMAACK1	87	D7	119	A16
24	K62/AD2	56	#TSTMD1	88	V_{DD}	120	A17
25	K61/AD1	57	R81/FOSC1/#DRD	89	V_{SS}	121	A18
26	K60/AD0	58	K50/#DMAREQ0	90	D6	122	A19
27	K53/DA0	59	R82/#DMAACK0	91	V_{DD}	123	A20
28	K54/DA1	60	P00/SIN0	92	V_{SS}	124	A21
29	AV_{DD}	61	V_{DD}	93	D5	125	A22
30	N.C.	62	V_{SS}	94	D4	126	A23
31	V_{SS}	63	P01/SOUT0	95	D3	127	V_{SS}
32	OSC2	64	P02/#SCLK0	96	D2	128	#CE4/#CE11

QFP15-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	#CE8/#RAS1/#CE14/#RAS3	33	R70/TM00	65	P06/#SCLK1	97	ARAMMD1
2	#CE9/#CE17	34	R71/TM01	66	P07/#SRDY1	98	ARAMMD0
3	#CE10	35	R72/TM10	67	A7	99	#BUSACK
4	VS5V	36	R73/TM11	68	A6	100	#BUSREQ
5	#NMI	37	R74/TM21	69	A5	101	BCLK
6	V_{SS}	38	R75/TM31	70	A4	102	#HCAS
7	#TSTMD	39	R76/TM41	71	A3	103	#LCAS
8	#RESET	40	R77/TM51	72	A2	104	#WRH/#BSH
9	V_{DD}	41	V_{SS}	73	A1	105	#WRL/#WR/#WE
10	V_{SS}	42	V_{DD}	74	A0/#BSL	106	#RD
11	OSC4	43	P10/EXCL00/T8UF0/DST0	75	D15	107	V_{DD}
12	OSC3	44	P11/EXCL01/T8UF1/DST1	76	V_{SS}	108	A8
13	AV_{RH}	45	P12/EXCL10/T8UF2/DST2	77	D14	109	A9
14	AV_{RL}	46	P13/EXCL20/T8UF3/DPCO	78	D13	110	A10
15	AV_{SS}	47	P14/EXCL30/#BUSGET/#DWE	79	D12	111	A11
16	K67/AD7	48	P15/EXCL40/#DMAEND0	80	D11	112	A12
17	K66/AD6	49	P16/EXCL50/#DMAEND1	81	D10	113	A13
18	K65/AD5	50	BTA3	82	D9	114	A14
19	K64/AD4	51	K51/#DMAREQ1	83	D8	115	A15
20	K63/AD3	52	R83/#DMAACK1	84	D7	116	A16
21	K62/AD2	53	#TSTMD1	85	V_{DD}	117	A17
22	K61/AD1	54	R81/FOSC1/#DRD	86	V_{SS}	118	A18
23	K60/AD0	55	K50/#DMAREQ0	87	D6	119	A19
24	K53/DA0	56	R82/#DMAACK0	88	V_{DD}	120	A20
25	K54/DA1	57	P00/SIN0	89	V_{SS}	121	A21
26	AV_{DD}	58	V_{DD}	90	D5	122	A22
27	V_{SS}	59	V_{SS}	91	D4	123	A23
28	OSC2	60	P01/SOUT0	92	D3	124	V_{SS}
29	OSC1	61	P02/#SCLK0	93	D2	125	#CE4/#CE11
30	N.C.	62	P03/#SRDY0	94	D1	126	#CE5/#CE15
31	V_{DD1}	63	P04/SIN1	95	D0	127	#CE6
32	K52/#ADTRG	64	P05/SOUT1	96	#WAIT	128	#CE7/#RAS0/#CE13/#RAS2

■ PIN DESCRIPTION

● Power Supply, Clock

Pin name	Pin No.		I/O	Function
	QFP5-128	QFP15-128		
V_{DD} x6	12, 45, 61, 88, 91, 110	9, 42, 58, 85, 88, 107	–	Power supply pin (+)
V_{SS} x9	9, 13, 31, 44, 62, 79, 89, 92, 127	6, 10, 27, 41, 59, 76, 86, 89, 124	–	Power supply pin (–)
V_{DD1}	34	31	–	Oscillation system power supply pin (+)
AV_{DD}	29	26	–	Analog system power supply pin (+)
AV_{SS}	18	15	–	Analog system power supply pin (–)
AV_{RH}	16	13	–	A/D converter reference voltage (+)
AV_{RL}	17	14	–	A/D converter reference voltage (–)
OSC1	33	29	I	Low-speed (OSC1) oscillation input pin (32kHz crystal oscillator)
OSC2	32	28	O	Low-speed (OSC1) oscillation output pin
OSC3	15	12	I	High-speed (OSC3) oscillation input pin (crystal/ceramic oscillator)
OSC4	14	11	O	High-speed (OSC3) oscillation output pin
VS5V	7	4	I	Input voltage threshold level setting VS5V = "0": TTL interface VS5V = "1": C-MOS interface
#TSTMD	10	7	I	E0C33A104 test pin (no pull-up resistor) Fix at high level in normal operation.
ARAMMD [1:0]	[1]:100 [0]:101	[1]:97 [0]:98	I	Built-in ARAM mode setting (no pull-up resistor) Set according to the ARAM mode to be used.
#TSTMD1	56	53	I	E0C33A104 test pin (no pull-up resistor) Fix at high level in normal operation.

● CPU, External System Bus

Pin name	Pin No.		I/O	Function
	QFP5-128	QFP15-128		
BTA3	53	50	I	Boot address setting BTA3 = "0": Booted from Area 10 (external memory)
#RESET	11	8	I	Initial reset pin
#NMI	8	5	I	NMI request pin
A0/#BSL	77	74	O	Address bus (A0)/Bus strobe low
A1–A7	76–70	73–67	O	Address bus
A8–A15	111–118	108–115	O	Address bus
A16–A23	119–126	116–123	O	Address bus
#RD	109	106	O	Read signal
#WRL/#WR/#WE	108	105	O	Low-byte write/Write/DRAM write
#WRH/#BSH	107	104	O	High-byte write/Bus strobe high
#HCAS	105	102	O	CAS output (high-byte strobe)
#LCAS	106	103	O	CAS output (low-byte strobe)
BCLK	104	101	O	Bus clock output
#BUSACK	102	99	O	Bus acknowledge
#CE4/CE11	128	125	O	Chip enable 4/Chip enable 11
#CE5/CE15	1	126	O	Chip enable 5/Chip enable 15
#CE6	2	127	O	Chip enable 6
#CE7/#RAS0/#CE13/#RAS2	3	128	O	Chip enable 7/Chip enable 13/DRAM direct control (RAS0/2 output)
#CE8/#RAS1/#CE14/#RAS3	4	1	O	Chip enable 8/Chip enable 14/DRAM direct control (RAS1/3 output)
#CE9/CE17	5	2	O	Chip enable 9/Chip enable 17
#CE10	6	3	O	Chip enable 10
D0–D7	98–93, 90, 87	95–90, 87, 84	I/O	Data bus
D8–D15	86–80, 78	83–77, 75	I/O	Data bus
#WAIT	99	96	I	Wait cycle request
#BUSREQ	103	100	I	Bus request

● Peripheral Circuit

Pin name	Pin No.		I/O	Function
	QFP5-128	QFP15-128		
K50 (/#DMAREQ0)	58	55	I	Input port/DMA request 0
K51 (/#DMAREQ1)	54	51	I	Input port/DMA request 1
K52 (/#ADTRG)	35	32	I	Input port/AD trigger
K53 (/DA0)	27	24	I	Input port/DAC output 0
K54 (/DA1)	28	25	I	Input port/DAC output 1
K60 (/AD0)	26	23	I	Input port/ADC input 0
K61 (/AD1)	25	22	I	Input port/ADC input 1
K62 (/AD2)	24	21	I	Input port/ADC input 2
K63 (/AD3)	23	20	I	Input port/ADC input 3
K64 (/AD4)	22	19	I	Input port/ADC input 4
K65 (/AD5)	21	18	I	Input port/ADC input 5
K66 (/AD6)	20	17	I	Input port/ADC input 6
K67 (/AD7)	19	16	I	Input port/ADC input 7
R70 (/TM00)	36	33	O	Output port (initial value = "0")/16-bit timer 0 (timer 00) clock output
R71 (/TM01)	37	34	O	Output port (initial value = "0")/16-bit timer 0 (timer 01) clock output
R72 (/TM10)	38	35	O	Output port (initial value = "0")/16-bit timer 1 (timer 10) clock output
R73 (/TM11)	39	36	O	Output port (initial value = "0")/16-bit timer 1 (timer 11) clock output
R74 (/TM21)	40	37	O	Output port (initial value = "0")/16-bit timer 2 (timer 21) clock output
R75 (/TM31)	41	38	O	Output port (initial value = "0")/16-bit timer 3 (timer 31) clock output
R76 (/TM41)	42	39	O	Output port (initial value = "0")/16-bit timer 4 (timer 41) clock output
R77 (/TM51)	43	40	O	Output port (initial value = "0")/16-bit timer 5 (timer 51) clock output
R81 (/FOSC1/#DRD)	57	54	O	Output port (initial value = "1")/OSC1 clock output/DRAM read
R82 (/#DMAACK0)	59	56	O	Output port (initial value = "1")/High-speed DMA acknowledge
R83 (/#DMAACK1)	55	52	O	Output port (initial value = "1")/High-speed DMA acknowledge
P00 (/SIN0)	60	57	I/O	I/O port/Serial interface Ch.0 data input
P01 (/SOUT0)	63	60	I/O	I/O port/Serial interface Ch.0 data output
P02 (/#SCLK0)	64	61	I/O	I/O port/Serial interface Ch.0 clock input/output
P03 (/#SRDY0)	65	62	I/O	I/O port/Serial interface Ch.0 ready output
P04 (/SIN1)	66	63	I/O	I/O port/Serial interface Ch.1 data input
P05 (/SOUT1)	67	64	I/O	I/O port/Serial interface Ch.1 data output
P06 (/#SCLK1)	68	65	I/O	I/O port/Serial interface Ch.1 clock input/output
P07 (/#SRDY1)	69	66	I/O	I/O port/Serial interface Ch.1 ready output
P10 (/EXCL00/T8UF0)	46	43	I/O	I/O port/Timer 00 event counter input/8-bit timer 0 output
P11 (/EXCL01/T8UF1)	47	44	I/O	I/O port/Timer 01 event counter input/8-bit timer 1 output
P12 (/EXCL10/T8UF2)	48	45	I/O	I/O port/Timer 10 event counter input/8-bit timer 2 output
P13 (/EXCL20/T8UF3)	49	46	I/O	I/O port/Timer 20 event counter input/8-bit timer 3 output
P14 (/EXCL30/#BUSGET/#DWE)	50	47	I/O	I/O port/Timer 30 event counter input/#BUSGET output/DRAM write
P15 (/EXCL40/#DMAEND0)	51	48	I/O	I/O port/Timer 40 event counter input/High-speed DMA Ch.0 end
P16 (/EXCL50/#DMAEND1)	52	49	I/O	I/O port/Timer 50 event counter input/High-speed DMA Ch.1 end

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