

HYS72T64400HFN-[3S/3.7]-B
HYS72T128420HFN-[3S/3.7]-B
HYS72T256420HFN-[3S/3.7]-B

240-Pin Fully-Buffered DDR2 SDRAM Modules
DDR2 SDRAM
RoHS Compliant Products



Internet Data Sheet

Rev. 1.1



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|--|--|
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1 Overview

This chapter describes the main characteristics of the 240-Pin Fully-Buffered DDR2 SDRAM Modules product family.

1.1 Features

- 240-pin Fully-Buffered ECC Dual-In-Line DDR2 SDRAM Module for PC, Workstation and Server main memory applications.
- Module organisation one rank 64M × 72, one rank 128M × 72, two ranks 128M × 72, two ranks 256M × 72
- JEDEC Standard Double Data Rate 2 Synchronous DRAMs (DDR2 SDRAMs) with 1.8 V (± 0.1 V) power supply.
- Built with 512Mb DDR2 SDRAMs in 60-ball FBGA Chipsize Packages.
- Re-drive and re-sync of all address, command, clock and data signals using AMB (Advanced Memory Buffer).
- High-Speed Differential Point-to-Point Link Interface at 1.5 V (Jedec standard pending).
- Host Interface and AMB component industry standard compliant.
- Supports SMBus protocol interface for access to the AMB configuration registers.
- Detects errors on the channel and reports them to the host memory controller.
- Automatic DDR2 DRAM Bus Calibration.
- Automatic Channel Calibration.
- Full Host Control of the DDR2 DRAMs.
- Over-Temperature Detection and Alert.
- Hot Add-on and Hot Remove Capability.
- MBIST and IBIST Test Functions.
- Transparent Mode for DRAM Test Support.
- Low profile: 133.35mm × 30.35 mm
- 240 Pin gold plated card connector with 1.00mm contact centers (JEDEC standard pending).
- Based on JEDEC standard reference card designs (Jedec standard pending).
- SPD (Serial Presence Detect) with 256 Byte serial E²PROM.Performance:
- RoHS Compliant Products¹⁾

TABLE 1
Performance for DDR2-667 and DDR2-533

| Product Type Speed Code | | | -3S | -3.7 | Unit |
|-------------------------|------|-----------|----------------|----------------|------|
| Speed Grade | | | PC2-5300 5-5-5 | PC2-4200 4-4-4 | — |
| max. Clock Frequency | @CL5 | f_{CK5} | 333 | 266 | MHz |
| | @CL4 | f_{CK4} | 266 | 266 | MHz |
| | @CL3 | f_{CK3} | 200 | 200 | MHz |
| min. RAS-CAS-Delay | | t_{RCD} | 15 | 15 | ns |
| min. Row Precharge Time | | t_{RP} | 15 | 15 | ns |
| min. Row Active Time | | t_{RAS} | 45 | 45 | ns |
| min. Row Cycle Time | | t_{RC} | 60 | 60 | ns |

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.



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1.2 Description

This document describes the electrical and mechanical features of Qimonda's 240-pin, PC2-4200F, PC2-5300F ECC type, Fully Buffered Double-Data-Rate Two Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FB-DIMMs). Fully Buffered DIMMs use commodity DRAMs isolated from the memory channel behind a buffer on the DIMM. They are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200, PC2-5300 refers to the DIMM naming convention indicating the DDR2 SDRAMs running at 266, 333 MHz clock speed and offering 4200, 5300 MB/s peak bandwidth. FB-DIMM features a novel architecture including the Advanced Memory Buffer. This single chip component, located in the center of each DIMM, acts as a repeater and buffer for all signals and commands which are exchanged between the host controller and the DDR2 SDRAMs including data in- and output. The AMB communicates with the host controller and / or the adjacent DIMMs on a system board using an Industry

Standard High-Speed Differential Point-to-Point Link Interface at 1.5 V.

The Advanced Memory Buffer also allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The Advanced Memory Buffer interface is responsible for handling channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the memory channel. Fully Buffered DIMM provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. The maximum memory capacity is 288 DDR2 SDRAM devices per channel or 8 DIMMs.



TABLE 2
Ordering Information (Pb-free components and assembly)

| Product Type ¹⁾ | Compliance Code ²⁾ | Description | SDRAM Technology |
|------------------------------|-------------------------------|------------------|------------------|
| PC2-4200F (DDR2-533): | | | |
| HYS72T64400HFN-3.7-B | 512MB 1R×8 PC2-4200F-444-11-A | 1 Rank, FB-DIMM | 512 Mbit (×8) |
| HYS72T128420HFN-3.7-B | 1GB 2R×8 PC2-4200F-444-11-B | 2 Ranks, FB-DIMM | 512 Mbit (×8) |
| HYS72T256420HFN-3.7-B | 2GB 2R×4 PC2-4200F-444-11-H | 2 Ranks, FB-DIMM | 512 Mbit (×4) |
| PC2-5300F (DDR2-667): | | | |
| HYS72T64400HFN-3S-B | 512MB 1R×8 PC2-4200F-444-11-A | 1 Rank, FB-DIMM | 512 Mbit (×8) |
| HYS72T128420HFN-3S-B | 1GB 2R×8 PC2-4200F-444-11-B | 2 Ranks, FB-DIMM | 512 Mbit (×8) |
| HYS72T256420HFN-3S-B | 2GB 2R×4 PC2-4200F-444-11-H | 2 Ranks, FB-DIMM | 512 Mbit (×4) |

- 1) All product types end with a place code, designating the silicon die revision. Example: HYS 72T64000HFA-3.7-A, indicating Rev. A dice are used for DDR2 SDRAM components. To learn more on Qimonda DDR2 module and component nomenclature see section 8 of this datasheet.
- 2) The Compliance Code is printed on the module label and describes the speed grade, e.g. "PC2-4200F-444-11-A", where 4200F means Fully Buffered DIMM with 4.26 GB/sec. Module Bandwidth and "444-11" means CAS latency = 4, t_{rd} latency = 4 and t_{rp} latency = 4 using JEDEC SPD Revision 1.1 and assembled on Raw Card "A".



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TABLE 3
Address Format

| DIMM Density | Module Organization | Memory Ranks | ECC/ Non-ECC | # of SDRAMs | # of row/bank/columns bits | Raw Card |
|--------------|---------------------|--------------|--------------|-------------|----------------------------|----------|
| 512 MB | 64M ×72 | 1 | ECC | 9 | 13/2/10 | A |
| 1 GB | 128M ×72 | 2 | ECC | 18 | 13/2/10 | B |
| 2 GB | 256M ×72 | 2 | ECC | 36 | 13/2/11 | H |

TABLE 4
Components on Modules

| Product Type | DRAM components ¹⁾ | DRAM Density | DRAM Organisation | Note ²⁾ |
|----------------|-------------------------------|--------------|-------------------|--------------------|
| HYS72T64000HF | HYB18T512800BF | 512 Mbit | 64M ×8 | |
| HYS72T128020HF | HYB18T512800BF | 512 Mbit | 64M ×8 | |
| HYS72T256020HF | HYB18T512400BF | 512 Mbit | 128M ×4 | |

1) Green Product

2) For a detailed description of all functionalities of the DRAM components on these modules see the component datasheet.



2 Pin Configuration

The pin configuration of the DDR2 SDRAM DIMM is listed by function in **Table 5** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 5
Pin Configuration of FB-DIMM

| Pin# | Name | Pin Type | Buffer Type | Function |
|------------------------|---------------------------|----------|-------------|--|
| Clock Signals | | | | |
| 228 | SCK | I | HSDL_15 | System Clock Input, positive line |
| 229 | $\overline{\text{SCK}}$ | I | HSDL_15 | System Clock Input, negative line |
| Control Signals | | | | |
| 17 | $\overline{\text{RESET}}$ | I | LV-CMOS | AMB reset signal |
| Northbound | | | | |
| 22 | PN0 | O | HSDL_15 | Primary Northbound Data, positive lines |
| 25 | PN1 | O | HSDL_15 | |
| 28 | PN2 | O | HSDL_15 | |
| 31 | PN3 | O | HSDL_15 | |
| 34 | PN4 | O | HSDL_15 | |
| 37 | PN5 | O | HSDL_15 | |
| 51 | PN6 | O | HSDL_15 | |
| 54 | PN7 | O | HSDL_15 | |
| 57 | PN8 | O | HSDL_15 | |
| 60 | PN9 | O | HSDL_15 | |
| 63 | PN10 | O | HSDL_15 | |
| 66 | PN11 | O | HSDL_15 | |
| 48 | PN12 | O | HSDL_15 | |
| 40 | PN13 | O | HSDL_15 | |
| 23 | $\overline{\text{PN0}}$ | O | HSDL_15 | |
| 26 | $\overline{\text{PN1}}$ | O | HSDL_15 | |
| 29 | $\overline{\text{PN2}}$ | O | HSDL_15 | |
| 32 | $\overline{\text{PN3}}$ | O | HSDL_15 | |
| 35 | $\overline{\text{PN4}}$ | O | HSDL_15 | |
| 38 | $\overline{\text{PN5}}$ | O | HSDL_15 | |
| 52 | $\overline{\text{PN6}}$ | O | HSDL_15 | |
| 55 | $\overline{\text{PN7}}$ | O | HSDL_15 | |
| 58 | $\overline{\text{PN8}}$ | O | HSDL_15 | |
| 61 | $\overline{\text{PN9}}$ | O | HSDL_15 | |
| 64 | $\overline{\text{PN10}}$ | O | HSDL_15 | |



| Pin# | Name | Pin Type | Buffer Type | Function |
|-------------------|------|----------|-------------|--|
| 67 | PN11 | O | HSDL_15 | |
| 49 | PN12 | O | HSDL_15 | |
| 41 | PN13 | O | HSDL_15 | |
| 142 | SN0 | I | HSDL_15 | Secondary Northbound Data, positive lines |
| 145 | SN1 | I | HSDL_15 | |
| 148 | SN2 | I | HSDL_15 | |
| 151 | SN3 | I | HSDL_15 | |
| 154 | SN4 | I | HSDL_15 | |
| 157 | SN5 | I | HSDL_15 | |
| 171 | SN6 | I | HSDL_15 | |
| 174 | SN7 | I | HSDL_15 | |
| 177 | SN8 | I | HSDL_15 | |
| 180 | SN9 | I | HSDL_15 | |
| 183 | SN10 | I | HSDL_15 | |
| 186 | SN11 | I | HSDL_15 | |
| 168 | SN12 | I | HSDL_15 | |
| 160 | SN13 | I | HSDL_15 | |
| 143 | SN0 | I | HSDL_15 | |
| 146 | SN1 | I | HSDL_15 | |
| 149 | SN2 | I | HSDL_15 | |
| 152 | SN3 | I | HSDL_15 | |
| 155 | SN4 | I | HSDL_15 | |
| 158 | SN5 | I | HSDL_15 | |
| 172 | SN6 | I | HSDL_15 | |
| 175 | SN7 | I | HSDL_15 | |
| 178 | SN8 | I | HSDL_15 | |
| 181 | SN9 | I | HSDL_15 | |
| 184 | SN10 | I | HSDL_15 | |
| 187 | SN11 | I | HSDL_15 | |
| 169 | SN12 | I | HSDL_15 | |
| 161 | SN13 | I | HSDL_15 | |
| Southbound | | | | |
| 70 | PS0 | I | HSDL_15 | Primary Southbound Data, positive lines |
| 73 | PS1 | I | HSDL_15 | |
| 76 | PS2 | I | HSDL_15 | |
| 79 | PS3 | I | HSDL_15 | |
| 82 | PS4 | I | HSDL_15 | |
| 93 | PS5 | I | HSDL_15 | |
| 96 | PS6 | I | HSDL_15 | |
| 99 | PS7 | I | HSDL_15 | |



| Pin# | Name | Pin Type | Buffer Type | Function |
|---------------|------|----------|-------------|--|
| 102 | PS8 | I | HSDL_15 | Primary Southbound Data, negative lines |
| 90 | PS9 | I | HSDL_15 | |
| 71 | PS0 | I | HSDL_15 | |
| 74 | PS1 | I | HSDL_15 | |
| 77 | PS2 | I | HSDL_15 | |
| 80 | PS3 | I | HSDL_15 | |
| 83 | PS4 | I | HSDL_15 | |
| 94 | PS5 | I | HSDL_15 | |
| 97 | PS6 | I | HSDL_15 | |
| 100 | PS7 | I | HSDL_15 | |
| 103 | PS8 | I | HSDL_15 | |
| 91 | PS9 | I | HSDL_15 | |
| 190 | SS0 | O | HSDL_15 | Secondary Southbound data, positive lines |
| 193 | SS1 | O | HSDL_15 | |
| 196 | SS2 | O | HSDL_15 | |
| 199 | SS3 | O | HSDL_15 | |
| 202 | SS4 | O | HSDL_15 | |
| 213 | SS5 | O | HSDL_15 | |
| 216 | SS6 | O | HSDL_15 | |
| 219 | SS7 | O | HSDL_15 | |
| 222 | SS8 | O | HSDL_15 | |
| 210 | SS9 | O | HSDL_15 | Secondary Southbound data, negative lines |
| 191 | SS0 | O | HSDL_15 | |
| 194 | SS1 | O | HSDL_15 | |
| 197 | SS2 | O | HSDL_15 | |
| 200 | SS3 | O | HSDL_15 | |
| 203 | SS4 | O | HSDL_15 | |
| 214 | SS5 | O | HSDL_15 | |
| 217 | SS6 | O | HSDL_15 | |
| 220 | SS7 | O | HSDL_15 | |
| 223 | SS8 | O | HSDL_15 | |
| 211 | SS9 | O | HSDL_15 | |
| EEPROM | | | | |
| 120 | SCL | I | CMOS | Serial Bus Clock |
| 119 | SDA | I/O | OD | Serial Bus Data |
| 239 | SA0 | I | CMOS | Serial Address Select Bus 2:0 |
| 240 | SA1 | I | CMOS | |
| 118 | SA2 | I | CMOS | |



| Pin# | Name | Pin Type | Buffer Type | Function |
|--|--------------------|----------|-------------|---|
| Power Supplies | | | | |
| 238 | V _{DDSPD} | PWR | – | EEPROM Power Supply |
| 9,10,12,13,129,130,132,133 | V _{CC} | PWR | – | AMB Core Power / Channel Interface Power |
| 15,117,135,237 | V _{TT} | PWR | – | Address/Command/Clock Termination Power |
| 1,2,3,5,6,7,108,109,111,112,113,115,116,121,122,123,125,126,127,231,232,233,235,236 | V _{DD} | PWR | – | Power Supply |
| 4,8,11,14,18,21,24,27,30,33,36,39,42,43,46,47,50,53,56,59,62,65,68,69,72,75,78,81,84,85,88,89,92,95,98,101,104,107,110,114,124,128,131,134,138,141,144,147,150,153,156,159,162,163,166,167,170,173,176,179,182,185,188,189,192,195,198,201,204,205,208,209,212,215,218,221,224,227,230,234 | V _{SS} | GND | – | Ground Plane |
| Other Pins | | | | |
| 19,20,44,45,86,87,105,106,139,140,164,165,206,207,225,226 | RFU | NC | – | Not connected |
| 136 | VID0 | – | – | Voltage ID |
| 16 | VID1 | – | – | |
| 137 | Test | AI | – | VREF |



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TABLE 6
Abbreviations for Buffer Type

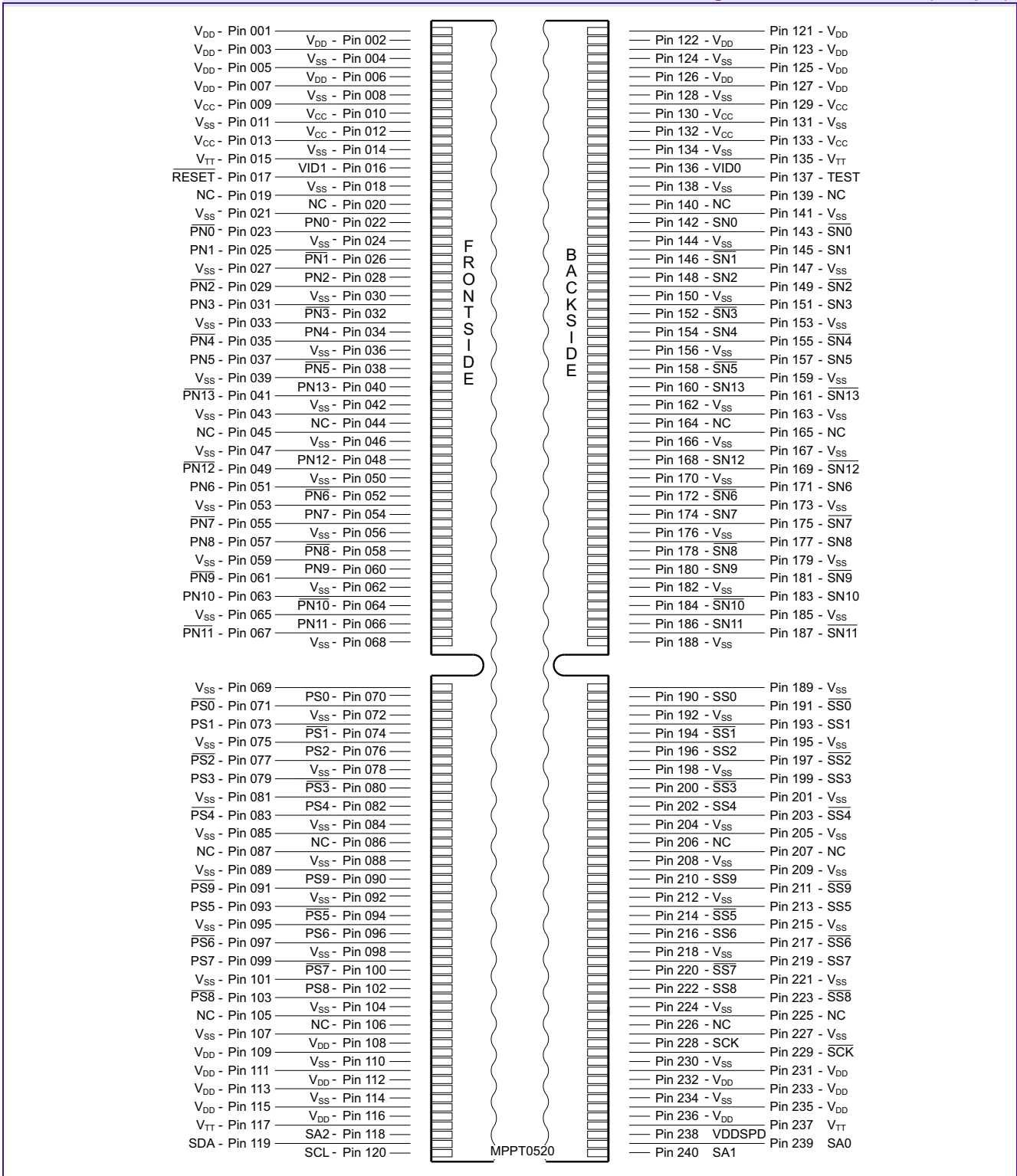
| Abbreviation | Description |
|--------------|---|
| HSDL_15 | High-Speed Differential Point-to-Point Link Interface at 1.5 V |
| LV-CMOS | Low Voltage CMOS |
| CMOS | CMOS Levels |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. |

TABLE 7
Abbreviations for Pin Type

| Abbreviation | Description |
|--------------|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| PWR | Power |
| GND | Ground |
| NU | Not Usable |
| NC | Not Connected |



FIGURE 1
Pin Configuration for FB-DIMM (240 pin)





3 Basic Functionality

The Advanced Memory Buffer (AMB) reference design complies with the FB-DIMM Architecture and Protocol Specification.

3.1 Advanced Memory Buffer Functionality

The Advanced Memory Buffer will perform the following FB-DIMM channel functions:

- Supports channel initialization procedures as defined in the initialization chapter of the FB-DIMM Architecture and Protocol Specification to align the clocks and the frame boundaries, verify channel connectivity, and identify AMB DIMM position.
- Supports the forwarding of southbound and northbound frames, servicing requests directed to a specific AMB or DIMM, as defined in the protocol chapter, and merging the return data into the northbound frames.
- If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames.
- Detects errors on the channel and reports them to the host memory controller.
- Support the FB-DIMM configuration register set as defined in the register chapters.
- Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.
- Provides a read buffer FIFO and a write buffer FIFO.
- Supports an SMBus protocol interface for access to the AMB configuration registers.
- Provides logic to support MEMBIST and IBIST Design for Test functions.
- Provides a register interface for the thermal sensor and status indicator.
- Functions as a repeater to extend the maximum length of FB-DIMM Links.

Transparent Mode for DRAM Test Support

In this mode, the Advanced Memory Buffer will provide lower speed tester access to DRAM pins through the FB-DIMM I/O pins. This allows the tester to send an arbitrary test pattern to the DRAMs. Transparent mode only supports a maximum DRAM frequency equivalent to DDR2 400. Transparent mode functionality:

- Reconfigures FB-DIMM inputs from differential high speed link receivers to two single ended lower speed receivers (~200 MHz)
- These inputs directly control DDR2 Command/Address and input data that is replicated to all DRAMs
- Uses low speed direct drive FB-DIMM outputs to bypass high speed Parallel/Serial circuitry and provide test results back to tester

DDR2 SDRAM Interface

- Supports DDR2 at speeds of 533, 667MT/s
- Supports 256Mb, 512Mb and 1Gb devices in x4 and x8 configurations
- 72-bit DDR2 SDRAM memory array

3.2 Interfaces

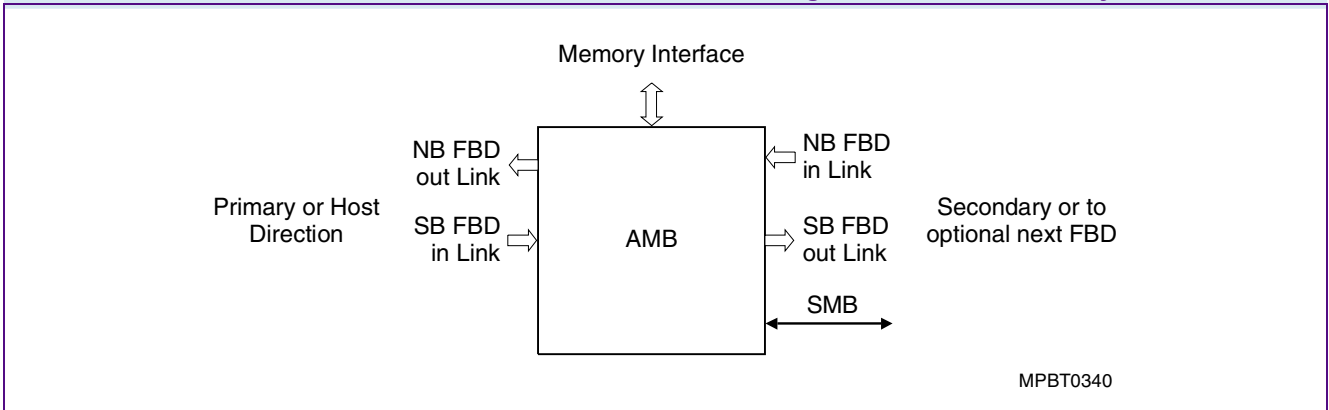
Figure 2 illustrates the Advanced Memory Buffer and all of its interfaces. They consist of two FB-DIMM links, one DDR2 channel and an SMBus interface. Each FB-DIMM link connects the Advanced Memory Buffer to a host memory

controller or an adjacent FB-DIMM. The DDR2 channel supports direct connection to the DDR2 SDRAMs on a Fully Buffered DIMM.



FIGURE 2

Block Diagram Advanced Memory Buffer Interface



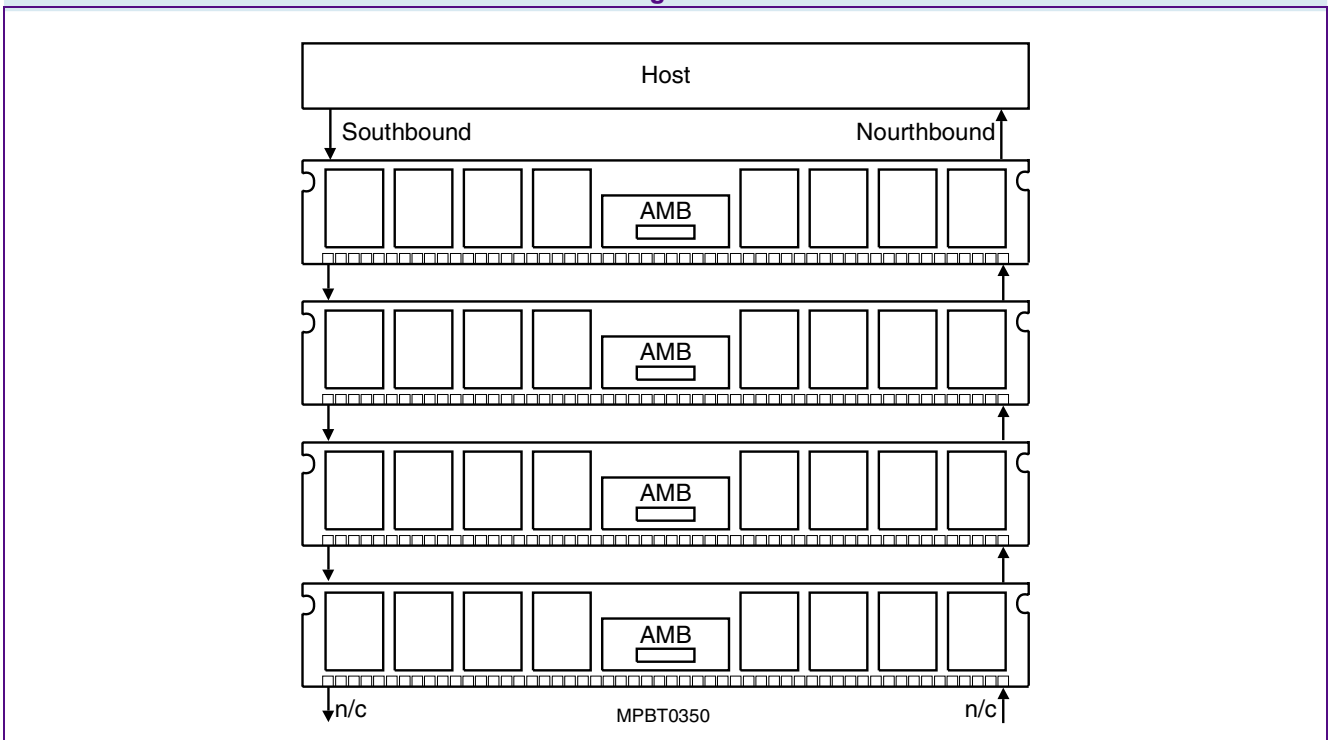
Interface Topology

The FB-DIMM channel uses a daisy-chain topology to provide expansion from a single DIMM per channel to up to 8 DIMMs per channel. The host sends data on the southbound link to the first DIMM where it is received and redriven to the second DIMM. On the southbound data path each DIMM receives the data and again re-drives the data to the next DIMM until the

last DIMM receives the data. The last DIMM in the chain initiates the transmission of data in the direction of the host (a.k.a. northbound). On the northbound data path each DIMM receives the data and re-drives the data to the next DIMM until the host is reached.

FIGURE 3

Block Diagram of Channel Southbound and Northbound Paths





3.3 High-Speed Differential Point-to-Point Link (at 1.5 V) Interfaces

The Advanced Memory Buffer supports one FB-DIMM Channel consisting of two bidirectional link interfaces using highspeed differential point-to-point electrical signaling. The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FB-DIMM. The northbound input link is 14 lanes wide and carries read return data or status information from the next FB-DIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any

read return data or status information that is generated internally. Data and commands sent to the DRAMs travel southbound on 10 primary differential signal line pairs. Data received from the DRAMs and status information travel northbound on 14 primary differential pairs. Data and commands sent to the adjacent DIMM upstream are repeated and travel further southbound on 10 secondary differential pairs. Data and status information received from the adjacent DIMM upstream travel further northbound on 14 secondary differential pairs.

3.3.1 DDR2 Channel

The DDR2 channel on the Advanced Memory Buffer supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data, and eight check-bit signals. There are two copies of address and command signals to support DIMM routing and electrical requirements. Four transfer bursts are driven on the data and check-bit lines at 800 MHz.

Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machines using write/read trial and error. Hardware aligns the read data and check-bits to a single core clock. The Advanced Memory Buffer provides four copies of the command clock phase references (CLK[3:0]) and write data/check-bit strobes (DQSs) for each DRAM nibble.

3.3.2 SMBus Slave Interface

The Advanced Memory Buffer supports an SMBus interface to allow system access to configuration registers independent of the FB-DIMM link. The Advanced Memory Buffer will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 kHz. SMBus access to the Advanced Memory Buffer may be a requirement to boot and

to set link strength, frequency and other parameters needed to insure robust configurations. It is also required for diagnostic support when the link is down. The SMBus address straps located on the DIMM connector are used by the unique ID.

3.3.3 Channel Latency

FB-DIMM channel latency is measured from the time a read request is driven on the FB-DIMM channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller. When not using the Variable Read Latency capability, the latency for a specific DIMM on a channel is always equal to the latency for any other DIMM on that channel. However, the latency for each DIMM in a specific configuration with some number of DIMMs installed may not be equal to the latency for each FB-DIMM in a configuration with some different number of DIMMs installed. As more DIMMs are added to the channel, additional latency is required to read from each DIMM on the

channel. Because the channel is based on the point-to-point interconnection of buffer components between DIMMs, memory requests are required to travel through N-1 buffers before reaching the Nth buffer. The result is that a 4 DIMM channel configuration will have greater idle read latency compared to a 1 DIMM channel configuration. The Variable Read Latency capability can be used to reduce latency for DIMMs closer to the host. The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values listed will have higher application performance and vice versa.



3.3.4 Peak Theoretical Channel Throughput

An FB-DIMM channel transfers read completion data on the Northbound data connection. 144 bits of data are transferred for every Northbound data frame. This matches the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 from a single channel or a DRAM burst of four from two lock stepped channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). The FB-DIMM frame rate matches the DRAM command clock because of the fixed 6:1 ratio of the FB-DIMM channel clock to the DRAM command clock. Therefore, the Northbound data connection will exhibit the same peak theoretical throughput as a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Northbound data connection is 4.267 GB/sec. Write data is transferred on the Southbound command and data connection, via Command+Wdata frames. 72 bits of data are transferred for every Command+Wdata frame. Two Command+Wdata frames match the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 transfers

from a single channel, or a burst of 4 from two lock-step channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). When the frame rate matches the DRAM command clock, the Southbound command and data connection will exhibit one half the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Southbound command and data connection is 2.133 GB/sec. The total peak theoretical throughput for a single FB-DIMM channel is defined as the sum of the peak theoretical throughput of the Northbound data connection and the Southbound command and data connection. When the frame rate matches the DRAM command clock, this is equal to 1.5 times the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical throughput of a single DDR2-533 channel would be 4.267 GB/sec., while the peak theoretical throughput of the entire FB-DIMM PC4200F channel would be 6.4GB/sec.

3.4 Hot-add

The FB-DIMM channel does not provide a mechanism to automatically detect and report the addition of a new DIMM south of the currently active last DIMM. It is assumed the system will be notified through some means of the addition of one or more new DIMMs so that specific commands can be sent to the host controller to initialize the newly added

DIMM(s) and perform a Hot-Add Reset to bring them into the channel timing domain. It should be noted that the power to the DIMM socket must be removed before a “hot-add” DIMM is inserted or removed. Applying or removing the power to a DIMM socket is a system platform function.

3.5 Hot-remove

In order to accomplish removal of DIMMs the host must perform a Fast Reset sequence targeted at the last DIMM that will be retained on the channel. The Fast Reset re-establish the appropriate last DIMM so that the Southbound Tx outputs of the last active DIMM and the Southbound and Northbound outputs of the DIMMs beyond the last active DIMM are disabled. Once the appropriate outputs are disabled the

system can coordinate the procedure to remove power in preparation for physical removal of the DIMM if needed. It should be noted that the power to the DIMM socket must be removed before a “hot-add” DIMM is inserted or removed. Applying or removing the power to a DIMM socket is a system platform function.

3.6 Hot-replace

Hot replace of DIMM is accomplished through combining the Hot-Remove and Hot-Add process.



4 Electrical Characteristics

4.1 Operating Conditions

TABLE 8
Absolute Maximum Ratings

| Symbol | Parameter | Rating | | Unit | Note |
|-------------------|---|--------|-------|------|------|
| | | Min. | Max. | | |
| V_{DD} | Voltage on V_{DD} pin relative to V_{SS} | -0.5 | +2.3 | V | 1) |
| V_{CC} | Voltage on V_{CC} pin relative to V_{SS} | -0.3 | 1.75 | V | |
| V_{DDQ} | Voltage on V_{DDQ} pin relative to V_{SS} | -0.5 | +2.3 | V | 1)2) |
| V_{DDL} | Voltage on V_{DDL} pin relative to V_{SS} | -0.5 | +2.3 | V | 1)2) |
| V_{IN}, V_{OUT} | Voltage on any pin relative to V_{SS} | -0.3 | +1.75 | V | 1) |
| T_{STG} | Storage Temperature | -55 | +100 | °C | 1)2) |
| V_{TT} | Voltage on V_{TT} pin relative to V_{SS} | -0.5 | 2.3 | V | |

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.

2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Attention: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 9
Operating Temperature Range

| Symbol | Parameter | Values | | Unit | Note |
|------------|---------------------------------------|--------|------|------|--------|
| | | Min. | Max. | | |
| T_{CASE} | DRAM Component Case Temperature Range | 0 | +95 | °C | 1)2)3) |
| T_{CASE} | AMB Component Case Temperature Range | 0 | +110 | °C | 1) |

1) Within the DRAM Component Case Temperature range all DRAM specification will be supported.

2) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C case temperature before initiating self-refresh operation.

3) Above 85 °C DRAM case temperature the Auto-Refresh command interval has to be reduced to $t_{REFI} = 3.9 \mu s$.



TABLE 10
Supply Voltage Levels and DC Operating Conditions

| Parameter | Symbol | Limit Values | | | Unit | Note |
|-----------------------------|---------------------|------------------------|------------------------|------------------------|------|------|
| | | Min. | Nom. | Max. | | |
| AMB Supply Voltage | V _{CC} | 1.455 | 1.5 | 1.575 | V | |
| DRAM Supply Voltage | V _{DD} | 1.7 | 1.8 | 1.9 | V | |
| Termination Voltage | V _{TT} | 0.48 × V _{DD} | 0.50 × V _{DD} | 0.52 × V _{DD} | V | |
| EEPROM Supply Voltage | V _{DDSPD} | 3.0 | 3.3 | 3.6 | V | |
| DC Input Logic High (SPD) | V _{IH(DC)} | 2.1 | — | V _{DDSPD} | V | 1) |
| DC Input Logic Low (SPD) | V _{IL(DC)} | — | — | 0.8 | V | 1) |
| DC Input Logic High (RESET) | V _{IH(DC)} | 1.0 | — | — | V | 2) |
| DC Input Logic Low (RESET) | V _{IL(DC)} | — | — | +0.5 | V | 1) |
| Leakage Current (RESET) | I _L | -90 | — | +90 | μA | 2) |
| Leakage Current (Link) | I _L | -5 | — | +5 | μA | 3) |

- 1) applies for SMB and SPD Bus Signals
- 2) applies for AMB CMOS Signal RESET
- 3) for all other AMB related DC parameters, please refer to the High Speed Differential Link Interface Specifications

TABLE 11
Timing Parameters

| Parameter | Symbol | Min. | Typ. | Max. | Units | Notes |
|---|--|------|-------|---------|--------|-------|
| EI Assertion Pass-Thru Timing | t _{EI Propagate} [†] | — | — | 4 | clks | |
| EI Deassertion Pass-Thru Timing | t _{EID} | — | — | Bitlock | clks | 2) |
| EI Assertion Duration | t _{EI} | 100 | — | — | clks | 1)2) |
| FBD Cmd to DDR Clk out that latches Cmd | — | — | 8.1 | — | ns | 3) |
| FBD Cmd to DDR Write | — | — | TBD | — | ns | |
| DDR Read to FBD (last DIMM) | — | — | 5.0 | — | ns | 4) |
| Resample Pass-Thru time | — | — | 1.075 | — | ns | |
| Resynch Pass-Thru time | — | — | 2.075 | — | ns | |
| Bit Lock Interval | t _{BitLock} | — | — | 119 | frames | 1) |
| Frame Lock Interval | t _{FrameLock} | — | — | 154 | frames | 1) |

- 1) Defined in FB-DIMM Architecture and Protocol Spec
- 2) Clocks defined as core clocks = 2x SCK input
- 3) @ DDR2-667 - measured from beginning of frame at southbound input to DDR clock output that latches the first command of a frame to the DRAMs
- 4) @ DDR2-667 - measured from latest DQS input to AMB to start of matching data frame at northbound FB-DIMM outputs



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

TABLE 12
Environmental Parameters

| Parameter | Symbol | Rating | Units | Note |
|---|------------------|-------------|-------|------|
| Operating Temperature | T _{OPR} | See Note | | 1) |
| Operating Humidity (relative) | H _{OPR} | 10 to 90 | % | 2) |
| Storage Temperature | T _{STG} | -50 to +100 | °C | 2) |
| Storage Humidity (without condensation) | H _{STG} | 5 to 95 | % | 2) |
| Barometric pressure (operating) | P _{BAR} | 3050 | m | 2) |
| Barometric pressure (storage) | P _{BAR} | 14240 | m | 2) |

- 1) The designer must meet the case temperature specifications for individual module components.
- 2) Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and the device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



5 Current Spec. and Conditions

The following table provides an overview of the measurement conditions.

TABLE 13
 I_{DD} Measurement Conditions

| Parameter | Symbol |
|--|--|
| Idle Current, single or last DIMM L0 state, idle (0 BW) Primary channel enabled, Secondary channel disabled CKE high. Command and address lines stable. DRAM clock active | $I_{CC_Idle_0}$ $I_{DD_Idle_0}$ |
| Idle Current, first DIMM L0 state, idle (0 BW) Primary and Secondary channels enabled. CKE high. Command and address lines stable. DRAM clock active | $I_{CC_Idle_1}$ $I_{DD_Idle_1}$ |
| Active Power L0 state 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high. | $I_{CC_Active_1}$ $I_{DD_Active_1}$ |
| Active Power, data pass through L0 state 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled. CKE high. Command and address lines stable. DRAM clock active. | $I_{CC_Active_2}$ $I_{DD_Active_2}$ |
| Training Primary and Secondary channels enabled. 100% toggle on all channels lanes. DRAMs idle (0 BW). CKE high. Command and address lines stable. DRAM clock active. | $I_{CC_Training}$ $I_{DD_Training}$ |
| IBIST Over all IBIST modes DRAM Idle (0 BW) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active | I_{CC_IBIST} I_{DD_IBIST} |



| Parameter | Symbol |
|---|--|
| MemBIST Over all MemBIST modes >50% DRAM BW (as dictated by the AMB) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active | $I_{CC_MEMBIST}$ $I_{DD_MEMBIST}$ |
| Electrical Idle DRAM Idle (0 BW) Primary channel Disabled Secondary channel Disabled CKE low. Command and Address lines Floated DRAM clock active, ODT and CKE driven low | I_{CC_EI} I_{DD_EI} |

Notes

1. Primary channel Drive strength at 100 % with De-emphasis at -6.5 dB
2. Secondary channel drive strength at 60 % with De-emphasis at -3 dB when enabled.
3. Address and Data fields provide a 50 % toggle rate on DRAM data and link lanes.
4. Burst Length = 4.
5. 10 lanes southbound and 14 lanes northbound are enabled and active (12 lanes NB if non-ECC DIMM).
6. Modeled with 27 Ω termination for command, address, and clocks, and 47 Ω termination for control.
7. Termination is referenced to $V_{TT} = V_{DD} / 2$.



TABLE 14

I_{CC}/I_{DD} Specification for PC2-5300F

| Product Type | HYS72T64400HFN-3S-B | HYS72T128420HFN-3S-B | HYS72T256420HFN-3S-B | Unit | Note |
|---------------|---------------------|----------------------|----------------------|------|------|
| Speed Grade | PC2-5300F | PC2-5300F | PC2-5300F | | |
| Symbol | Max. | Max. | Max. | | |
| ICC_Idle_0 | 2.02 | 2.08 | 2.04 | A | |
| PCC_Idle_0 | 3.07 | 3.16 | 3.09 | W | |
| IDD_Idle_0 | 0.76 | 1.1 | 2.07 | A | |
| PDD_Idle_0 | 1.34 | 1.94 | 3.65 | W | |
| ITOT_Idle_0 | 2.85 | 3.2 | 4.13 | A | |
| PTOT_Idle_0 | 4.47 | 5.12 | 6.76 | W | |
| ICC_Idle_1 | 2.61 | 2.7 | 2.64 | A | |
| PCC_Idle_1 | 3.92 | 4.05 | 3.96 | W | |
| IDD_Idle_1 | 0.76 | 1.09 | 1.96 | A | |
| PDD_Idle_1 | 1.34 | 1.93 | 3.45 | W | |
| ITOT_Idle_1 | 3.44 | 3.83 | 4.62 | A | |
| PTOT_Idle_1 | 5.32 | 6.01 | 7.42 | W | |
| ICC_Active_1 | 2.78 | 2.86 | 2.82 | A | |
| PCC_Active_1 | 4.16 | 4.28 | 4.22 | W | |
| IDD_Active_1 | 1.8 | 2.19 | 3.84 | A | |
| PDD_Active_1 | 3.17 | 3.85 | 6.71 | W | |
| ITOT_Active_1 | 4.63 | 5.05 | 6.69 | A | |
| PTOT_Active_1 | 7.37 | 8.13 | 10.96 | W | |
| ICC_Active_2 | 2.67 | 2.66 | 2.77 | A | |
| PCC_Active_2 | 4 | 3.98 | 4.16 | W | |
| IDD_Active_2 | 0.64 | 0.64 | 1.8 | A | |
| PDD_Active_2 | 1.13 | 1.13 | 3.17 | W | |
| ITOT_Active_2 | 3.41 | 3.37 | 4.65 | A | |
| PTOT_Active_2 | 5.22 | 5.17 | 7.39 | W | |
| ICC_IBIST | 3.61 | 3.74 | 3.65 | A | |
| PCC_IBIST | 5.37 | 5.55 | 5.43 | W | |
| IDD_IBIST | 0.62 | 0.93 | 1.78 | A | |
| PDD_IBIST | 1.09 | 1.65 | 3.15 | W | |
| ITOT_IBIST | 4.3 | 4.72 | 5.45 | A | |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| Product Type | HYS72T64400HFN-3S-B | HYS72T128420HFN-3S-B | HYS72T256420HFN-3S-B | Unit | Note |
|---------------|---------------------|----------------------|----------------------|------|------|
| Speed Grade | PC2-5300F | PC2-5300F | PC2-5300F | | |
| Symbol | Max. | Max. | Max. | | |
| PTOT_IBIST | 6.53 | 7.24 | 8.58 | W | |
| ICC_Training | 3.28 | 3.39 | 3.33 | A | |
| PCC_Training | 4.9 | 5.06 | 4.96 | W | |
| IDD_Trainig | 0.62 | 0.93 | 1.78 | A | |
| PDD_Training | 1.09 | 1.65 | 3.15 | W | |
| ITOT_Trainig | 3.98 | 4.38 | 5.13 | A | |
| PTOT_Training | 6.07 | 6.75 | 8.12 | W | |
| ICC_EI | 1.46 | 1.52 | 1.48 | A | |
| PCC_EI | 2.22 | 2.3 | 2.25 | W | |
| IDD_EI | 0.12 | 0.14 | 0.22 | A | |
| PDD_EI | 0.21 | 0.25 | 0.39 | W | |
| ITOT_EI | 1.62 | 1.72 | 1.83 | A | |
| PTOT_EI | 2.47 | 2.61 | 2.75 | W | |
| ICC_MEMBIST | 2.84 | 2.92 | 2.91 | A | |
| PCC_MEMBIST | 4.25 | 4.37 | 4.35 | W | |
| IDD_MEMBIST | 2.26 | 2.58 | 4.23 | A | |
| PDD_MEMBIST | 3.99 | 4.54 | 7.4 | W | |
| ITOT_MEMBIST | 5.18 | 5.51 | 7.17 | A | |
| PTOT_MEMBIST | 8.31 | 8.92 | 11.77 | W | |



TABLE 15

I_{CC}/I_{DD} Specification for PC2-4200F

| Product Type | HYS72T64400HFN-3.7-B | HYS72T128420HFN-3.7-B | HYS72T256420HFN-3.7-B | Unit | Note |
|---------------|----------------------|-----------------------|-----------------------|------|------|
| Speed Grade | PC2-4200F | PC2-4200F | PC2-4200F | | |
| Symbol | Max. | Max. | Max. | | |
| ICC_Idle_0 | 1.72 | 1.77 | 1.74 | A | |
| PCC_Idle_0 | 2.61 | 2.69 | 2.65 | W | |
| IDD_Idle_0 | 0.72 | 1.02 | 1.93 | A | |
| PDD_Idle_0 | 1.27 | 1.81 | 3.4 | W | |
| ITOT_Idle_0 | 2.48 | 2.81 | 3.69 | A | |
| PTOT_Idle_0 | 3.92 | 4.51 | 6.06 | W | |
| ICC_Idle_1 | 2.24 | 2.3 | 2.27 | A | |
| PCC_Idle_1 | 3.37 | 3.47 | 3.42 | W | |
| IDD_Idle_1 | 0.72 | 1.01 | 1.9 | A | |
| PDD_Idle_1 | 1.27 | 1.79 | 3.35 | W | |
| ITOT_Idle_1 | 3.03 | 3.33 | 4.21 | A | |
| PTOT_Idle_1 | 4.71 | 5.27 | 6.8 | W | |
| ICC_Active_1 | 2.4 | 2.47 | 2.45 | A | |
| PCC_Active_1 | 3.6 | 3.71 | 3.68 | W | |
| IDD_Active_1 | 1.83 | 2.19 | 3.96 | A | |
| PDD_Active_1 | 3.23 | 3.86 | 6.92 | W | |
| ITOT_Active_1 | 4.27 | 4.67 | 6.41 | A | |
| PTOT_Active_1 | 6.88 | 7.57 | 10.6 | W | |
| ICC_Active_2 | 2.28 | 2.28 | 2.39 | A | |
| PCC_Active_2 | 3.44 | 3.44 | 3.59 | W | |
| IDD_Active_2 | 0.6 | 0.6 | 1.84 | A | |
| PDD_Active_2 | 1.05 | 1.05 | 3.24 | W | |
| ITOT_Active_2 | 2.94 | 2.96 | 4.26 | A | |
| PTOT_Active_2 | 4.55 | 4.57 | 6.86 | W | |
| ICC_IBIST | 3.07 | 3.17 | 3.12 | A | |
| PCC_IBIST | 4.6 | 4.74 | 4.67 | W | |
| IDD_IBIST | 0.57 | 0.85 | 1.64 | A | |
| PDD_IBIST | 1.02 | 1.51 | 2.89 | W | |
| ITOT_IBIST | 3.72 | 4.04 | 4.78 | A | |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| Product Type | HYS72T64400HFN-3.7-B | HYS72T128420HFN-3.7-B | HYS72T256420HFN-3.7-B | Unit | Note |
|---------------|----------------------|-----------------------|-----------------------|------|------|
| Speed Grade | PC2-4200F | PC2-4200F | PC2-4200F | | |
| Symbol | Max. | Max. | Max. | | |
| PTOT_IBIST | 5.68 | 6.26 | 7.58 | W | |
| ICC_Training | 2.81 | 2.89 | 2.85 | A | |
| PCC_Training | 4.21 | 4.34 | 4.28 | W | |
| IDD_Trainig | 0.57 | 0.85 | 1.64 | A | |
| PDD_Training | 1.02 | 1.51 | 2.89 | W | |
| ITOT_Trainig | 3.46 | 3.76 | 4.52 | A | |
| PTOT_Training | 5.3 | 5.86 | 7.19 | W | |
| ICC_EI | 1.21 | 1.25 | 1.23 | A | |
| PCC_EI | 1.85 | 1.91 | 1.87 | W | |
| IDD_EI | 0.11 | 0.14 | 0.23 | A | |
| PDD_EI | 0.19 | 0.24 | 0.41 | W | |
| ITOT_EI | 1.37 | 1.45 | 1.59 | A | |
| PTOT_EI | 2.08 | 2.21 | 2.39 | W | |
| ICC_MEMBIST | 2.43 | 2.5 | 2.5 | A | |
| PCC_MEMBIST | 3.65 | 3.76 | 3.76 | W | |
| IDD_MEMBIST | 2.19 | 2.54 | 4.03 | A | |
| PDD_MEMBIST | 3.87 | 4.47 | 7.05 | W | |
| ITOT_MEMBIST | 4.7 | 5.05 | 6.54 | A | |
| PTOT_MEMBIST | 7.59 | 8.24 | 10.82 | W | |



6 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- Table 16 “PC2-5300F-555” on Page 25
- Table 17 “PC2-4200F-444” on Page 30

TABLE 16
PC2-5300F-555

| Product Type | | HYS72T64400HFN-3S-B | HYS72T128420HFN-3S-B | HYS72T256420HFN-3S-B |
|--------------------|--|---------------------|----------------------|----------------------|
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-5300F-555 | PC2-5300F-555 | PC2-5300F-555 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 0 | SPD Size CRC / Total / Used | 92 | 92 | 92 |
| 1 | SPD Revision | 11 | 11 | 11 |
| 2 | Key Byte / DRAM Device Type | 09 | 09 | 09 |
| 3 | Voltage Level of this Assembly | 12 | 12 | 12 |
| 4 | SDRAM Addressing | 44 | 44 | 48 |
| 5 | Module Physical Attributes | 23 | 23 | 23 |
| 6 | Module Type | 07 | 07 | 07 |
| 7 | Module Organization | 09 | 11 | 10 |
| 8 | Fine Timebase (FTB) Dividend and Divisor | 00 | 00 | 00 |
| 9 | Medium Timebase (MTB) Dividend | 01 | 01 | 01 |
| 10 | Medium Timebase (MTB) Divisor | 04 | 04 | 04 |
| 11 | $t_{CK,MIN}$ (min. SDRAM Cycle Time) | 0C | 0C | 0C |
| 12 | $t_{CK,MAX}$ (max. SDRAM Cycle Time) | 20 | 20 | 20 |
| 13 | CAS Latencies Supported | 33 | 33 | 33 |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| Product Type | | HYS72T64400HFN-3S-B | HYS72T128420HFN-3S-B | HYS72T256420HFN-3S-B |
|--------------------|---|---------------------|----------------------|----------------------|
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-5300F-555 | PC2-5300F-555 | PC2-5300F-555 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 14 | $t_{CAS.MIN}$ (min. CAS Latency Time) | 3C | 3C | 3C |
| 15 | Write Recovery Values Supported (WR) | 42 | 42 | 42 |
| 16 | $t_{WR.MIN}$ (Write Recovery Time) | 3C | 3C | 3C |
| 17 | Write Latency Times Supported | 72 | 72 | 72 |
| 18 | Additive Latency Times Supported | 50 | 50 | 50 |
| 19 | $t_{RCD.MIN}$ (min. RAS# to CAS# Delay) | 3C | 3C | 3C |
| 20 | $t_{RRD.MIN}$ (min. Row Active to Row Active Delay) | 1E | 1E | 1E |
| 21 | $t_{RP.MIN}$ (min. Row Precharge Time) | 3C | 3C | 3C |
| 22 | t_{RAS} and t_{RC} Extension | 00 | 00 | 00 |
| 23 | $t_{RAS.MIN}$ (min. Active to Precharge Time) | B4 | B4 | B4 |
| 24 | $t_{RC.MIN}$ (min. Active to Active / Refresh Time) | F0 | F0 | F0 |
| 25 | $t_{RFC.MIN}$ LSB (min. Refresh Recovery Time Delay) | A4 | A4 | A4 |
| 26 | $t_{RFC.MIN}$ MSB (min. Refresh Recovery Time Delay) | 01 | 01 | 01 |
| 27 | $t_{WTR.MIN}$ (min. Internal Write to Read Cmd Delay) | 1E | 1E | 1E |
| 28 | $t_{RTP.MIN}$ (min. Internal Read to Precharge Cmd Delay) | 1E | 1E | 1E |
| 29 | Burst Lengths Supported | 03 | 03 | 03 |
| 30 | Terminations Supported | 07 | 07 | 07 |
| 31 | Drive Strength Supported | 01 | 01 | 01 |
| 32 | t_{REFI} (avg. SDRAM Refresh Period) | C2 | C2 | C2 |
| 33 | $T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta | 50 | 50 | 50 |
| 34 | Psi(T-A) DRAM | 7A | 7A | 7A |
| 35 | ΔT_0 (DT0) DRAM | 48 | 48 | 48 |
| 36 | ΔT_{2Q} (DT2Q) DRAM | 2E | 2E | 2E |
| 37 | ΔT_{2P} (DT2P) DRAM | 36 | 36 | 36 |
| 38 | ΔT_{3N} (DT3N) DRAM | 27 | 27 | 27 |
| 39 | ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W) DRAM | 4C | 4C | 4C |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| Product Type | | HYS72T64400HFN-3S-B | HYS72T128420HFN-3S-B | HYS72T256420HFN-3S-B |
|--------------------|---|---------------------|----------------------|----------------------|
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-5300F-555 | PC2-5300F-555 | PC2-5300F-555 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 40 | ΔT_{5B} (DT5B) DRAM | 20 | 20 | 20 |
| 41 | ΔT_7 (DT7) DRAM | 23 | 23 | 23 |
| 42 - 78 | Not used | 00 | 00 | 00 |
| 79 | FBDIMM ODT Values | 01 | 22 | 22 |
| 80 | Not used | 00 | 00 | 00 |
| 81 | Channel Protocols Supported LSB | 02 | 02 | 02 |
| 82 | Channel Protocols Supported MSB | 00 | 00 | 00 |
| 83 | Back-to-Back Access Turnaround Time | 10 | 10 | 10 |
| 84 | AMB Read Access Delay for DDR2-800 | 56 | 56 | 58 |
| 85 | AMB Read Access Delay for DDR2-667 | 40 | 40 | 42 |
| 86 | AMB Read Access Delay for DDR2-533 | 36 | 36 | 38 |
| 87 | Psi(T-A) AMB | 30 | 30 | 30 |
| 88 | ΔT_{Idle_0} (DT Idle_0) AMB | 60 | 60 | 6A |
| 89 | ΔT_{Idle_1} (DT Idle_1) AMB | 7A | 7A | 84 |
| 90 | ΔT_{Idle_2} (DT Idle_2) AMB | 6E | 6E | 6E |
| 91 | ΔT_{Active_1} (DT Active_1) AMB | A1 | A1 | AF |
| 92 | ΔT_{Active_2} (DT Active_2) AMB | 7F | 7F | 8B |
| 93 | ΔT_{L0s} (DT L0s) AMB | 00 | 00 | 00 |
| 94 - 97 | Not used | 00 | 00 | 00 |
| 98 | AMB Junction Temperature Maximum (T_{jmax}) | 00 | 00 | 00 |
| 99 | Category Byte | 0A | 0A | 0A |
| 100 | Not used | 00 | 00 | 00 |
| 101 | AMB Personality Bytes: Pre-initialization (1) | 80 | 80 | 80 |
| 102 | AMB Personality Bytes: Pre-initialization (2) | 20 | 20 | 20 |
| 103 | AMB Personality Bytes: Pre-initialization (3) | 00 | 00 | 00 |
| 104 | AMB Personality Bytes: Pre-initialization (4) | 44 | 44 | 44 |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| Product Type | | HYS72T64400HFN-3S-B | HYS72T128420HFN-3S-B | HYS72T256420HFN-3S-B |
|--------------------|--|---------------------|----------------------|----------------------|
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-5300F-555 | PC2-5300F-555 | PC2-5300F-555 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 105 | AMB Personality Bytes: Pre-initialization (5) | 04 | 04 | 04 |
| 106 | AMB Personality Bytes: Pre-initialization (6) | 80 | 80 | 80 |
| 107 | AMB Personality Bytes: Post-initialization (1) | 48 | 48 | 48 |
| 108 | AMB Personality Bytes: Post-initialization (2) | 53 | 53 | 53 |
| 109 | AMB Personality Bytes: Post-initialization (3) | B3 | B3 | B1 |
| 110 | AMB Personality Bytes: Post-initialization (4) | 43 | 43 | 43 |
| 111 | AMB Personality Bytes: Post-initialization (5) | 65 | 65 | 65 |
| 112 | AMB Personality Bytes: Post-initialization (6) | 4C | 4C | 4C |
| 113 | AMB Personality Bytes: Post-initialization (7) | 00 | 00 | 00 |
| 114 | AMB Personality Bytes: Post-initialization (8) | 10 | 10 | 10 |
| 115 | AMB Manufacturers JEDEC ID Code LSB | 80 | 80 | 80 |
| 116 | AMB Manufacturers JEDEC ID Code MSB | 89 | 89 | 89 |
| 117 | DIMM Manufacturers JEDEC ID Code LSB | 85 | 85 | 85 |
| 118 | DIMM Manufacturers JEDEC ID Code MSB | 51 | 51 | 51 |
| 119 | Module Manufacturing Location | xx | xx | xx |
| 120 | Module Manufacturing Date Year | xx | xx | xx |
| 121 | Module Manufacturing Date Week | xx | xx | xx |
| 122 - 125 | Module Serial Number | xx | xx | xx |
| 126 | Cyclical Redundancy Code LSB | 20 | 1C | EA |
| 127 | Cyclical Redundancy Code MSB | 42 | 4A | CB |
| 128 | Module Product Type, Char #1 | 37 | 37 | 37 |
| 129 | Module Product Type, Char #2 | 32 | 32 | 32 |
| 130 | Module Product Type, Char #3 | 54 | 54 | 54 |
| 131 | Module Product Type, Char #4 | 36 | 31 | 32 |
| 132 | Module Product Type, Char #5 | 34 | 32 | 35 |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| | | | | |
|---------------------------|---|----------------------------|-----------------------------|-----------------------------|
| Product Type | | HYS72T64400HFN-3S-B | HYS72T128420HFN-3S-B | HYS72T256420HFN-3S-B |
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-5300F-555 | PC2-5300F-555 | PC2-5300F-555 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 133 | Module Product Type, Char #6 | 34 | 38 | 36 |
| 134 | Module Product Type, Char #7 | 30 | 34 | 34 |
| 135 | Module Product Type, Char #8 | 30 | 32 | 32 |
| 136 | Module Product Type, Char #9 | 48 | 30 | 30 |
| 137 | Module Product Type, Char #10 | 46 | 48 | 48 |
| 138 | Module Product Type, Char #11 | 4E | 46 | 46 |
| 139 | Module Product Type, Char #12 | 33 | 4E | 4E |
| 140 | Module Product Type, Char #13 | 53 | 33 | 33 |
| 141 | Module Product Type, Char #14 | 42 | 53 | 53 |
| 142 | Module Product Type, Char #15 | 20 | 42 | 42 |
| 143 | Module Product Type, Char #16 | 20 | 20 | 20 |
| 144 | Module Product Type, Char #17 | 20 | 20 | 20 |
| 145 | Module Product Type, Char #18 | 20 | 20 | 20 |
| 146 | Module Revision Code | 9x | 9x | 9x |
| 147 | Test Program Revision Code | xx | xx | xx |
| 148 | DRAM Manufacturers JEDEC ID Code LSB | 85 | 85 | 85 |
| 149 | DRAM Manufacturers JEDEC ID Code MSB | 51 | 51 | 51 |
| 150 | informal AMB content revision tag (MSB) | 01 | 01 | 01 |
| 151 | informal AMB content revision tag (LSB) | 09 | 09 | 09 |
| 152 - 175 | Not used | 00 | 00 | 00 |
| 176 - 255 | Blank for customer use | FF | FF | FF |



TABLE 17
PC2-4200F-444

| Product Type | | HYS72T64400HFN-3.7-B | HYS72T128420HFN-3.7-B | HYS72T256420HFN-3.7-B |
|--------------------|---|----------------------|-----------------------|-----------------------|
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-4200F-444 | PC2-4200F-444 | PC2-4200F-444 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 0 | SPD Size CRC / Total / Used | 92 | 92 | 92 |
| 1 | SPD Revision | 11 | 11 | 11 |
| 2 | Key Byte / DRAM Device Type | 09 | 09 | 09 |
| 3 | Voltage Level of this Assembly | 12 | 12 | 12 |
| 4 | SDRAM Addressing | 44 | 44 | 48 |
| 5 | Module Physical Attributes | 23 | 23 | 23 |
| 6 | Module Type | 07 | 07 | 07 |
| 7 | Module Organization | 09 | 11 | 10 |
| 8 | Fine Timebase (FTB) Dividend and Divisor | 00 | 00 | 00 |
| 9 | Medium Timebase (MTB) Dividend | 01 | 01 | 01 |
| 10 | Medium Timebase (MTB) Divisor | 04 | 04 | 04 |
| 11 | $t_{CK,MIN}$ (min. SDRAM Cycle Time) | 0F | 0F | 0F |
| 12 | $t_{CK,MAX}$ (max. SDRAM Cycle Time) | 20 | 20 | 20 |
| 13 | CAS Latencies Supported | 33 | 33 | 33 |
| 14 | $t_{CAS,MIN}$ (min. CAS Latency Time) | 3C | 3C | 3C |
| 15 | Write Recovery Values Supported (WR) | 32 | 32 | 32 |
| 16 | $t_{WR,MIN}$ (Write Recovery Time) | 3C | 3C | 3C |
| 17 | Write Latency Times Supported | 72 | 72 | 72 |
| 18 | Additive Latency Times Supported | 50 | 50 | 50 |
| 19 | $t_{RCD,MIN}$ (min. RAS# to CAS# Delay) | 3C | 3C | 3C |
| 20 | $t_{RRD,MIN}$ (min. Row Active to Row Active Delay) | 1E | 1E | 1E |
| 21 | $t_{RP,MIN}$ (min. Row Precharge Time) | 3C | 3C | 3C |
| 22 | t_{RAS} and t_{RC} Extension | 00 | 00 | 00 |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| Product Type | | HYS72T64400HFN-3.7-B | HYS72T128420HFN-3.7-B | HYS72T256420HFN-3.7-B |
|--------------------|---|----------------------|-----------------------|-----------------------|
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-4200F-444 | PC2-4200F-444 | PC2-4200F-444 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 23 | $t_{RAS,MIN}$ (min. Active to Precharge Time) | B4 | B4 | B4 |
| 24 | $t_{RC,MIN}$ (min. Active to Active / Refresh Time) | F0 | F0 | F0 |
| 25 | $t_{RFC,MIN}$ LSB (min. Refresh Recovery Time Delay) | A4 | A4 | A4 |
| 26 | $t_{RFC,MIN}$ MSB (min. Refresh Recovery Time Delay) | 01 | 01 | 01 |
| 27 | $t_{WTR,MIN}$ (min. Internal Write to Read Cmd Delay) | 1E | 1E | 1E |
| 28 | $t_{RTP,MIN}$ (min. Internal Read to Precharge Cmd Delay) | 1E | 1E | 1E |
| 29 | Burst Lengths Supported | 03 | 03 | 03 |
| 30 | Terminations Supported | 07 | 07 | 07 |
| 31 | Drive Strength Supported | 01 | 01 | 01 |
| 32 | t_{REFI} (avg. SDRAM Refresh Period) | C2 | C2 | C2 |
| 33 | $T_{CASE,MAX}$ Delta / ΔT_{4R4W} Delta | 50 | 50 | 50 |
| 34 | Psi(T-A) DRAM | 7A | 7A | 7A |
| 35 | ΔT_0 (DT0) DRAM | 40 | 40 | 40 |
| 36 | ΔT_{2Q} (DT2Q) DRAM | 29 | 29 | 29 |
| 37 | ΔT_{2P} (DT2P) DRAM | 36 | 36 | 36 |
| 38 | ΔT_{3N} (DT3N) DRAM | 21 | 21 | 21 |
| 39 | ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W) DRAM | 40 | 40 | 40 |
| 40 | ΔT_{5B} (DT5B) DRAM | 1E | 1E | 1E |
| 41 | ΔT_7 (DT7) DRAM | 22 | 22 | 22 |
| 42 - 78 | Not used | 00 | 00 | 00 |
| 79 | FBDIMM ODT Values | 01 | 22 | 22 |
| 80 | Not used | 00 | 00 | 00 |
| 81 | Channel Protocols Supported LSB | 02 | 02 | 02 |
| 82 | Channel Protocols Supported MSB | 00 | 00 | 00 |
| 83 | Back-to-Back Access Turnaround Time | 10 | 10 | 10 |
| 84 | AMB Read Access Delay for DDR2-800 | 56 | 56 | 58 |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| | | | | |
|---------------------------|---|-----------------------------|------------------------------|------------------------------|
| Product Type | | HYS72T64400HFN-3.7-B | HYS72T128420HFN-3.7-B | HYS72T256420HFN-3.7-B |
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-4200F-444 | PC2-4200F-444 | PC2-4200F-444 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 85 | AMB Read Access Delay for DDR2-667 | 40 | 40 | 42 |
| 86 | AMB Read Access Delay for DDR2-533 | 36 | 36 | 38 |
| 87 | Psi(T-A) AMB | 30 | 30 | 30 |
| 88 | ΔT_{Idle_0} (DT Idle_0) AMB | 52 | 52 | 5B |
| 89 | ΔT_{Idle_1} (DT Idle_1) AMB | 66 | 66 | 71 |
| 90 | ΔT_{Idle_2} (DT Idle_2) AMB | 60 | 60 | 60 |
| 91 | ΔT_{Active_1} (DT Active_1) AMB | 84 | 84 | 92 |
| 92 | ΔT_{Active_2} (DT Active_2) AMB | 6A | 6A | 71 |
| 93 | ΔT_{LOs} (DT L0s) AMB | 00 | 00 | 00 |
| 94 - 97 | Not used | 00 | 00 | 00 |
| 98 | AMB Junction Temperature Maximum (T_{jmax}) | 00 | 00 | 00 |
| 99 | Category Byte | 0A | 0A | 0A |
| 100 | Not used | 00 | 00 | 00 |
| 101 | AMB Personality Bytes: Pre-initialization (1) | 80 | 80 | 80 |
| 102 | AMB Personality Bytes: Pre-initialization (2) | 20 | 20 | 20 |
| 103 | AMB Personality Bytes: Pre-initialization (3) | 00 | 00 | 00 |
| 104 | AMB Personality Bytes: Pre-initialization (4) | 44 | 44 | 44 |
| 105 | AMB Personality Bytes: Pre-initialization (5) | 04 | 04 | 04 |
| 106 | AMB Personality Bytes: Pre-initialization (6) | 80 | 80 | 80 |
| 107 | AMB Personality Bytes: Post-initialization (1) | 48 | 48 | 48 |
| 108 | AMB Personality Bytes: Post-initialization (2) | 53 | 53 | 53 |
| 109 | AMB Personality Bytes: Post-initialization (3) | B3 | B3 | B1 |
| 110 | AMB Personality Bytes: Post-initialization (4) | 43 | 43 | 43 |
| 111 | AMB Personality Bytes: Post-initialization (5) | 65 | 65 | 65 |
| 112 | AMB Personality Bytes: Post-initialization (6) | 4C | 4C | 4C |
| 113 | AMB Personality Bytes: Post-initialization (7) | 00 | 00 | 00 |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| | | | | |
|---------------------------|--|-----------------------------|------------------------------|------------------------------|
| Product Type | | HYS72T64400HFN-3.7-B | HYS72T128420HFN-3.7-B | HYS72T256420HFN-3.7-B |
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-4200F-444 | PC2-4200F-444 | PC2-4200F-444 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 114 | AMB Personality Bytes: Post-initialization (8) | 10 | 10 | 10 |
| 115 | AMB Manufacturers JEDEC ID Code LSB | 80 | 80 | 80 |
| 116 | AMB Manufacturers JEDEC ID Code MSB | 89 | 89 | 89 |
| 117 | DIMM Manufacturers JEDEC ID Code LSB | 85 | 85 | 85 |
| 118 | DIMM Manufacturers JEDEC ID Code MSB | 51 | 51 | 51 |
| 119 | Module Manufacturing Location | xx | xx | xx |
| 120 | Module Manufacturing Date Year | xx | xx | xx |
| 121 | Module Manufacturing Date Week | xx | xx | xx |
| 122 - 125 | Module Serial Number | xx | xx | xx |
| 126 | Cyclical Redundancy Code LSB | FC | C0 | F6 |
| 127 | Cyclical Redundancy Code MSB | 7C | 74 | ED |
| 128 | Module Product Type, Char #1 | 37 | 37 | 37 |
| 129 | Module Product Type, Char #2 | 32 | 32 | 32 |
| 130 | Module Product Type, Char #3 | 54 | 54 | 54 |
| 131 | Module Product Type, Char #4 | 36 | 31 | 32 |
| 132 | Module Product Type, Char #5 | 34 | 32 | 35 |
| 133 | Module Product Type, Char #6 | 34 | 38 | 36 |
| 134 | Module Product Type, Char #7 | 30 | 34 | 34 |
| 135 | Module Product Type, Char #8 | 30 | 32 | 32 |
| 136 | Module Product Type, Char #9 | 48 | 30 | 30 |
| 137 | Module Product Type, Char #10 | 46 | 48 | 48 |
| 138 | Module Product Type, Char #11 | 4E | 46 | 46 |
| 139 | Module Product Type, Char #12 | 33 | 4E | 4E |
| 140 | Module Product Type, Char #13 | 2E | 33 | 33 |
| 141 | Module Product Type, Char #14 | 37 | 2E | 2E |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| | | | | |
|---------------------------|---|-----------------------------|------------------------------|------------------------------|
| Product Type | | HYS72T64400HFN-3.7-B | HYS72T128420HFN-3.7-B | HYS72T256420HFN-3.7-B |
| Organization | | 512MB | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC2-4200F-444 | PC2-4200F-444 | PC2-4200F-444 |
| JEDEC SPD Revision | | Rev. 1.1 | Rev. 1.1 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX |
| 142 | Module Product Type, Char #15 | 42 | 37 | 37 |
| 143 | Module Product Type, Char #16 | 20 | 42 | 42 |
| 144 | Module Product Type, Char #17 | 20 | 20 | 20 |
| 145 | Module Product Type, Char #18 | 20 | 20 | 20 |
| 146 | Module Revision Code | 7x | 7x | 7x |
| 147 | Test Program Revision Code | xx | xx | xx |
| 148 | DRAM Manufacturers JEDEC ID Code LSB | 85 | 85 | 85 |
| 149 | DRAM Manufacturers JEDEC ID Code MSB | 51 | 51 | 51 |
| 150 | informal AMB content revision tag (MSB) | 01 | 01 | 01 |
| 151 | informal AMB content revision tag (LSB) | 09 | 09 | 09 |
| 152 - 175 | Not used | 00 | 00 | 00 |
| 176 - 255 | Blank for customer use | FF | FF | FF |



7 Package Outline

All Components are surface mounted on one or both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR2 SDRAM signals. Bypass capacitors for DDR2 SDRAM devices are located

near the device power pins. The AMB device in the center of the DIMM has a metal Heat Sink. The FB-DIMM mechanical outlines are consistent with JEDEC MO-256.

TABLE 18
Raw Card Reference

| JEDEC Raw Card | Infineon PCB | | Dimensions | | | |
|----------------|--------------|-----------------|------------|-------------|----------------|-------|
| | | | Width [mm] | Height [mm] | Thickness [mm] | Notes |
| R/C A | L-DIM-240-21 | Figure 4 | 133.35 | 30.35 | 8.2 | 1) |
| R/C B | L-DIM-240-22 | Figure 5 | 133.35 | 30.35 | 8.2 | 1) |
| R/C H | L-DIM-240-25 | Figure 6 | 133.35 | 30.35 | 8.2 | 1) |

1) Thickness includes Infineon Heat Sink. Some early production modules with Jedec Heatspreader may be thicker up to 8.2mm.

Attention: Heat Sink heat up during operation. When unplugging a DIMM from a system direct skin contact should be avoided until the Heat Sink has reached room temperature.

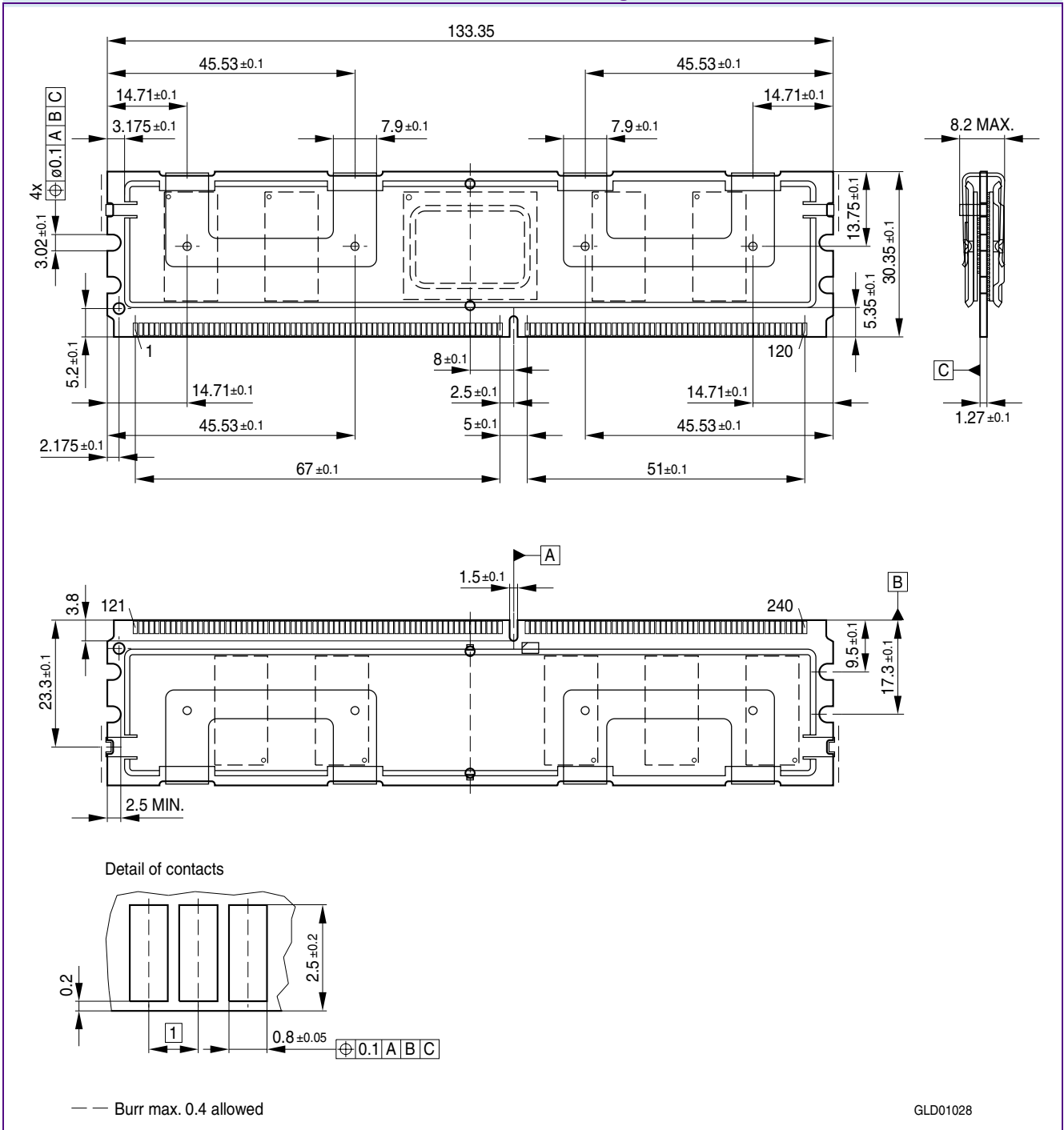
Attention: The Heat Sink is mechanically loaded. Do not remove. Removal of the clip may cause injuries.

Attention: Any mechanical stress on the Heat Sink should be avoided. Touching the Heat Sink while plugging or unplugging the module may permanently damage the DIMM.



FIGURE 4

Package Outline L-DIM-240-21 with Full Heat Sink



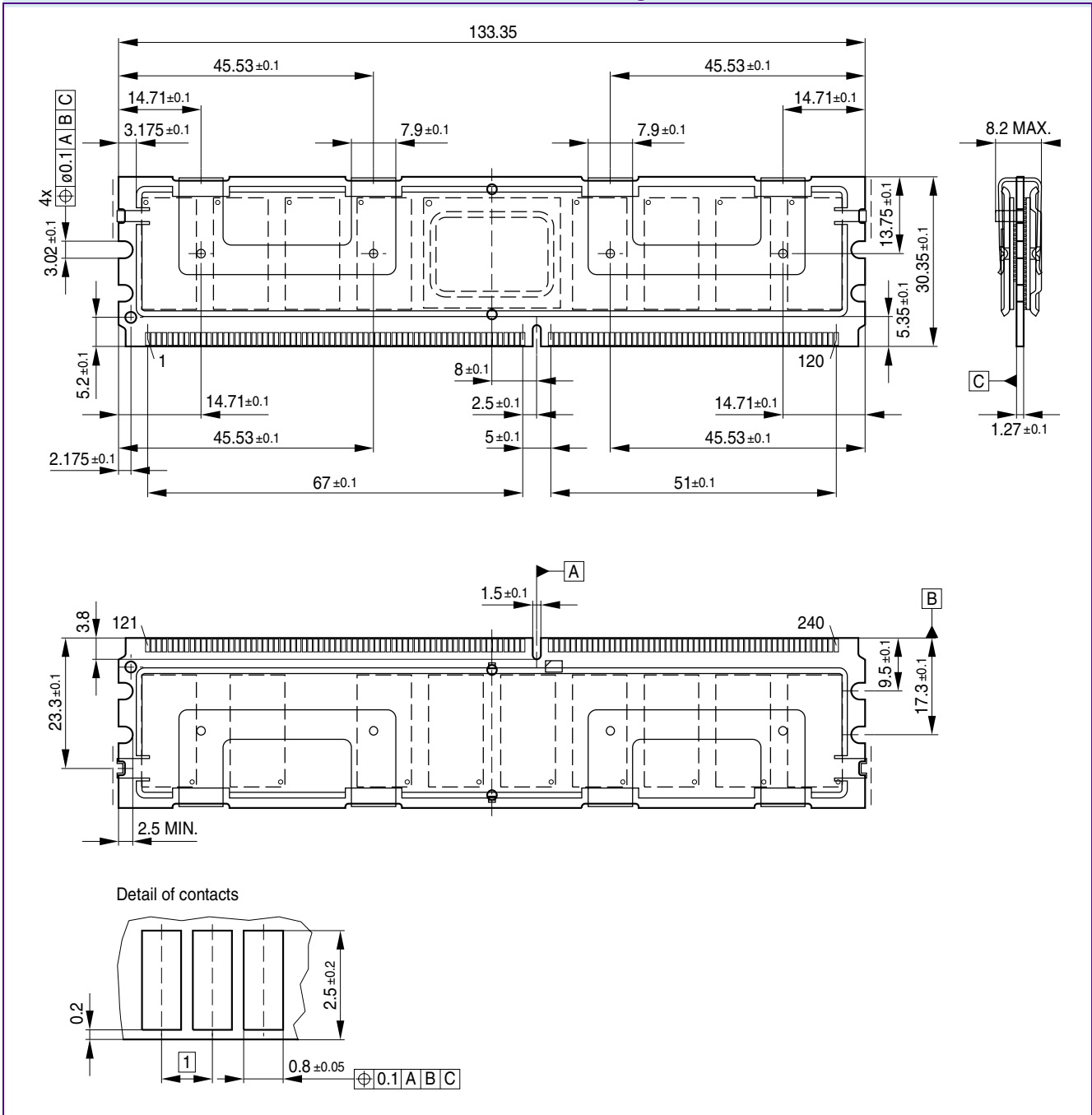
Notes

1. Please contact your sales or marketing representative for more details on package dimensions.
2. General tolerances +/- 0.15
3. Drawing according to ISO 8015



FIGURE 5

Package Outline L-DIM-240-22 with Full Heat Sink

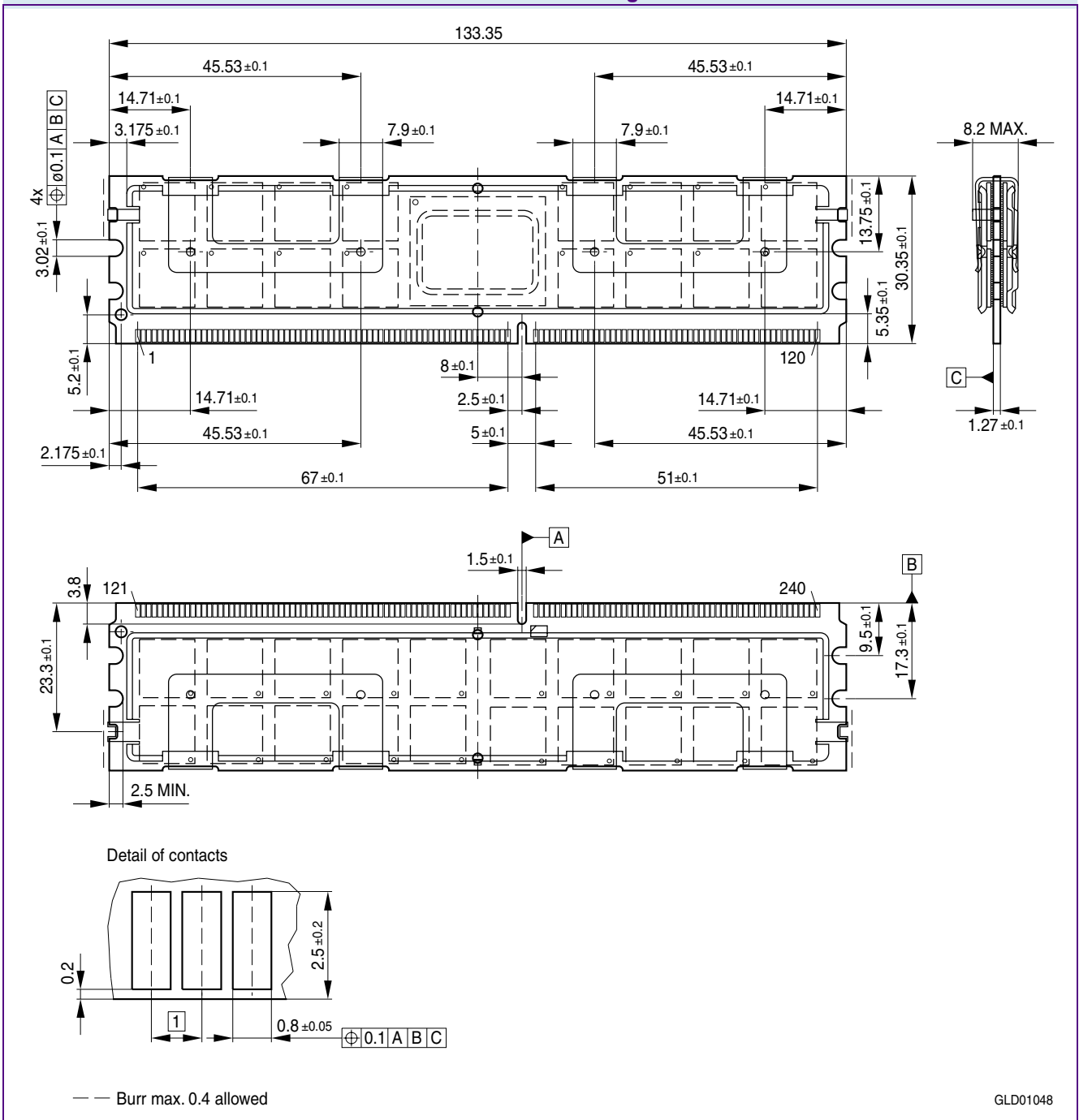


Notes

1. Please contact your sales or marketing representative for more details on package dimensions.
2. General tolerances +/- 0.15
3. Drawing according to ISO 8015



FIGURE 6
Package Outline L-DIM-240-25 with Full Heat Sink



GLD01048

Notes

1. Please contact your sales or marketing representative for more details on package dimensions.
2. General tolerances +/- 0.15
3. Drawing according to ISO 8015



8 DDR2 Nomenclature

TABLE 19
Nomenclature Fields and Examples

| Example for | Field Number | | | | | | | | | | |
|-------------|--------------|----|---|-------|----|---|---|---|---|----|----|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| Micro-DIMM | HYS | 64 | T | 64128 | 0 | 2 | 0 | K | M | -5 | -A |
| DDR2 DRAM | HYB | 18 | T | 5121G | 16 | | 0 | A | C | -5 | |

TABLE 20
DDR2 DIMM Nomenclature

| Field | Description | Values | Coding |
|-------|--|---------|----------------|
| 1 | Qimonda Module Prefix | HYS | Constant |
| 2 | Module Data Width [bit] | 64 | Non-ECC |
| | | 72 | ECC |
| 3 | DRAM Technology | T | DDR2 |
| 4 | Memory Density per I/O [Mbit]; Module Density ¹⁾ | 32 | 256 MByte |
| | | 64 | 512 MByte |
| | | 128 | 1 GByte |
| | | 256 | 2 GByte |
| | | 512 | 4 GByte |
| 5 | Raw Card Generation | 0 .. 9 | Look up table |
| 6 | Number of Module Ranks | 0, 2, 4 | 1, 2, 4 |
| 7 | Product Variations | 0 .. 9 | Look up table |
| 8 | Package, Lead-Free Status | A .. Z | Look up table |
| 9 | Module Type | D | SO-DIMM |
| | | M | Micro-DIMM |
| | | R | Registered |
| | | U | Unbuffered |
| | | F | Fully Buffered |
| 10 | Speed Grade | -2.5 | PC2-6400 6-6-6 |
| | | -3 | PC2-5300 4-4-4 |
| | | -3S | PC2-5300 5-5-5 |
| | | -3.7 | PC2-4200 4-4-4 |
| | | -5 | PC2-3200 3-3-3 |



HYS72T[64/128/256]4[00/20]HFN-[3S/3.7]-B

| Field | Description | Values | Coding |
|-------|--------------|--------|--------|
| 11 | Die Revision | -A | First |
| | | -B | Second |

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

TABLE 21
DDR2 DRAM Nomenclature

| Field | Description | Values | Coding |
|-------|---------------------------|--------|-----------------------|
| 1 | Qimonda Component Prefix | HYB | Constant |
| 2 | Interface Voltage [V] | 18 | SSTL_18 |
| 3 | DRAM Technology | T | DDR2 |
| 4 | Component Density [Mbit] | 256 | 256 Mbit |
| | | 512 | 512 Mbit |
| | | 1G | 1 Gbit |
| | | 2G | 2 Gbit |
| 5+6 | Number of I/Os | 40 | ×4 |
| | | 80 | ×8 |
| | | 16 | ×16 |
| 7 | Product Variations | 0 .. 9 | Look up table |
| 8 | Die Revision | A | First |
| | | B | Second |
| 9 | Package, Lead-Free Status | C | FBGA, lead-containing |
| | | F | FBGA, lead-free |
| 10 | Speed Grade | -2.5 | DDR2-800 6-6-6 |
| | | -3 | DDR2-667 4-4-4 |
| | | -3S | DDR2-667 5-5-5 |
| | | -3.7 | DDR2-533 4-4-4 |
| | | -5 | DDR2-400 3-3-3 |



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