LD6805 series

Low-dropout regulators, low noise, 150 mA

Rev. 1 — 22 September 2011 Objective data sheet

1. Product profile

1.1 General description

The LD6805 series is a small-size Low-DropOut regulator (LDO) family with ultra high Power Supply Rejection Ratio (PSRR) of 75 dB and a voltage drop of 250 mV at 150 mA current rating.

The devices are available in a HUSON4 QFN plastic package.

The operating voltage ranges from 2.3 V to 5.5 V and the output voltage ranges from 1.2 V to 3.6 V. All devices use the same regulator design and are manufactured in monolithic silicon technology.

These features make the LD6805 series ideal for use in applications requiring component miniaturization, such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features and benefits

- Input voltage range 2.3 V to 5.5 V
- Output voltage range 1.2 V to 3.6 V
- Dropout voltage 250 mV at 150 mA output rating
- Low quiescent current in shutdown mode (typical 0.1 μA)
- 40 μV RMS output noise voltage (typical value) at 10 Hz to 100 kHz
- Turn-on time 200 μs
- 75 dB PSRR at 1 kHz
- LD6805K/xxH: high-ohmic (3-state) output state when disabled
- LD6805K/xxP: low-ohmic output state when disabled
- Integrated ESD protection of 6 kV Human Body Model
- HUSON4 QFN plastic package
- Pb-free, RoHS compliant and free of Halogen and Antimony (dark green compliant)

1.3 Applications

- Analog and digital interfaces requiring lower than standard supply voltage in mobile appliances such as mobile phones, media players and so on.

2. Pinning information

2.1 Pinning

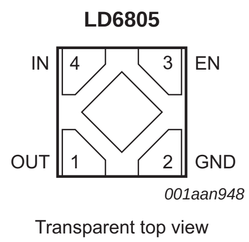


Fig 1. Pin configuration for HUSON4

2.2 Pin description

Table 1. Pin description HUSON4

Symbol	Pin	Description
OUT	1	regulator output voltage
GND	2	supply ground
EN	3	device enable input; active HIGH
IN	4	regulator input voltage
i.c.	TAB	internal connected[1]

[1] The TAB is GND level (It is placed on the reverse side of the IC). The TAB should be connected to the GND, but leaving open is also allowed.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
LD6805K/xxH	HUSON4	plastic thermal enhanced ultra thin small outline package; no leads; 4 terminals; body 1 × 1 × 0.55 mm	SOT1194-1
LD6805K/xxP	HUSON4	plastic thermal enhanced ultra thin small outline package; no leads; 4 terminals; body 1 × 1 × 0.55 mm	SOT1194-1

3.1 Ordering options

Further information on output voltage is available on request; see Section 19 "Contact information"

Table 3. Type number extension of high ohmic output

Type number	Nominal output voltage	Type number	Nominal output voltage
LD6805K/12H	1.2 V	LD6805K/23H	2.3 V
LD6805K/13H	1.3 V	LD6805K/25H	2.5 V
LD6805K/14H	1.4 V	LD6805K/28H	2.8 V
LD6805K/16H	1.6 V	LD6805K/29H	2.9 V
LD6805K/18H	1.8 V	LD6805K/30H	3.0 V
LD6805K/20H	2.0 V	LD6805K/33H	3.3 V
LD6805K/22H	2.2 V	LD6805K/36H	3.6 V

Table 4. Type number extension of pull-down output

Type number	Nominal output voltage	Type number	Nominal output voltage
LD6805K/12P	1.2 V	LD6805K/23P	2.3 V
LD6805K/13P	1.3 V	LD6805K/25P	2.5 V
LD6805K/14P	1.4 V	LD6805K/28P	2.8 V
LD6805K/16P	1.6 V	LD6805K/29P	2.9 V
LD6805K/18P	1.8 V	LD6805K/30P	3.0 V
LD6805K/20P	2.0 V	LD6805K/33P	3.3 V
LD6805K/22P	2.2 V	LD6805K/36P	3.6 V

4. Block diagram

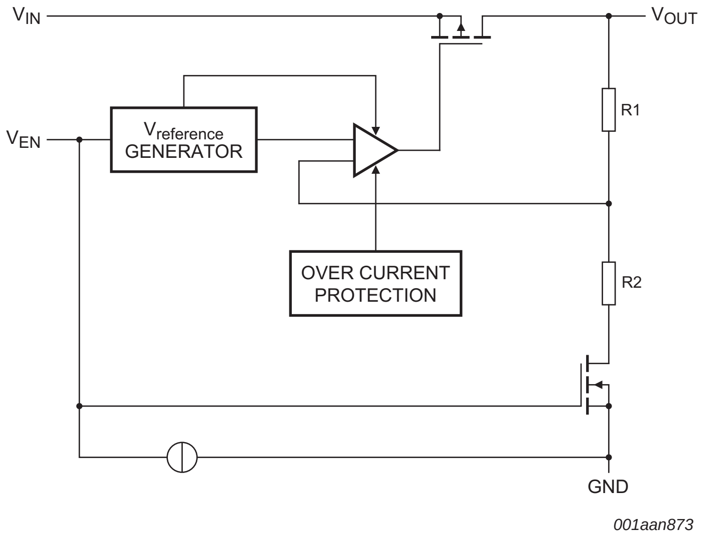


Fig 2. Block diagram of LD6805KxxH

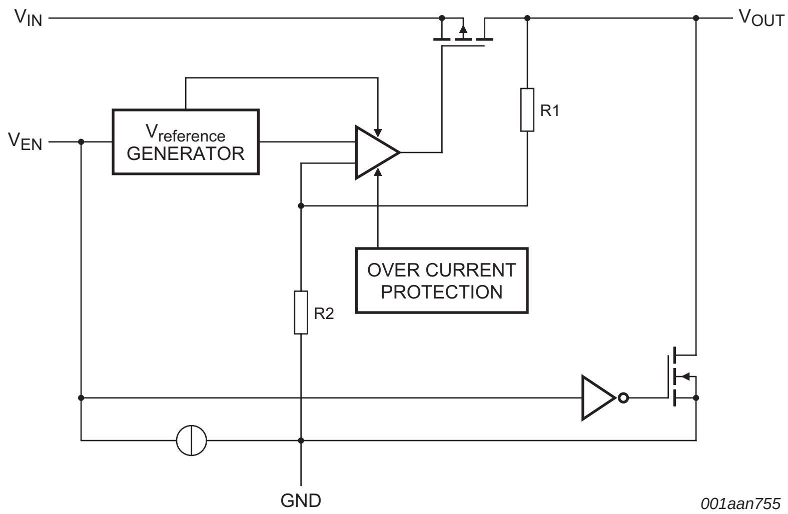


Fig 3. Block diagram of LD6805KxxP

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IN}	voltage on pin IN	4 ms transient		–0.5	+6.0	V
P_{tot}	total power dissipation		[1]	-	400	mW
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–40	+125	°C
T_{amb}	ambient temperature			–40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model level 6	[2]		±6	kV
		machine model class 3	[3]	-	±400	V

[1] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two layer PCB.

[2] According to IEC 61340-3-1.

[3] According to JESD22-A115C.

6. Recommended operating conditions

Table 6. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			-	+125	°C
Pin IN						
V_{IN}	voltage on pin IN			2.3	5.5	V
Pin EN						
V_{EN}	voltage on pin EN			0	V_{IN}	V
Pin OUT						
$C_{L(ext)}$	external load capacitance		[1]	1.0	-	µF

[1] See Section 10.1 “Output capacitor values”.

7. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	250	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas for example to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area directly below the LDO. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Avoid the use of solder-stop varnish under the chip

[2] Use the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value can vary in applications using different layer stacks and layouts.

8. Characteristics

Table 8. Electrical characteristics

At recommended input voltages and T_{amb} = −40 to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔV_O	output voltage variation	V_{OUT} < 1.8 V; I_{OUT} = 1 mA					
		Tamb = +25 °C		−3	-	+3	%
		−30 °C ≤ Tamb ≤ +85 °C		−4	-	+4	%
		V_{OUT} ≥ 1.8 V; I_{OUT} = 1 mA					
		Tamb = +25 °C		−2	-	+2	%
		−30 °C ≤ Tamb ≤ +85 °C		−3	-	+3	%
Line regulation error							
$\Delta V_O/(V_O \times \Delta V_I)$	relative output voltage variation with input voltage	V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V		−0.1	-	+0.1	%/V
Load regulation error							
$\Delta ς_O/(ς_O \times \Delta I_O)$	relative output voltage variation with output current	1 mA ≤ IOUT ≤ 150 mA			0.0025	0.01	%/mA
V_{do}	dropout voltage	I_{OUT} = 150 mA; V_{IN} < $V_{O(nom)}$	[1]	-	250	-	mV
V_{IL}	LOW-level input voltage	pin EN		0	-	0.4	V
V_{IH}	HIGH-level input voltage	pin EN		1.1	-	5.5	V
I_{OUT}	current on pin OUT			-	-	150	mA
I_{OM}	peak output current	VIN = (VO(nom) + 0.5 V) to 5.5 V	[1]				
		$V_{O(nom)}$ > 1.8 V; VOUT = 0.95 × VO(nom)		200	-	-	mA
		$V_{O(nom)}$ < 1.8 V; VOUT = 0.9 × VO(nom)		200	-	-	mA
I_{sc}	short-circuit current	pin OUT		-	300	-	mA
I_q	quiescent current	VEN = 1.1 V; IOUT = 0 mA		-	35	-	μA
		VEN = 1.1 V; 1 mA ≤ IOUT ≤ 150 mA		-	150	-	μA
		VEN ≤ 0.4 V		-	0.1	1	μA
PSRR	power supply rejection ratio	V_{IN} = VO(nom) + 1.0 V; IOUT = 50 mA; f_{ripple} = 1 kHz	[1]	-	−75	-	dB
$V_{n(o)(RMS)}$	RMS output noise voltage	f_{ripple} = 10 Hz to 100 kHz; CL(ext) = 1 mF		-	40	-	mV
$t_{startup(reg)}$	regulator start-up time	V_{IN} = 5.5 V; V_{OUT} = 0.95 × VO(nom); I_{OUT} = 150 mA; C_L = 1 μF	[1]	-	-	200	μs
$t_{sd(reg)}$	regulator shutdown time	V_{IN} = 5.5 V; $C_{L(ext)}$ = 1 μF	[2]	-	150	-	μs
Rpd	pull-down resistance		[2]	-	100	-	Ω

[1] $V_{O(nom)}$ = nominal output voltage (device specific).

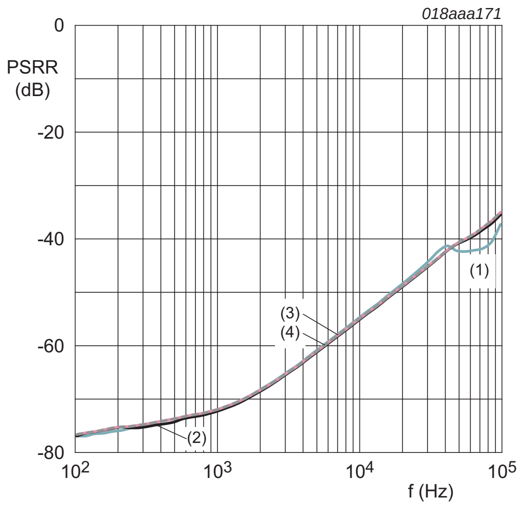
[2] LD6805KxxP only.

9. Dynamic behavior

9.1 Power Supply Rejection Ratio (PSRR)

PSRR stands for the capability of the regulator to suppress unwanted signals on the input voltage like noise or ripples.

$$PSRR[dB] = 20log\frac{V_{out(ripple)}}{V_{in(ripple)}} \text{ for all frequencies}$$



(1) 1 mA.

(2) 50 mA.

(3) 100 mA.

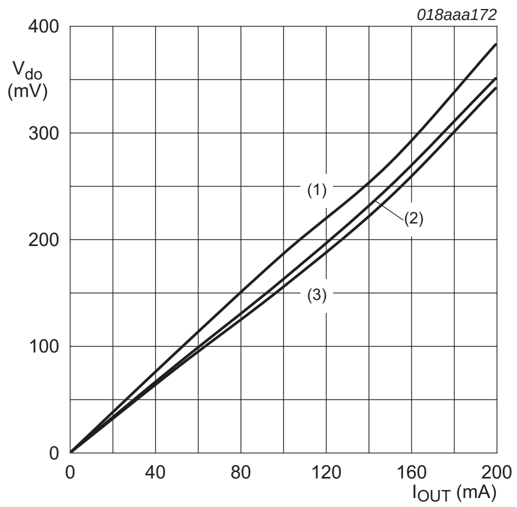
(4) 200 mA.

Fig 4. PSSR for LD6805K/18P

9.2 Dropout

The dropout voltage is defined as the smallest input to output voltage difference at a specified load current when the regulator operates within its linear region with the pass transistor functioning as a plain resistor. This means that the input voltage is below the nominal output voltage value.

A small dropout voltage guaranties lower power consumption and efficiency maximization.



(1) +85 °C

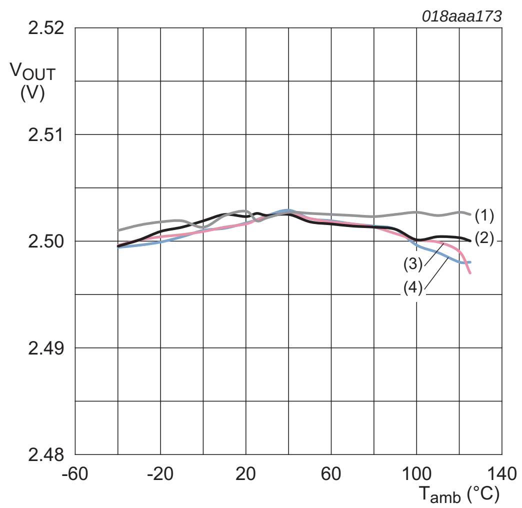
(2) +25 °C

(3) –40 °C

Fig 5. Dropout voltage as a function of temperature for LD6805K/25P

9.3 Accuracy

The LD6805 series guarantees high accuracy of the nominal output voltage.



(1) I_{OUT} = 1 mA

(2) I_{OUT} = 100 mA

(3) I_{OUT} = 150 mA

(4) I_{OUT} = 200 mA

Fig 6. Accuracy for LD6805K/25P

10. Application information

10.1 Output capacitor values

The LD6805 series requires external capacitors at the output to guarantee a stable regulator behavior. Also an input capacitor is recommended to keep the input voltage stable. These capacitors should not under-run the specified minimum Equivalent Series Resistance (ESR).

The absolute value of the total capacitance attached to the output pin OUT influences the shutdown time ($t_{sd(reg)}$) of the LD6805 series.

Table 9. External load capacitor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{L(ext)}$	external load capacitance	[1]	-	1.0	-	μF
ESR	equivalent series resistance		5	-	500	mΩ

[1] The minimum value of capacitance for stability and correct operation is 0.7 μF. The capacitor tolerance should be ±30 % or better over the temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure that this minimum capacitance specification is met. The recommended capacitor type is X7R to meet the full device temperature specification of –40 °C to +125 °C.

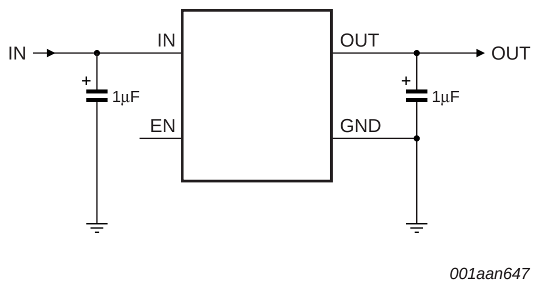


Fig 7. Application diagram

11. Test information

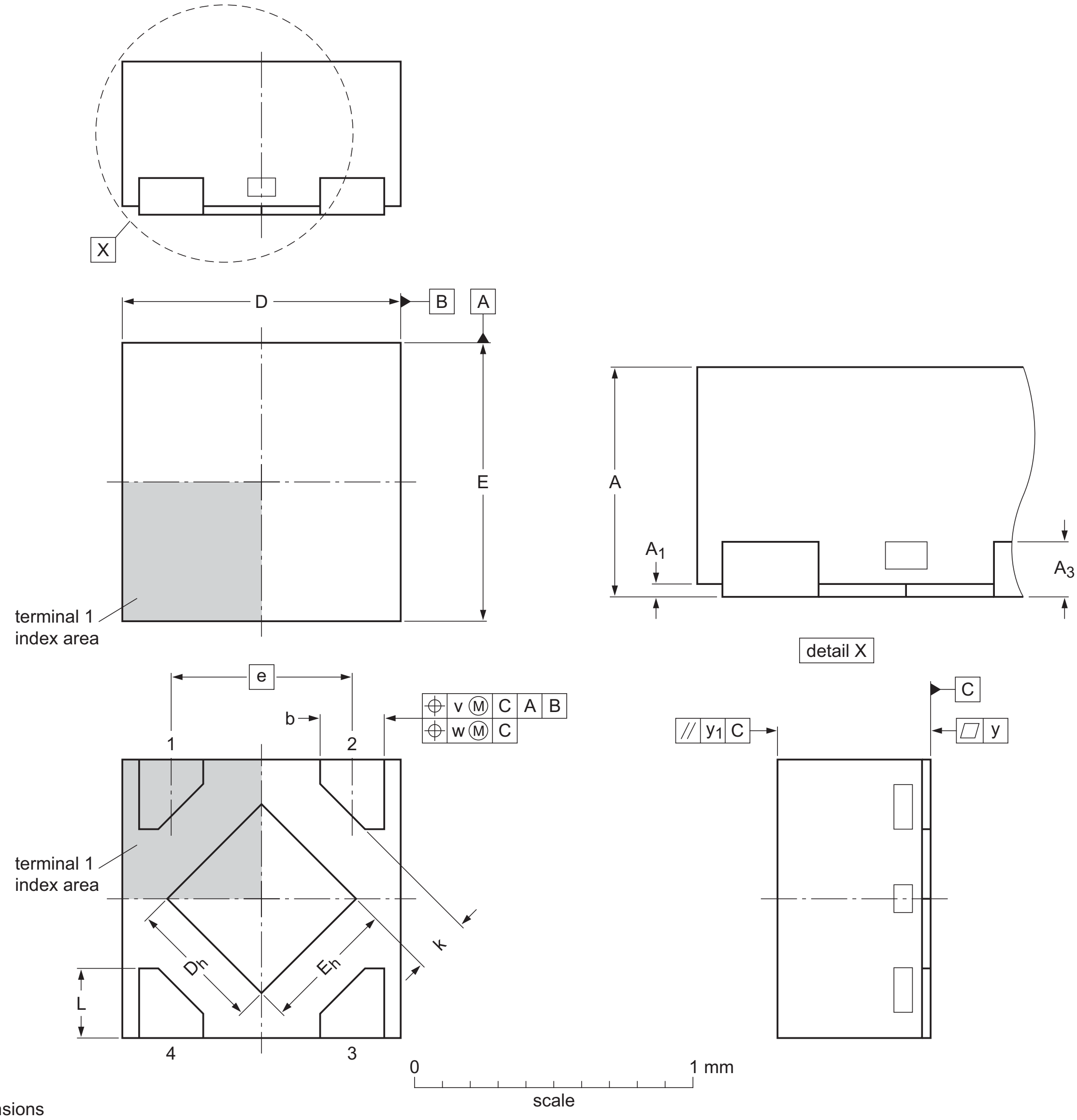
11.1 Quality information

This product has been qualified in accordance with *NX2-00001 NXP Semiconductors Quality and Reliability Specification* and is suitable for use in consumer applications.

12. Package outline

HUSON4: plastic thermal enhanced ultra thin small outline package; no leads; 4 terminals; body 1 x 1 x 0.55 mm

SOT1194-1



Dimensions

Unit(1)		A	A_1	A_3	b	D	D_h	E	E_h	e	k	L	v	w	y	y_1
mm	max	0.55	0.05	0.152	0.30	1.05	0.53	1.05	0.53			0.30				
	nom				0.25	1.00	0.48	1.00	0.48	0.65		0.25	0.1	0.05	0.05	0.05
	min		0.00	0.05	0.20	0.95	0.43	0.95	0.43		0.2	0.20				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1194-1_po

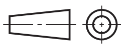
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1194-1	- - -	- - -	- - -			~~11-01-25~~ 11-05-30

Fig 8. Package outline SOT1194-1 (HUSON4)

13. Soldering

Footprint information for reflow soldering of HXSON4 package **SOT1194-1**

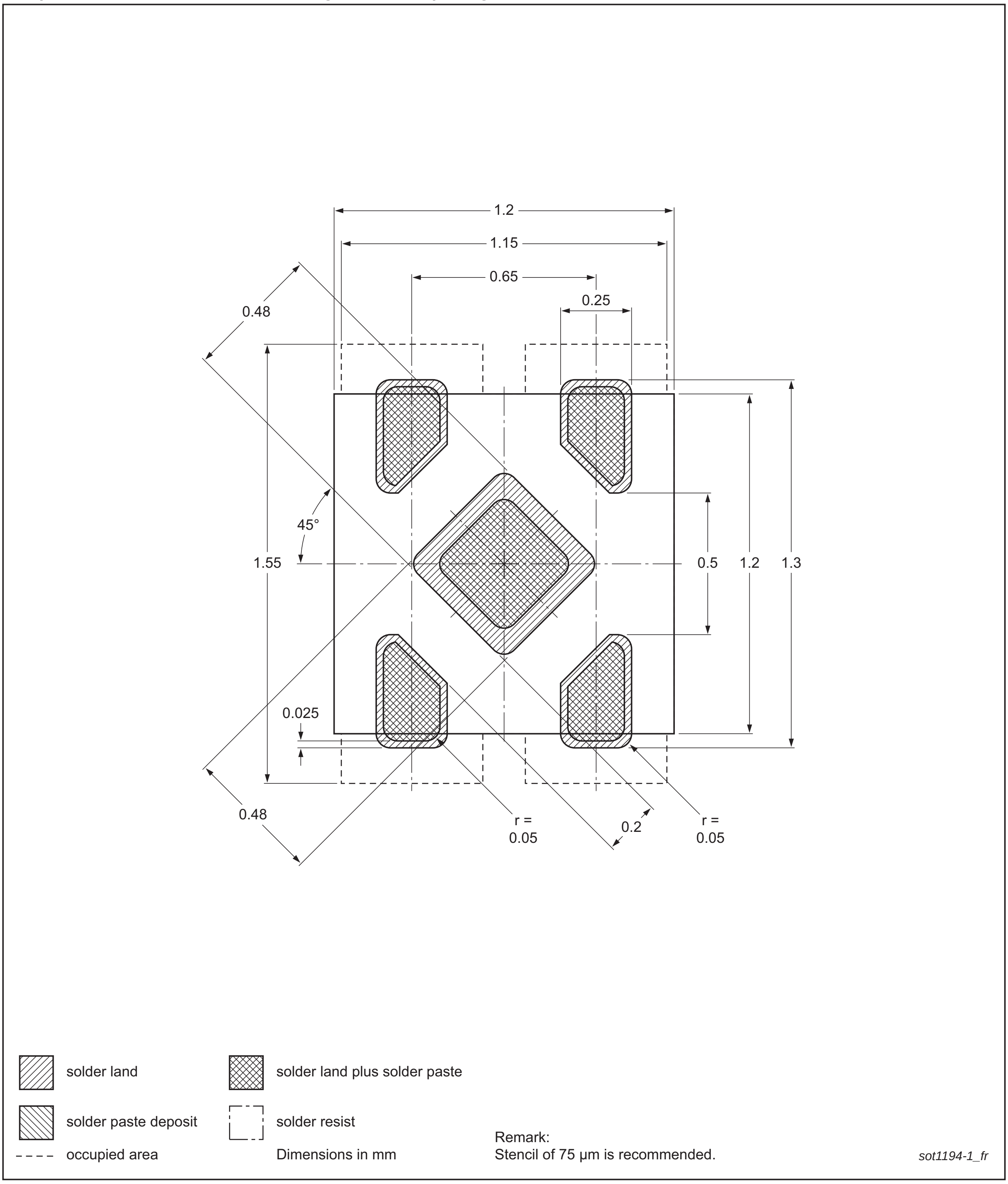


Fig 9. Soldering footprint SOT1194-1 (HUSON4)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

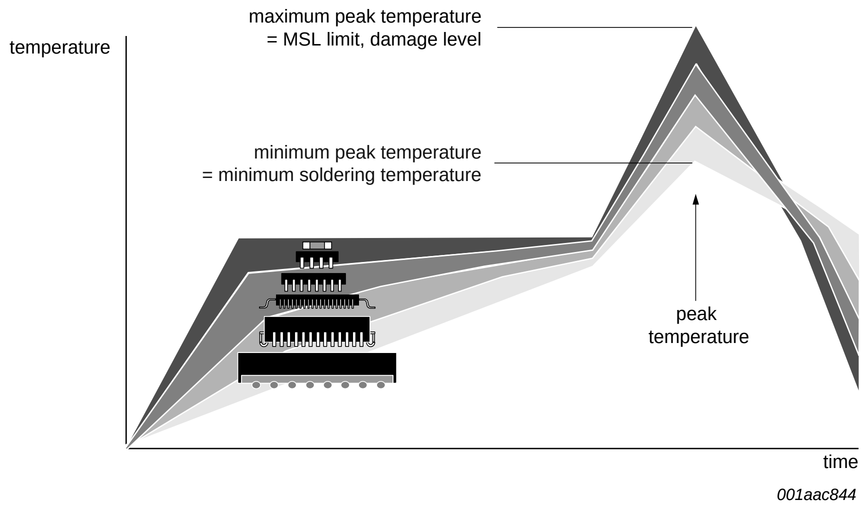
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.



MSL: Moisture Sensitivity Level

Fig 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15. Abbreviations

Table 12. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
LDO	Low DropOut
MM	Machine Model
OSP	Organic Solderability Preservation
PCB	Printed-Circuit Board
PSRR	Power Supply Rejection Ratio
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances

16. References

[1] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[2] **IEC 61340-3-1 —** Methods for simulation of electrostatic effects - Human body model (HBM) electrostatic discharge test waveforms

[3] **JESD22-A115C —** Electrostatic discharge (ESD) Sensitivity Testing Machine Model (MM)

[4] **NX2-00001 —** NXP Semiconductors Quality and Reliability Specification

[5] **AN10365 —** Surface mount reflow soldering description

17. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LD6805_SER v.1	20110922	Objective data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

20. Tables

21. Figures

22. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 22 September 2011

Document identifier: LD6805_SER