4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 4035 (G and H types) and MMC 4035 (E and F types) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package The MMC 4035 integrated circuit is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via JK logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low). Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high. In the parallel or serial mode information is transfered on positive clock transition. When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal. JK input logic is provided on the first stage SERIAL input to minimize logic requirements particulary in counting and sequence-generation applications. With JK inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

FEATURES

- 4-stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- JK inputs on first stage
- Asynchronous TRUE/COMPLEMENT control an all outputs
- Static flip-flop operation; master-slave configuration
- Buffered inputs and outputs
- High speed 12 MHz (typ.) at V_{DD} = 10 V.

ABSOLUTE MAXIMUM RATINGS

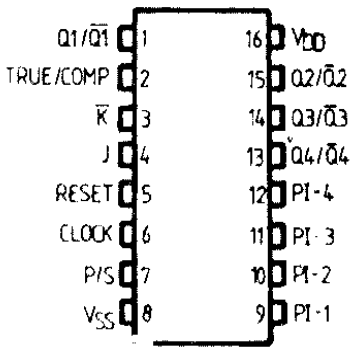
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_I	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

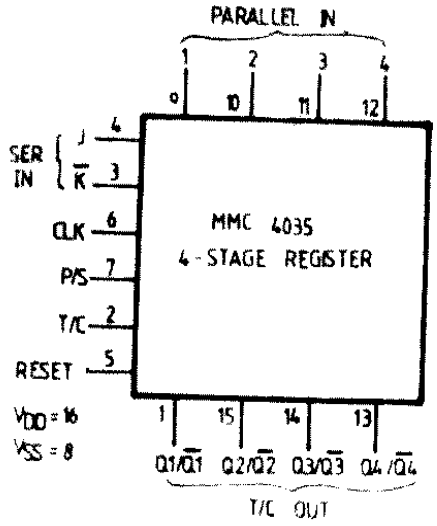
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_I	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

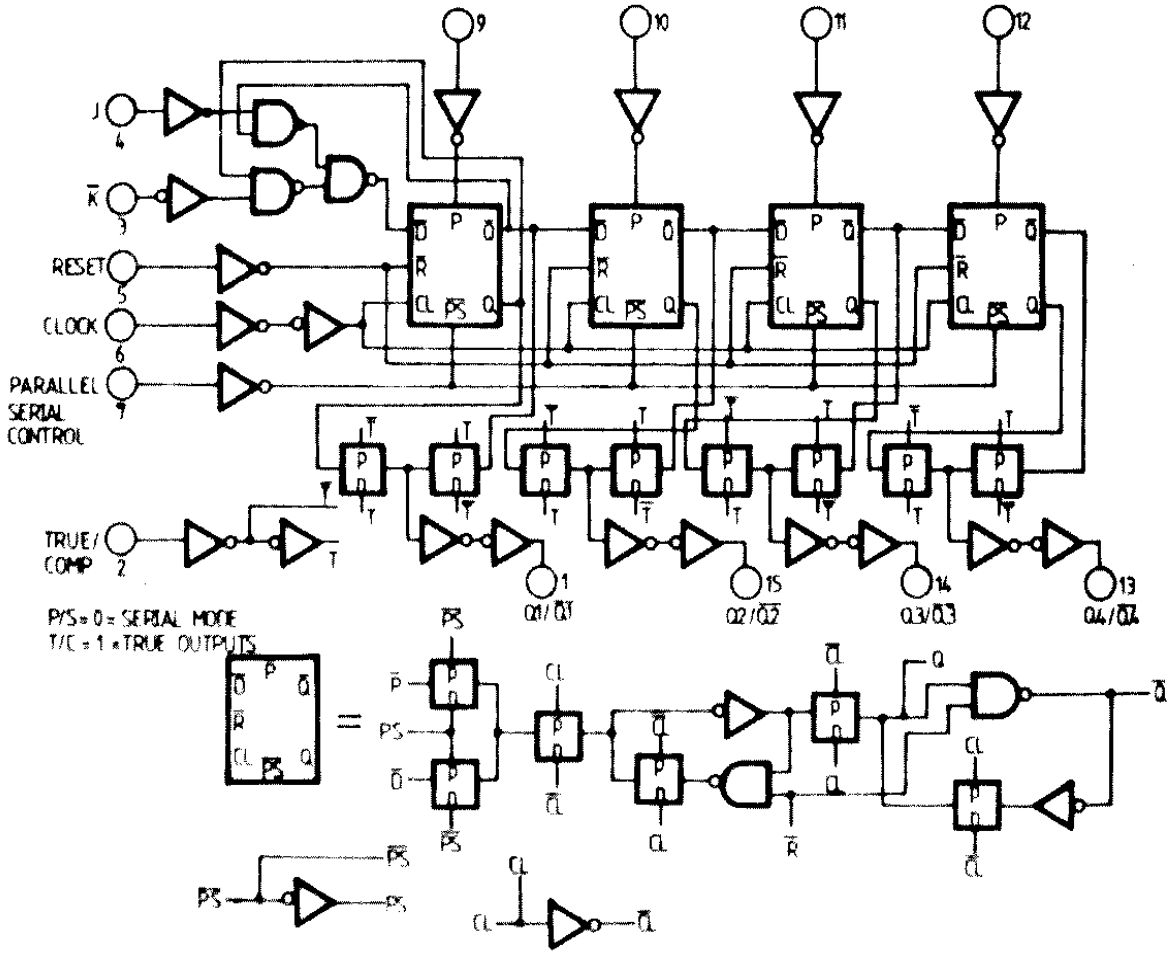


TRUTH TABLE

FIRST STAGE

CLOCK (↗)	t_{n-1} (INPUTS)				t_n(OUTPUTS)
	J	K	R	Q_{n-1}	Q_n
↗	0	X	0	0	0
↗	1	X	0	0	1
↗	X	0	0	1	0
↗	1	0	0	Q_{n-1}	$\overline{Q}_{n-1}$ TOGGLE MODE
↗	X	1	0	1	1
↘	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 [5]	±0.1		±1	μA
		E, F types	0/15			15		±0.3		±10 [5]	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

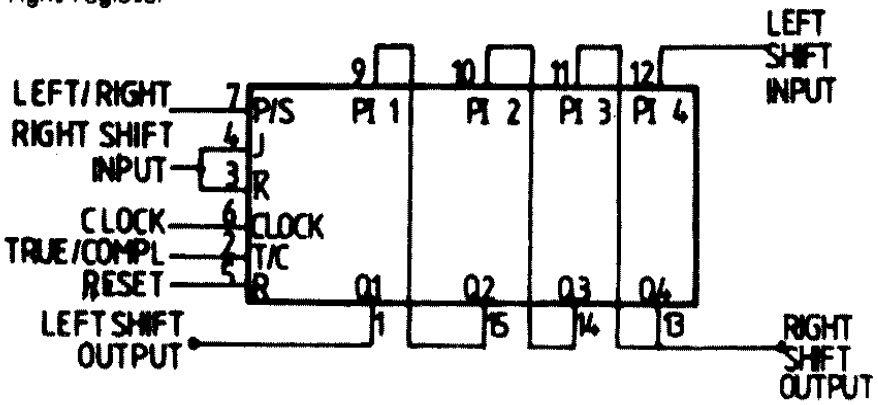
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

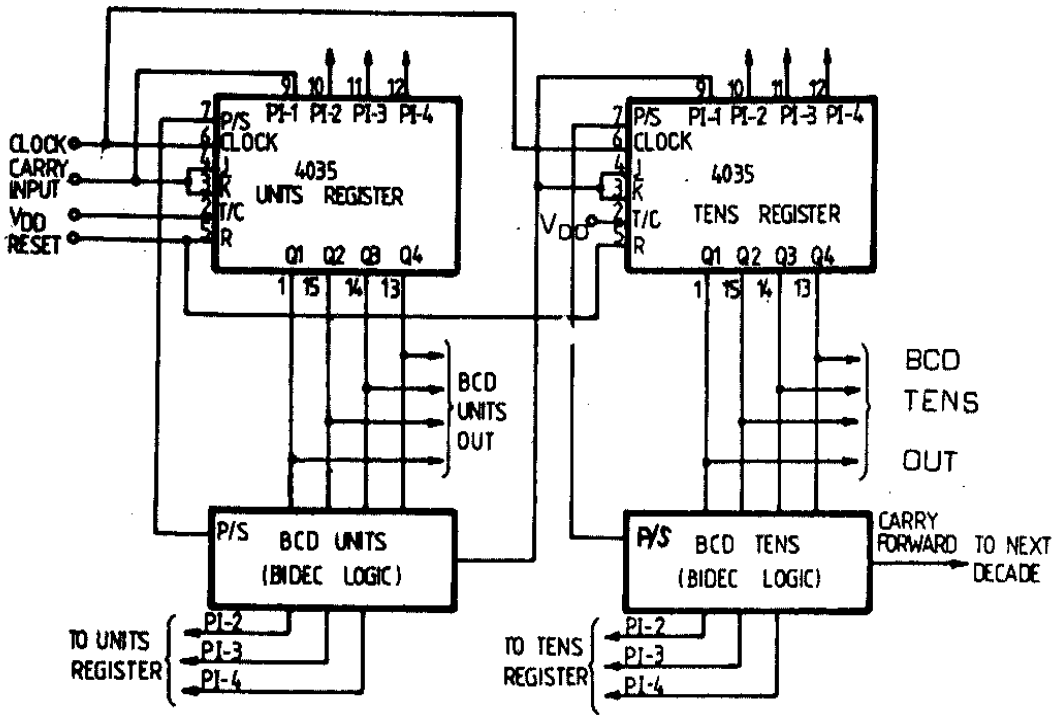
PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	Unit
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time	5		250	500	ns
		10		100	200	
		15		75	150	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	2	4		MHz
		10	6	12		
		15	8	16		
t_W	Clock pulse width	5		100	200	ns
		10		45	90	
		15		30	60	
t_r, t_f	Clock input rise or fall time	5		15		µs
		10		15		
		15		15		
t_{setup}	Data setup time J/K lines	5		110	220	ns
		10		40	80	
		15		30	60	
t_{setup}	Data setup time Parallel-In-Lines	5		70	140	ns
		10		25	50	
		15		20	40	
Reset operation						
t_{PLH}, t_{PHL}	Propagation delay time	5		230	460	ns
		10		100	200	
		15		80	160	
t_W	Reset pulse width	5		125	250	ns
		10		55	110	
		15		40	40	

TYPICAL APPLICATIONS

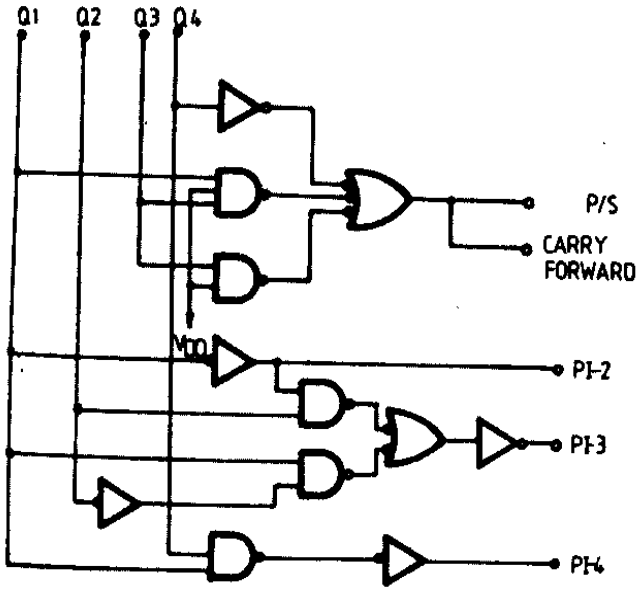
Shift left/shift right register



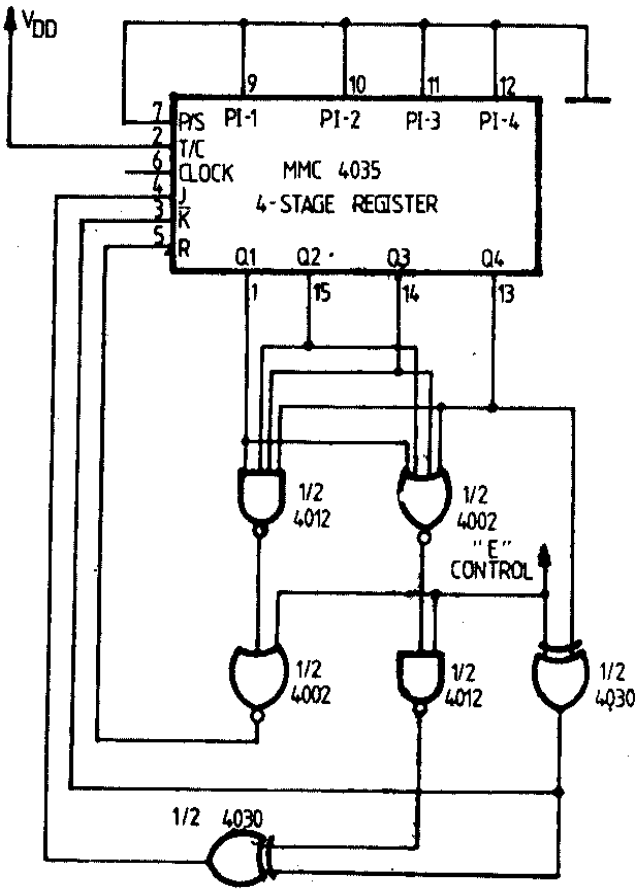
Binary — to — BCD converter



BIDEC logic



Double sequence generator



State sequences

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line).

Control = E = 0

	Q_1 A	Q_2 B	Q_3 C	Q_4 D		Q_1 A	Q_2 B	Q_3 C	Q_4 D
0	0	0	0	0	15	1	1	1	1
1	1	0	0	0	14	0	0	1	1
2	0	1	0	0	13	1	0	1	1
5	1	0	1	0	10	0	1	0	1
10	0	1	0	1	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	09	0
8	0	0	0	1	7	1	1	1	0