National Semiconductor

NM5100/NM100500 ECL I/O 256k BiCMOS SRAM 262,144 x 1 Bit

General Description

The NM5100 and NM100500 are a 262,144-bit fully static, asynchronous, random access memories organized as 262,144 words by 1 bit. The devices are based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM5100 operates with a supply voltage of −5.2V ±5%, yet the input and output voltage levels are temperature compensated 100k ECL compatible. The NM100500 operates with a −4.2V to −4.8V supply voltage.

Reading the memory is accomplished by pulling the chip select ($\overline{S}$) pin LOW while the write enable ($\overline{W}$) pin remains HIGH allowing the memory contents to be displayed on the output pin (Q). The output pin will remain inactive (LOW) if either the chip select ($\overline{S}$) pin is HIGH or the write enable ($\overline{W}$) pin is LOW.

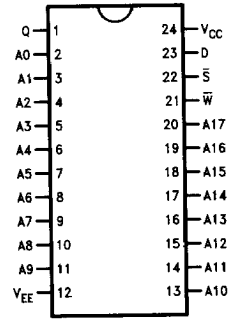
Writing to the device is accomplished by having the chip select ($\overline{S}$) and the write enable ($\overline{W}$) pins LOW. Data on the input pin will then be written into the memory address specified on the address pins (A0–A17).

Features

- 15 ns/18 ns speed grades over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100k ECL I/O
- Power supply −5.2V ±5% (NM5100)
- Power supply −4.2V to −4.8V (NM100500)
- Low power dissipation <1.1W
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 24-pin flatpack

Connection Diagrams

400 Mil Ceramic DIP



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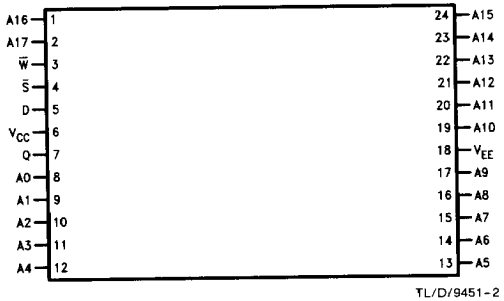
Top View

365 x 535 Ceramic Flatpack (30 Mil Lead Pitch)



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Top View

Pin Names

A0–A17	Address Inputs
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable
Q	Data Out
D	Data In
V_{CC}	Ground
V_{EE}	Power

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