NEC

User's Manual

AS17934

Device File

PC-9800 Series (MS-DOS™) Base

IBM PC/AT™ (PC DOS™) Base

Target Device:

μPD17933
μPD17934
μPD17933A
μPD17934A

Document No. U11733EJ2V0UM00 (2nd edition)
Date Published November 1999 N CP(K)
Printed in Japan

[MEMO]

***emIC-17K* and *SIMPLEHOST* are trademarks of NEC Corporation.**
MS-DOS and Windows are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries.
PC DOS and PC/AT are trademarks of IBM Corporation.

M7A 98.8

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J99.1

MAJOR REVISIONS IN THIS EDITION

Page	Description
Throughout	Target devices added: μPD17933A, 17934A
p.7	[File list in AS17934] File names added: D17933A.DEV, D17934A.DEV

The mark ★ shows major revised points.

[MEMO]

Device files are files that store unique data (device data) dependent upon the 17K Series devices. This information is required when using the following 17K Series software development tools.

- RA17K assembler package
- *SIMPLEHOST*™
- *emlC-17K*™

The following device files are contained in AS17934.

- μPD17933 device files
- μPD17934 device files
- ★ • μPD17433A device file
- ★ • μPD17434A device file

In each device file the file extension is .DEV.

[File list in AS17934]

Device File	File Name	Target Device
AS17934	D17933.DEV	μPD17933
	D17934.DEV	μPD17934
★	D17933A.DEV	μPD17933A[Note]
★	D17934A.DEV	μPD17934A[Note]

Note Under development

For details of the RA17K assembler package and the use of device files contained in the μPD17933, 17934, 17933A, and 17934A, see the **RA17K Assembler Package User's Manual (U10305E)**.

[MEMO]

CONTENTS

[MEMO]

CHAPTER 1 DEVICE DATA

During assembly, the device files provide the following data related to the device.

(1) Program memory (ROM) capacity

★ μPD17933, 17933A: 6144 × 16 bits (0000H to 2FFFH)

★ μPD17934, 17934A: 8192 × 16 bits (0000H to 3FFFH)

(2) Data memory (RAM) capacity

448 × 4 bits (BANK0 to BANK3)

(3) Usable instructions

See **CHAPTER 2 INSTRUCTION SET.**

(4) Register file, port register, and peripheral register read and write data

See **CHAPTER 3 RESERVED SYMBOLS.**

(5) Reserved symbols

See **CHAPTER 3 RESERVED SYMBOLS.**

(6) Device files, device numbers, and SE board numbers

Device files register a device number for each device and a SE board number to indicate the best SE board for developing various products. These device files are also included in ICE files and PRO files output by the RA17K assembler package. These device files are used when the in-circuit emulator checks the development environment and during mask order checking.

Table 1-1. Relations among Device Files, Device Numbers, and SE Board Numbers

Device File	Device Name	Device Number	SE Board Number	SE Board
★ AS17934	μPD17933, 17933A	5A	59	SE-17934
★	μPD17934, 17934A	59		

[MEMO]

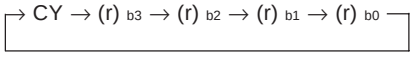
2.1 Instruction Set Summary

b_{14} - b_{11} \ b_{15}		0		1	
BIN	HEX				
0000	0	ADD	r, m	ADD	m, #n4
0001	1	SUB	r, m	SUB	m, #n4
0010	2	ADDC	r, m	ADDC	m, #n4
0011	3	SUBC	r, m	SUBC	m, #n4
0100	4	AND	r, m	AND	m, #n4
0101	5	XOR	r, m	XOR	m, #n4
0110	6	OR	r, m	OR	m, #n4
0111	7	INC INC RORC MOVT PUSH POP GET PUT PEEK POKE BR CALL RET RETSK RETI EI DI STOP HALT NOP	AR IX r DBF, @AR AR AR DBF, p p, DBF WR, rf rf, WR @AR @AR s h		
1000	8	LD	r,m	ST	m, r
1001	9	SKE	m, #n4	SKGE	m, #n4
1010	A	MOV	@r,m	MOV	m, @r
1011	B	SKNE	m, #n4	SKLT	m, #n4
1100	C	BR	addr (page 0)	CALL	addr (page 0)
1101	D	BR	addr (page 1)	MOV	m, #n4
1110	E			SKT	m, #n
1111	F			SKF	m, #n

2.2 Legend

AR	:	Address register
ASR	:	Address stack register indicated by stack pointers
addr	:	Program memory address (low-order 11 bits)
BANK	:	Bank register
CMP	:	Compare flag
CY	:	Carry flag
DBF	:	Data buffer
h	:	Halt release conditions
INTEF	:	Interrupt enable flag
INTR	:	Register that is automatically saved to a stack when an interrupt occurs
INTSK	:	Interrupt stack register
IX	:	Index register
MP	:	Data memory row address pointer
MPE	:	Memory pointer enable flag
m	:	Data memory address indicated by m_R and m_C
m_R	:	Data memory row address (high)
m_C	:	Data memory column address (low)
n	:	Bit position (4 bits)
n4	:	Immediate data (4 bits)
PAGE	:	Page (Bit 11 of program counter)
PC	:	Program counter
p	:	Peripheral address
p_H	:	Peripheral address (high-order 3 bits)
p_L	:	Peripheral address (low-order 4 bits)
r	:	General register column address
rf	:	Register file address
rf_R	:	Register file row address (high-order 3 bits)
rf_C	:	Register file column address (low-order 4 bits)
SP	:	Stack pointer
s	:	Stop release conditions
WR	:	Window register
(×)	:	× indicates addressed contents

2.3 Instruction List

Instruction Set	Mnemonic	Operand	Operation	Instruction Code			
				Op Code	Operand		
Addition	ADD	r, m	(r) ← (r) + (m)	00000	m_R	m_C	r
		m, #n4	(m) ← (m) + n4	10000	m_R	m_C	n4
	ADDC	r, m	(r) ← (r) + (m) + CY	00010	m_R	m_C	r
		m, #n4	(m) ← (m) + n4 + CY	10010	m_R	m_C	n4
	INC	AR	AR ← AR + 1	00111	000	1001	0000
		IX	IX ← IX + 1	00111	000	1000	0000
Subtraction	SUB	r, m	(r) ← (r) – (m)	00001	m_R	m_C	r
		m, #n4	(m) ← (m) – n4	10001	m_R	m_C	n4
	SUBC	r, m	(r) ← (r) – (m) – CY	00011	m_R	m_C	r
		m, #n4	(m) ← (m) – n4 – CY	10011	m_R	m_C	n4
Logical operation	OR	r, m	(r) ← (r) ∨ (m)	00110	m_R	m_C	r
		m, #n4	(m) ← (m) ∨ n4	10110	m_R	m_C	n4
	AND	r, m	(r) ← (r) ∧ (m)	00100	m_R	m_C	r
		m, #n4	(m) ← (m) ∧ n4	10100	m_R	m_C	n4
	XOR	r, m	(r) ← (r) ∀ (m)	00101	m_R	m_C	r
		m, #n4	(m) ← (m) ∀ n4	10101	m_R	m_C	n4
Decision	SKT	m, #n	CMP ← 0, if (m) ∧ n = n, then skip	11110	m_R	m_C	n
	SKF	m, #n	CMP ← 0, if (m) ∧ n = 0, then skip	11111	m_R	m_C	n
Comparison	SKE	m, #n4	(m) – n4, skip if zero	01001	m_R	m_C	n4
	SKNE	m, #n4	(m) – n4, skip if not zero	01011	m_R	m_C	n4
	SKGE	m, #n4	(m) – n4, skip if not borrow	11001	m_R	m_C	n4
	SKLT	m, #n4	(m) – n4, skip if borrow	11011	m_R	m_C	n4
Rotation	RORC	r		00111	000	0111	r
Transfer	LD	r, m	(r) ← (m)	01000	m_R	m_C	r
	ST	m, r	(m) ← (r)	11000	m_R	m_C	r
	MOV	@r, m	if MPE = 1 : (MP, (r)) ← (m) if MPE = 0 : (BANK, m_R, (r)) ← (m)	01010	m_R	m_C	r
		m, @r	if MPE = 1 : (m) ← (MP, (r)) if MPE = 0 : (m) ← (BANK, m_R, (r))	11010	m_R	m_C	r
		m, #n4	(m) ← n4	11101	m_R	m_C	n4
	MOVT	DBF, @AR	SP ← SP–1, ASR ← PC, PC ← AR, DBF ← (PC), PC ← ASR, SP ← SP + 1	00111	000	0001	0000
	PUSH	AR	SP ← SP –1, ASR ← AR	00111	000	1101	0000
	POP	AR	AR ← ASR, SP ← SP + 1	00111	000	1100	0000
	GET	DBF, p	DBF ← (p)	00111	p_H	1011	p_L
	PUT	p, DBF	(p) ← DBF	00111	p_H	1010	p_L
	PEEK	WR, rf	WR ← (rf)	00111	rf_R	0011	rf_C
	POKE	rf, WR	(rf) ← WR	00111	rf_R	0010	rf_C

Instruction Set	Mnemonic	Operand	Operation	Instruction Code			
				Op Code	Operand		
Branch	BR	addr	PC_{10-0} ← addr, PAGE ← 0	01100	addr		
			PC_{10-0} ← addr, PAGE ← 1	01101			
		@AR	PC ← AR	00111	000	0100	0000
Subroutine	CALL	addr	SP ← SP – 1, ASR ← PC PC_{11} ← 0, PC_{10-0} ← addr	11100	addr		
		@AR	SP ← SP – 1, ASR ← PC PC ← AR	00111	000	0101	0000
	RET		PC ← ASR, SP ← SP + 1	00111	000	1110	0000
	RETSK		PC ← ASR, SP ← SP + 1 and skip	00111	001	1110	0000
	RETI		PC ← ASR, INTR ← INTSK, SP ← SP + 1	00111	010	1110	0000
Interrupt	EI		INTEF ← 1	00111	000	1111	0000
	DI		INTEF ← 0	00111	001	1111	0000
Others	STOP	s	STOP	00111	010	1111	s
	HALT	h	HALT	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

2.4 Macro Instructions Bundled with Assembler (RA17K)

Legend

flag n : FLG-type symbol

n : Bit No.

< > : Contents between < > symbols can be omitted.

	Mnemonic	Operand	Operation	n
Bundled macros	SKTn	flag 1, ··· flag n	if (flag 1) to (flag n) = all “1”, then skip	1≤ n ≤ 4
	SKFn	flag 1, ··· flag n	if (flag 1) to (flag n) = all “0”, then skip	1≤ n ≤ 4
	SETn	flag 1, ··· flag n	(flag 1) to (flag n)← 1	1 ≤ n ≤ 4
	CLRn	flag 1, ··· flag n	(flag 1) to (flag n)← 0	1 ≤ n ≤ 4
	NOTn	flag 1, ··· flag n	if (flag n) = “0”, then (flag n)← 1 if (flag n) = “1”, then (flag n) ← 0	1 ≤ n ≤ 4
	INITFLG	<NOT> flag 1, ··· <<NOT> flag n>	if description = NOT flag n, then (flag n) ← 0 if description = flag n, then (flag n)← 1	1 ≤ n ≤ 4
	BANKn		(BANK) ← n	0 ≤ n ≤ 15
Extended instruction	BRX	Label	Jump Label	–
	CALLX	function-name	CALL sub-routine	–
	SYSCALX	function-name or expression	CALL system sub-routine	–
	INITFLGX	<NOT/INV> flag 1, ··· <NOT/INV> flag n	if description = NOT (or INV) flag, (flag)← 0 if description = flag, (flag) ← 1	n ≤ 4

[MEMO]

CHAPTER 3 RESERVED SYMBOLS

★ The symbols defined for the μPD17933, 17933A, 17934, and 17934A are described on the following pages. These symbols are listed below.

- Data buffer (DBF)
- System register (SYSREG)
- LCD segment register
- Port register
- Register file (Control register)
- Peripheral hardware register
- Others

3.1 Data Buffer (DBF)

Symbol Name	Attribute	Value	R/W	Description
DBF3	MEM	0.0CH	R/W	DBF bits 15 to 12
DBF2	MEM	0.0DH	R/W	DBF bits 11 to 8
DBF1	MEM	0.0EH	R/W	DBF bits 7 to 4
DBF0	MEM	0.0FH	R/W	DBF bits 3 to 0

3.2 System Register (SYSREG)

Symbol Name	Attribute	Value	R/W	Description
AR3	MEM	0.74H	R/W	Address register bits 15 to 12
AR2	MEM	0.75H	R/W	Address register bits 11 to 8
AR1	MEM	0.76H	R/W	Address register bits 7 to 4
AR0	MEM	0.77H	R/W	Address register bits 3 to 0
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Index register bits 10 to 8
MPH	MEM	0.7AH	R/W	Memory pointer bits 6 to 4
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Index register bits 7 to 4
MPL	MEM	0.7BH	R/W	Memory pointer bits 3 to 0
IXL	MEM	0.7CH	R/W	Index register bits 3 to 0
RPH	MEM	0.7DH	R/W	General register pointer bits 6 to 3
RPL	MEM	0.7EH	R/W	General register pointer bits 2 to 0
BCD	FLG	0.7EH.0	R/W	BCD operation flag
PSW	MEM	0.7FH	R/W	Program status word
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index enable flag

3.3 LCD Segment Register

Symbol Name	Attribute	Value	R/W	Description
LCDD19	MEM	14.5CH	R/W	LCD segment register
LCDD18	MEM	14.5DH	R/W	LCD segment register
LCDD17	MEM	14.5EH	R/W	LCD segment register
LCDD16	MEM	14.5FH	R/W	LCD segment register
LCDD15	MEM	14.60H	R/W	LCD segment register
LCDD14	MEM	14.61H	R/W	LCD segment register
LCDD13	MEM	14.62H	R/W	LCD segment register
LCDD12	MEM	14.63H	R/W	LCD segment register
LCDD11	MEM	14.64H	R/W	LCD segment register
LCDD10	MEM	14.65H	R/W	LCD segment register
LCDD9	MEM	14.66H	R/W	LCD segment register
LCDD8	MEM	14.67H	R/W	LCD segment register
LCDD7	MEM	14.68H	R/W	LCD segment register
LCDD6	MEM	14.69H	R/W	LCD segment register
LCDD5	MEM	14.6AH	R/W	LCD segment register
LCDD4	MEM	14.6BH	R/W	LCD segment register
LCDD3	MEM	14.6CH	R/W	LCD segment register
LCDD2	MEM	14.6DH	R/W	LCD segment register
LCDD1	MEM	14.6EH	R/W	LCD segment register
LCDD0	MEM	14.6FH	R/W	LCD segment register

3.4 Port Register

Symbol Name	Attribute	Value	R/W	Description
P0A1	FLG	0.70H.1	R/W	Port 0A bit 1
P0A0	FLG	0.70H.0	R/W	Port 0A bit 0
P0B3	FLG	0.71H.3	R/W	Port 0B bit 3
P0B2	FLG	0.71H.2	R/W	Port 0B bit 2
P0B1	FLG	0.71H.1	R/W	Port 0B bit 1
P0B0	FLG	0.71H.0	R/W	Port 0B bit 0
P0C3	FLG	0.72H.3	R/W	Port 0C bit 3
P0C2	FLG	0.72H.2	R/W	Port 0C bit 2
P0C1	FLG	0.72H.1	R/W	Port 0C bit 1
P0C0	FLG	0.72H.0	R/W	Port 0C bit 0
P0D3	FLG	0.73H.3	R Note	Port 0D bit 3
P0D2	FLG	0.73H.2	R Note	Port 0D bit 2
P0D1	FLG	0.73H.1	R Note	Port 0D bit 1
P0D0	FLG	0.73H.0	R Note	Port 0D bit 0
P1A3	FLG	1.70H.3	R/W	Port 1A bit 3
P1A2	FLG	1.70H.2	R/W	Port 1A bit 2
P1A1	FLG	1.70H.1	R/W	Port 1A bit 1
P1A0	FLG	1.70H.0	R/W	Port 1A bit 0
P1C3	FLG	1.72H.3	R Note	Port 1C bit 3
P1C2	FLG	1.72H.2	R Note	Port 1C bit 2
P1C1	FLG	1.72H.1	R Note	Port 1C bit 1
P1C0	FLG	1.72H.0	R Note	Port 1C bit 0
P1D3	FLG	1.73H.3	R/W	Port 1D bit 3
P1D2	FLG	1.73H.2	R/W	Port 1D bit 2
P1D1	FLG	1.73H.1	R/W	Port 1D bit 1
P1D0	FLG	1.73H.0	R/W	Port 1D bit 0
P2A2	FLG	2.70H.2	R/W	Port 2A bit 2
P2A1	FLG	2.70H.1	R/W	Port 2A bit 1
P2A0	FLG	2.70H.0	R/W	Port 2A bit 0
P2B3	FLG	2.71H.3	R/W	Port 2B bit 3
P2B2	FLG	2.71H.2	R/W	Port 2B bit 2
P2B1	FLG	2.71H.1	R/W	Port 2B bit 1
P2B0	FLG	2.71H.0	R/W	Port 2B bit 0
P2C3	FLG	2.72H.3	R/W	Port 2C bit 3
P2C2	FLG	2.72H.2	R/W	Port 2C bit 2
P2C1	FLG	2.72H.1	R/W	Port 2C bit 1
P2C0	FLG	2.72H.0	R/W	Port 2C bit 0

Note These ports are input-only ports. The assembler and in-circuit emulator will not output error messages even if an instruction to output from these ports is written. Also, if the instruction is actually executed on a device, the operation will have no change.

3.5 Register File (Control Register)

Symbol Name	Attribute	Value	R/W	Description
SP	MEM	0.81H	R/W	Stack pointer
DBFSP	MEM	0.84H	R	DBF stack pointer
SPRSEL	MEM	0.85H	R/W	Stack overflow select flag (Settable only once after power application)
MOVTSEL1	FLG	0.87H.1	R/W	MOVT bit select flag
MOVTSEL0	FLG	0.87H.0	R/W	MOVT bit select flag
SYSRSP	MEM	0.88H	R	System register stack pointer
WDTCK	MEM	15.02H	R/W	Watchdog timer clock select flag
WDTRES	FLG	15.03H.3	R/W	Watchdog timer count reset
PLLSCNF	FLG	15.10H.3	R/W	Swallow counter MSB set flag
★ PLLMD2[Note]	FLG	15.10H.2	R/W	PLL mode select flag
PLLMD1	FLG	15.10H.1	R/W	PLL mode select flag
PLLMD0	FLG	15.10H.0	R/W	PLL mode select flag
PLLRFCK3	FLG	15.11H.3	R/W	PLL reference frequency select flag
PLLRFCK2	FLG	15.11H.2	R/W	PLL reference frequency select flag
PLLRFCK1	FLG	15.11H.1	R/W	PLL reference frequency select flag
PLLRFCK0	FLG	15.11H.0	R/W	PLL reference frequency select flag
PLLUL	FLG	15.12H.0	R	PLL unlock FF flag
BEEP0SEL	FLG	15.14H.2	R/W	BEEP0 enable flag
BEEP0CK1	FLG	15.14H.1	R/W	BEEP0 clock select flag
BEEP0CK0	FLG	15.14H.0	R/W	BEEP0 clock select flag
WDTCY	FLG	15.16H.0	R	Watchdog timer/stack pointer reset status detection flag
BTM0CY	FLG	15.17H.0	R	Basic timer 0 carry flag
BTM1CK0	FLG	15.18H.0	R/W	Basic timer 1 clock select flag
SIO1CK1	FLG	15.1CH.1	R/W	Serial interface 1 I/O clock select flag
SIO1CK0	FLG	15.1CH.0	R/W	Serial interface 1 I/O clock select flag
SIO1MOD	FLG	15.1DH.2	R/W	Serial interface 1 SI1/SO2 select flag
SIO1HIZ	FLG	15.1DH.1	R/W	Serial interface 1 general-purpose port select flag
SIO1TS	FLG	15.1DH.0	R/W	Serial interface 1 transmit/receive start flag
IEG0	FLG	15.1FH.0	R/W	INT0 pin interrupt request detection edge direction select flag
FCGCH0	FLG	15.20H.0	R/W	FCG channel select flag
IFCG0STT	FLG	15.21H.0	R	IF counter gate status detection flag (1: open, 0: close)
IFCMD1	FLG	15.22H.3	R/W	IF counter mode select flag (10: FMIFC, 11: AMIFC2)
IFCMD0	FLG	15.22H.2	R/W	IF counter mode select flag (00: FCG, 01: AMIFC)
IFCCK1	FLG	15.22H.1	R/W	IF counter clock select flag
IFCCK0	FLG	15.22H.0	R/W	IF counter clock select flag
IFCSTRT	FLG	15.23H.1	W	IF counter count start
IFCRES	FLG	15.23H.0	R/W	IF counter reset

★ **Note** Provided for the μPD17933A and 17934A only.

Symbol Name	Attribute	Value	R/W	Description
ADCCH3	FLG	15.24H.3	R/W	A/D converter channel select flag
ADCCH2	FLG	15.24H.2	R/W	A/D converter channel select flag
ADCCH1	FLG	15.24H.1	R/W	A/D converter channel select flag
ADCCH0	FLG	15.24H.0	R/W	A/D converter channel select flag
ADCSTRT	FLG	15.25H.1	R/W	A/D converter compare start flag
ADCCMP	FLG	15.25H.0	R	A/D converter compare result detection flag
TM0EN	FLG	15.2BH.3	R/W	Modulo timer 0 count start flag
TM0RES	FLG	15.2BH.2	R/W	Modulo timer 0 reset flag (The value is 0 when read)
TM0CK1	FLG	15.2BH.1	R/W	Modulo timer 0 clock select flag (10: TM10, 11: TM11)
TM0CK0	FLG	15.2BH.0	R/W	Modulo timer 0 clock select flag (00: 75 kHz, 01: 25 kHz)
TM0OVF	FLG	15.2CH.3	R	Modulo timer 0 overflow detection flag
IPSIO1	FLG	15.2FH.3	R/W	Serial interface 1 interrupt enable flag
IPBTM1	FLG	15.2FH.2	R/W	Basic timer 1 interrupt enable flag
IPTM0	FLG	15.2FH.1	R/W	Modulo timer 0 interrupt enable flag
IP0	FLG	15.2FH.0	R/W	INT0 pin interrupt enable flag
IRQSIO1	FLG	15.3CH.0	R/W	Serial interface 1 interrupt request detection flag
IRQBTM1	FLG	15.3DH.0	R/W	Basic timer 1 interrupt request detection flag
IRQTM0	FLG	15.3EH.0	R/W	Modulo timer 0 interrupt request detection flag
INT0	FLG	15.3FH.3	R/W	INT0 pin status detection flag
IRQ0	FLG	15.3FH.0	R/W	INT0 pin interrupt request detection flag
LCDEN	FLG	15.40H.0	R/W	LCD driver display start flag
★ LCDDBCK	FLG	15.40H.3	R/W	Clock selection of LCD display pressure booster circuit
LCD19SEL	FLG	15.69H.2	R/W	P2A2/LCD19 switching flag
LCD18SEL	FLG	15.69H.1	R/W	P2A1/LCD18 switching flag
LCD17SEL	FLG	15.69H.0	R/W	P2A0/LCD17 switching flag
P0DPLD3	FLG	15.6AH.3	R/W	POD3 pin pull-down resistor switching flag
P0DPLD2	FLG	15.6AH.2	R/W	POD2 pin pull-down resistor switching flag
P0DPLD1	FLG	15.6AH.1	R/W	POD1 pin pull-down resistor switching flag
P0DPLD0	FLG	15.6AH.0	R/W	POD0 pin pull-down resistor switching flag
P2CBIO3	FLG	15.6BH.3	R/W	P2C3 I/O select flag
P2CBIO2	FLG	15.6BH.2	R/W	P2C2 I/O select flag
P2CBIO1	FLG	15.6BH.1	R/W	P2C1 I/O select flag
P2CBIO0	FLG	15.6BH.0	R/W	P2C0 I/O select flag
P2BBIO3	FLG	15.6CH.3	R/W	P2B3 I/O select flag
P2BBIO2	FLG	15.6CH.2	R/W	P2B2 I/O select flag
P2BBIO1	FLG	15.6CH.1	R/W	P2B1 I/O select flag
P2BBIO0	FLG	15.6CH.0	R/W	P2B0 I/O select flag

Symbol Name	Attribute	Value	R/W	Description
P1DBIO3	FLG	15.6DH.3	R/W	P1D3 I/O select flag
P1DBIO2	FLG	15.6DH.2	R/W	P1D2 I/O select flag
P1DBIO1	FLG	15.6DH.1	R/W	P1D1 I/O select flag
P1DBIO0	FLG	15.6DH.0	R/W	P1D0 I/O select flag
P1ABIO3	FLG	15.6EH.3	R/W	P1A3 I/O select flag
P1ABIO2	FLG	15.6EH.2	R/W	P1A2 I/O select flag
P1ABIO1	FLG	15.6EH.1	R/W	P1A1 I/O select flag
P1ABIO0	FLG	15.6EH.0	R/W	P1A0 I/O select flag
P0BBIO3	FLG	15.6FH.3	R/W	P0B3 I/O select flag
P0BBIO2	FLG	15.6FH.2	R/W	P0B2 I/O select flag
P0BBIO1	FLG	15.6FH.1	R/W	P0B1 I/O select flag
P0BBIO0	FLG	15.6FH.0	R/W	P0B0 I/O select flag

3.6 Peripheral Hardware Register

Symbol Name	Attribute	Value	R/W	Description
ADCR	DAT	02H	R/W	A/D converter reference voltage set register
SIO1SFR	DAT	04H	R/W	Serial interface 1 presettable shift register
TM0M	DAT	1AH	R/W	Timer modulo 0 register
TM0C	DAT	1BH	R	Timer modulo 0 counter
AR	DAT	40H	R/W	Address register
DBFSTK	DAT	41H	R/W	DBF stack register
PLLR	DAT	42H	R/W	PLL data register
IFC	DAT	43H	R	IF counter data register

3.7 Others

Symbol Name	Attribute	Value	Description
DBF	DAT	0FH	Operand (DBF) for GET/PUT/MOVT/MOVTH/MOVTL instruction
IX	DAT	01H	Operand (IX) for INC instruction
AR_EPA1	DAT	8040H	Operand (EPA bit ON) for CALL/BR/MOVT/MOVTH/MOVTL instruction
AR_EPA0	DAT	4040H	Operand (EPA bit OFF) for CALL/BR/MOVT/MOVTH/MOVTL instruction

3.8 List of Reserved Words (in Alphabetical Order)

3.8.1 Instructions and directives

ADD	EXITR	NIBBLE7V	SKF1
ADDC	EXTRN	NIBBLE8	SKF2
AND	FLG	NIBBLE8V	SKF3
BANK0	GET	NOBMAC	SKF4
BANK1	GLOBAL	NOLIST	SKGE
BANK2	HALT	NOMAC	SKLT
BANK3	IF	NOP	SKNE
BANK14	IFCHAR	NOT1	SKT
BANK15	IFNCHAR	NOT2	SKT1
BR	INC	NOT3	SKT2
BRR	INCLUDE	NOT4	SKT3
C14344	INITFLG	OBMAC	SKT4
C4444	IRP	OMAC	SMAC
CALL	LAB	OR	ST
CASE	LBMAC	ORG	STOP
CLR1	LD	OTHER	SUB
CLR2	LFCOND	PEEK	SUBC
CLR3	LIST	POKE	SUMMARY
CLR4	LITERAL	POP	TAG
CSEG	LMAC	PUBLIC	TITLE
DAT	MACRO	PURGE	XOR
DB	MEM	PUSH	ZZZERROR
DI	MOV	PUT	ZZZMCHK
DW	MOVT	REPT	ZZZMSG
EI	NIBBLE	RET	
EJECT	NIBBLE1	RETI	
ELSE	NIBBLE2	RETSK	
END	NIBBLE2V	RORC	
ENDCASE	NIBBLE3	SBMAC	
ENDIF	NIBBLE3V	SET	
ENDIFC	NIBBLE4	SET1	
ENDIFNC	NIBBLE4V	SET2	
ENDM	NIBBLE5	SET3	
ENDP	NIBBLE5V	SET4	
ENDR	NIBBLE6	SFCOND	
EOF	NIBBLE6V	SKE	
EXIT	NIBBLE7	SKF	

3.8.2 Registers and flags

ADCCH0	INT0	MOVTSEL1	P1DBIO2
ADCCH1	IP0	MPE	P1DBIO3
ADCCH2	IPBTM1	MPH	P2A0
ADCCH3	IPSIO1	MPL	P2A1
ADCCMP	IPTM0	P0A0	P2A2
ADCR	IRQ0	P0A1	P2B0
ADCSTRT	IRQBTM1	P0B0	P2B1
AR	IRQSIO1	P0B1	P2B2
AR0	IRQTM0	P0B2	P2B3
AR1	IX	P0B3	P2BBIO0
AR2	IXE	P0C0	P2BBIO1
AR3	IXH	P0C1	P2BBIO2
AR_EPA0	IXL	P0C2	P2BBIO3
AR_EPA1	IXM	P0C3	P2C0
BANK	LCD17SEL	P0D0	P2C1
BCD	LCD18SEL	P0D1	P2C2
BEEP0CK0	LCD19SEL	P0D2	P2C3
BEEP0CK1	LCDD0	P0D3	P2CBIO0
BEEP0SEL	LCDD1	P0DPLD0	P2CBIO1
BTM0CY	LCDD2	P0DPLD1	P2CBIO2
BTM1CK0	LCDD3	P0DPLD2	P2CBIO3
CMP	LCDD4	P0DPLD3	PLLMD0
CY	LCDD5	P1A0	PLLMD1
★ DBF	LCDD6	P1A1	PLLMD2[Note]
DBF0	LCDD7	P1A2	PLLR
DBF1	LCDD8	P1A3	PLLRFCK0
DBF2	LCDD9	P1ABIO0	PLLRFCK1
DBF3	LCDD10	P1ABIO1	PLLRFCK2
DBFSP	LCDD11	P1ABIO2	PLLRFCK3
DBFSTK	LCDD12	P1ABIO3	PLLSCNF
FCGCH0	LCDD13	P1C0	PLLUL
IEG0	LCDD14	P1C1	PSW
IFC	LCDD15	P1C2	RPH
IFCCK0	LCDD16	P1C3	RPL
IFCCK1	LCDD17	P1D0	SIO1CK0
IFCGOSTT	LCDD18	P1D1	SIO1CK1
IFCMD0	LCDD19	P1D2	SIO1HIZ
★ IFCMD1	LCDDBCK	P1D3	SIO1MOD
IFCRES	LCDEN	P1DBIO0	SIO1SFR
IFCSTRT	MOVTSEL0	P1DBIO1	SlO1TS

★ **Note** Provided for the μPD17933A and 17934A only.

SP

SPRSEL

SYSRSP

TM0C

TM0CK0

TM0CK1

TM0EN

TM0M

TM0OVF

TM0RES

WDTCK

WDTCY

WDTRES

WR

Z

ZZZ0

ZZZ1

ZZZ2

ZZZ3

ZZZ4

ZZZ5

ZZZ6

ZZZ7

ZZZ8

ZZZ9

ZZZALBMAC

ZZZALMAC

ZZZARGC

ZZZDEVID

ZZZEPA

ZZZLSARG

ZZZPRINT

ZZZSKIP

ZZZSYDOC

ZZZLINE

CHAPTER 4 LOAD MODULE FILE FORMAT

HEX-format load module files output by the RA17K assembler package have two types of output formats: ICE files and PRO files.

These two types of files must be used according to the target application. Besides having a user program area, they also have an assembly environment data area, an in-circuit emulator operating environment data area, and other areas.

(1) HEX-format load module file format

The data contained in HEX-format load module files output by the assembler is output in the following format.

[Example of HEX-format load module file format]

```
 :  10  0002   00  2B41000BFC80F ··· 3A20  EC
 |   |   |     |                |          |
<1><2>  <3>   <4>              <5>        <6>

 :  00  0000   01  FF
 |   |   |     |   |
<1><2>  <3>   <4> <6>
```

<1> Record mark

This indicates the start of a record.

<2> Code amount (2 digits)

This indicates the amount of code (byte data) stored in a record. This value is expressed as a hexadecimal number, with a maximum value of 10H (16 units). The value for the end record is 00H.

<3> Address (4 digits)

This indicates the start address of the code shown in a record. The value for the end record is 0000H, and has no relation to the address.

<4> Record type (2 digits)

A value of 00H indicates “data record” as the record type and a value of 01H indicates “end record.”

<5> Code (up to 32 digits (16 bytes))

Code is output to this field one byte at a time, up to 16 bytes.

<6> Check sum (2 digits)

Each data from fields <2>, <3>, <4>, <5> and <6> is output to this field (with even parity) as byte data with an LSB value of 00H based on byte-unit sums.

(2) ICE files

ICE files are output as HEX-format files exclusive to the in-circuit emulator (IE-17K, IE-17K-ET, or EMU-17K [Note]) output by the RA17K assembler package. Figure 4-1 shows the output format assembled using the AS17933, 17933A, 17934, and 17934A.

Note Manufactured by I.C Corp.

Figure 4-1. ICE File Format (1/2)

★ **(a) AS17933, 17933A**

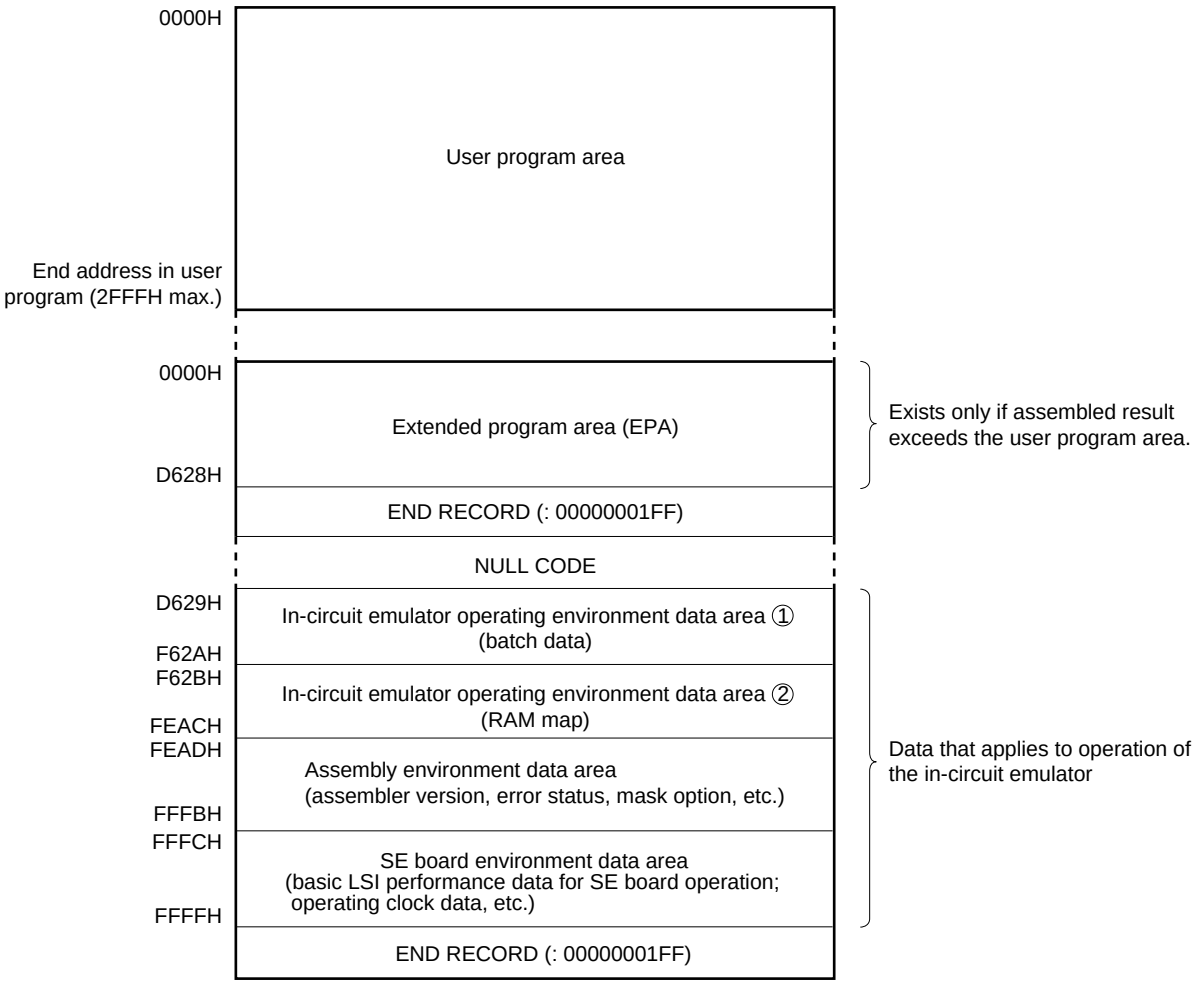
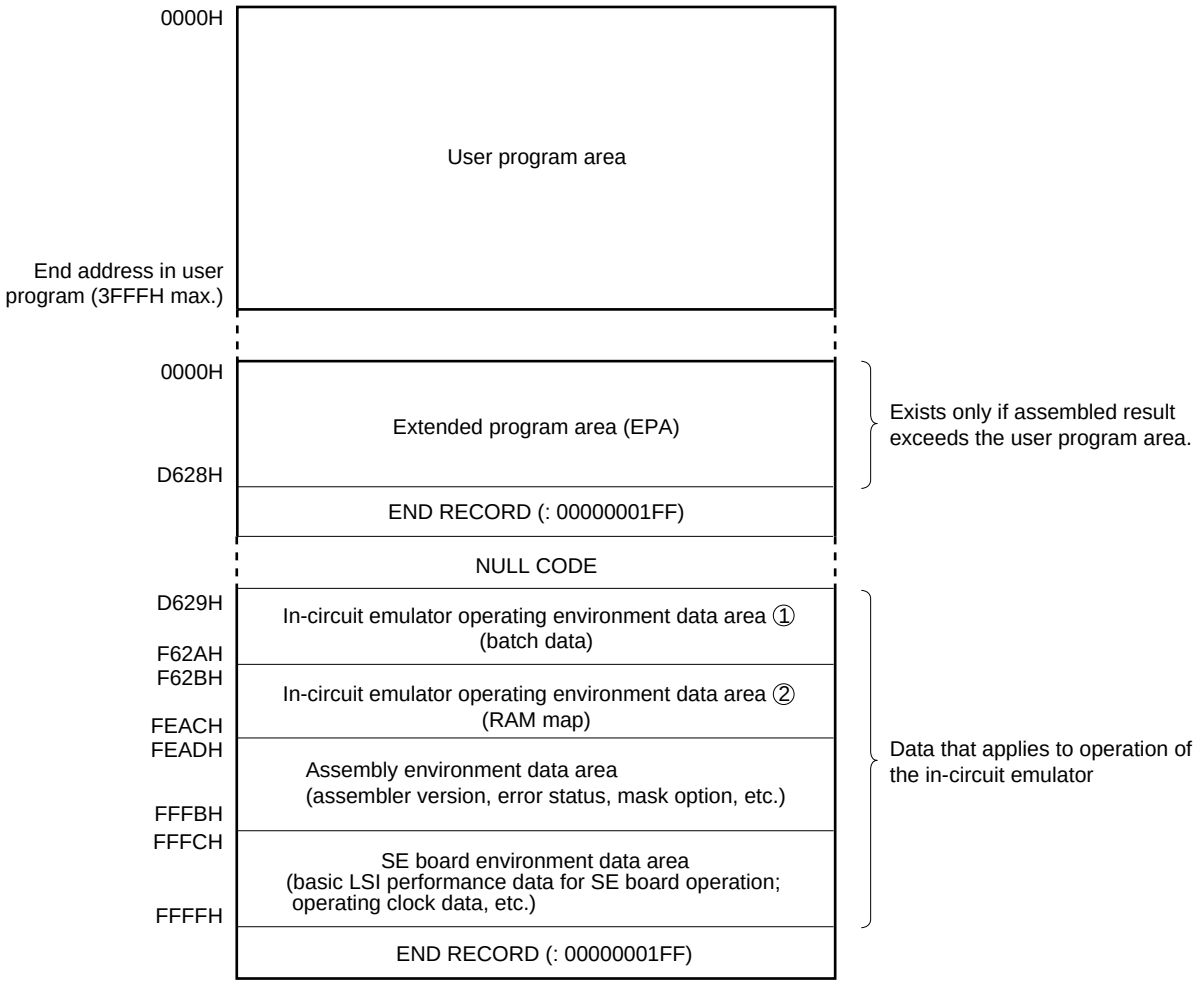


Figure 4-1. ICE File Format (2/2)

★ **(b) AS17934, 17934A**



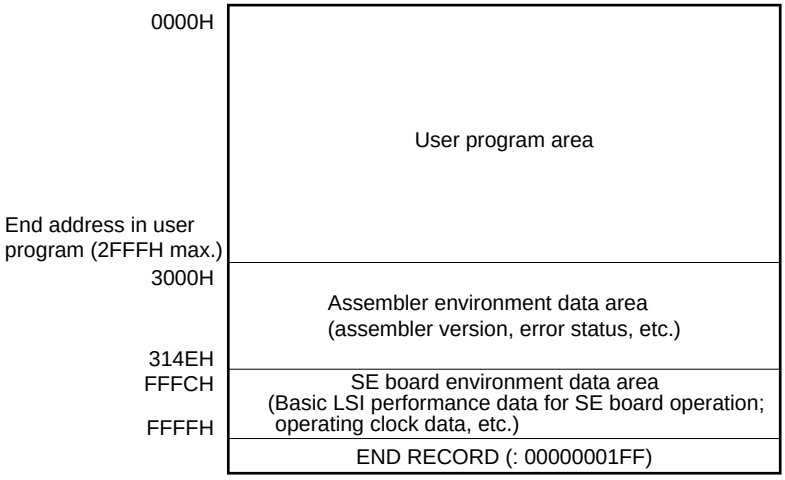
(3) PRO files

PRO files are output as HEX-format files exclusive to the PROM and one-time PROM products that are used for mask order and stand-alone SE board evaluations that are output by the RA17K assembler package. These are output when "/PRO" is specified as an assembly option during assembly.

★ Figure 4-2 shows the output format assembled using the AS17933, 17933A, 17934, and 17934A.

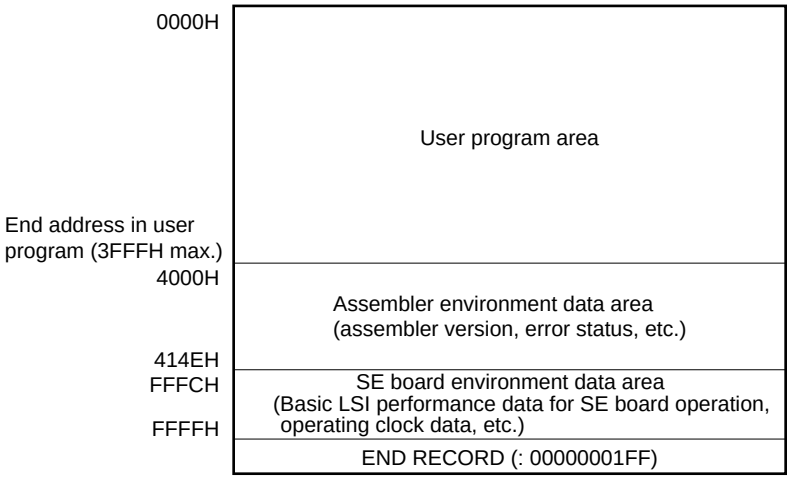
Figure 4-2. PRO File Format

★ **(a) AS17933, 17933A**



Remark The range of 314FH to FFFBH does not exist in PRO files.

★ **(b) AS17934, 17934A**



Remark The range of 414FH to FFFBH does not exist in PRO files.

(4) File comparison of load module files

Even when there are no changes in the source file, changes may occur in the assembler output results (i.e., the assembly environment data area). This is because the data in the assembly environment data area includes items such as the source file creation date.

Table 4-1. Items Whose Assembler Output Result May Change Even When Source File Has No Change (1/2)

★ **(a) AS17933, 17933A**

Item	Address	
	ICE file	PRO file
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FEADH - FECCH	3000H - 301FH
SIMPLEHOST information	FFADH	3100H
Error or warning status	FFB0H	3103H
File creation date and time **Note**	FFBEH - FFC7H	3111H - 311AH
Device name	FFC8H - FFD7H	311BH - 312AH
Device file version	FFDDH	3130H
Assembler version	FFE1H	3134H

Note The creation date/time of the most recent source file or sequence file is written.

Caution Do not make changes to load module files only.
Change load module files by changing the source file and then reassembling. Revising load module files only may cause the histories of the other files to become mismatched, resulting in bugs.

Table 4-1. Items Whose Assembler Output Result May Change Even When Source File Has No Change (2/2)

★ **(b) AS17934, 17934A**

Item	Address	
	ICE file	PRO file
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FEADH - FECCH	4000H - 401FH
SIMPLEHOST information	FFADH	4100H
Error or warning status	FFB0H	4103H
File creation date and time **Note**	FFBEH - FFC7H	4111H - 411AH
Device name	FFC8H - FFD7H	411BH - 412AH
Device file version	FFDDH	4130H
Assembler version	FFE1H	4134H

Note The creation date/time of the most recent source file or sequence file is written.

Caution Do not make changes to load module files only.
Change load module files by changing the source file and then reassembling. Revising load module files only may cause the histories of the other files to become mismatched, resulting in bugs.

NEC

Facsimile Message

From:

Name

Company

Tel. FAX

Address

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

Thank you for your kind support.

North America
NEC Electronics Inc.
Corporate Communications Dept.
Fax: 1-800-729-9288
1-408-588-6130

Europe
NEC Electronics (Europe) GmbH
Technical Documentation Dept.
Fax: +49-211-6503-274

South America
NEC do Brasil S.A.
Fax: +55-11-6465-6829

Hong Kong, Philippines, Oceania
NEC Electronics Hong Kong Ltd.
Fax: +852-2886-9022/9044

Korea
NEC Electronics Hong Kong Ltd.
Seoul Branch
Fax: 02-528-4411

Taiwan
NEC Electronics Taiwan Ltd.
Fax: 02-2719-5951

Asian Nations except Philippines
NEC Electronics Singapore Pte. Ltd.
Fax: +65-250-3583

Japan
NEC Semiconductor Technical Hotline
Fax: 044-548-7900

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity	❑	❑	❑	❑
Technical Accuracy	❑	❑	❑	❑
Organization	❑	❑	❑	❑