# BLD6G21L-50; BLD6G21LS-50

TD-SCDMA 2010 MHz to 2025 MHz fully integrated Doherty transistor

Rev. 2 — 17 August 2010

**Product data sheet** 

## 1. Product profile

### 1.1 General description

The BLD6G21L-50 and BLD6G21LS-50 incorporate a fully integrated Doherty solution using NXP's state of the art GEN6 LDMOS technology. This device is perfectly suited for TD-SCDMA base station applications at frequencies from 2010 MHz to 2025 MHz. The main and peak device, input splitter and output combiner are integrated in a single package. This package consists of one gate and drain lead and two extra leads of which one is used for biasing the peak amplifier and the other is not connected. It only requires the proper input/output match and bias setting as with a normal class-AB transistor.

**Table 1. Typical performance** *RF performance at T<sub>h</sub> = 25 °C.* 

Mode of operation	f	V <sub>DS</sub>	P <sub>L(AV)</sub>	Gp	$\eta_{D}$	ACPR	P <sub>L(3dB)</sub>
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)	(W)
TD-SCDMA [1][2]	2010 to 2025	28	8	14.5	43	-24	53

<sup>[1]</sup> Test signal: 6-carrier TD-SCDMA; PAR = 10.8 dB at 0.01 % probability on CCDF.

#### **CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

#### 1.2 Features and benefits

- Typical TD-SCDMA performance at frequencies from 2010 MHz to 2025 MHz:
  - ◆ Average output power = 8 W
  - ◆ Power gain = 14.5 dB
  - ◆ Efficiency = 43 %
- Fully optimized integrated Doherty concept:
  - integrated asymmetrical power splitter at input
  - integrated power combiner
  - peak biasing down to 0 V
  - low junction temperature
  - high efficiency
- 100 % peak power tested for guaranteed output power capability



<sup>[2]</sup>  $I_{Dq} = 170 \text{ mA (main)}$ ;  $V_{GS(amp)peak} = 0 \text{ V}$ .

- Integrated ESD protection
- Good pair match (main and peak on the same chip)
- Independent control of main and peak bias
- Internally matched for ease of use
- Excellent ruggedness
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

High efficiency RF power amplifiers with digital pre-distortion for TD-SCDMA multi carrier applications in the 2010 MHz to 2025 MHz range.

# 2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol		
BLD6G2	1L-50 (SOT1130A)					
1	drain					
2	gate + bias main		1	. 1		
3	source	<u>[1]</u>		2		
4	n.c.		3	2 7 7 3		
5	bias peak		4 5	001aak920		
BLD6G2	1LS-50 (SOT1130B)					
1	drain					
2	gate + bias main		1	1		
3	source	<u>[1]</u>		2		
4	n.c.		3	2 7 3		
5	bias peak		2 5	001aak920		

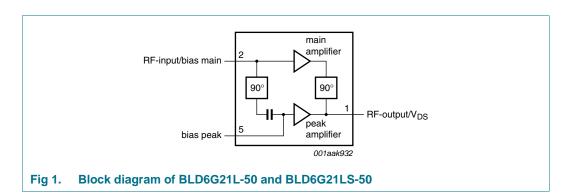
<sup>[1]</sup> Connected to flange.

# 3. Ordering information

Table 3. Ordering information

Type number	Packag	Package				
	Name	Description	Version			
BLD6G21L-50	-	flanged ceramic package; 2 mounting holes; 4 leads	SOT1130A			
BLD6G21LS-50	-	earless flanged ceramic package; 4 leads	SOT1130B			

#### **Block diagram** 4.



#### **Limiting values** 5.

#### **Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Valid for both main and peak device.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
V <sub>GS(amp)main</sub>	main amplifier gate-source voltage		-0.5	+13	V
V <sub>GS(amp)peak</sub>	peak amplifier gate-source voltage		-0.5	+13	V
I <sub>D</sub>	drain current		-	10.2	Α
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature		-	200	°C

### Thermal characteristics

Table 5. **Thermal characteristics** 

Symbol	Parameter	Conditions	Тур	Unit
$R_{th(j\text{-case})}$	thermal resistance from junction to case	$T_{case}$ = 80 °C; $P_L$ = 8 W	<u>11</u> 2.1	K/W

<sup>[1]</sup> When operated with a 6-carrier TD-SCDMA modulated signal with PAR = 10.8 dB at 0.01 % probability on CCDF.

#### **Characteristics** 7.

**Characteristics** Table 6.

Valid for both main and peak device.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.62 \text{ mA}$	65	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$V_{DS} = 10 \text{ V}; I_{D} = 31 \text{ mA}$	1.4	1.8	2.4	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28 \text{ V}; I_{D} = 170 \text{ mA}$	1.55	2.05	2.55	V
I <sub>DSS</sub>	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$	-	-	1.4	μΑ
I <sub>DSX</sub>	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	4.95	5.5	-	Α

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**Table 6.** Characteristics ...continued Valid for both main and peak device.

	•					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$I_{GSS}$	gate leakage current	$V_{GS} = 11 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	140	nA
9fs	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 1.55 \text{ A}$	1.4	2.2	-	S
$R_{DS(on)} \\$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_{D} = 1.085 \text{ A}$	-	0.52	0.736	Ω

# 8. Application information

#### Table 7. Application information

Mode of operation: 6-carrier TD-SCDMA; PAR 10.8 dB at 0.01 % probability on CCDF; f = 2017.5 MHz; RF performance at  $V_{DS} = 28$  V;  $I_{Dq} = 170$  mA;  $V_{GS(amp)peak} = 0$  V;  $T_{case} = 25$  °C; unless otherwise specified; in a production circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$P_{L(AV)}$	average output power		-	8	-	W
Gp	power gain	$P_{L(AV)} = 8 W$	13	14.5	-	dB
$\eta_{D}$	drain efficiency	$P_{L(AV)} = 8 W$	39	43	-	%
PARO	output peak-to-average ratio	$P_{L(AV)} = 8 W$	-	9.4	-	dB
RLin	input return loss	$P_{L(AV)} = 8 W$	8	23	-	dB
ACPR	adjacent channel power ratio	$P_{L(AV)} = 8 W$	-	-24	-20	dBc

#### Table 8. Application information

Mode of operation: Pulsed CW;  $\delta$  = 10 %;  $t_p$  = 100  $\mu$ s; RF performance at  $V_{DS}$  = 28 V;  $I_{Dq}$  = 170 mA;  $V_{GS(amp)peak}$  = 0 V;  $T_{case}$  = 25 °C; unless otherwise specified; in a production circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
P <sub>L(3dB)</sub>	output power at 3 dB gain compression		46	53	-	W

#### 8.1 Ruggedness in Doherty operation

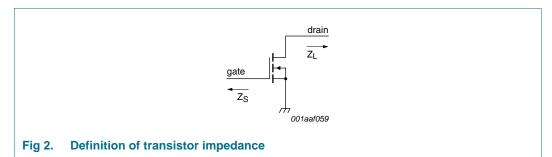
The BLD6G21L-50 and BLD6G21LS-50 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 170 \text{ mA}$ ;  $P_L = 8 \text{ W}$  (TD-SCDMA); f = 2017.5 MHz.

### 8.2 Impedance information

Table 9. Typical impedance

Measured Load Pull data; typical values unless otherwise specified.

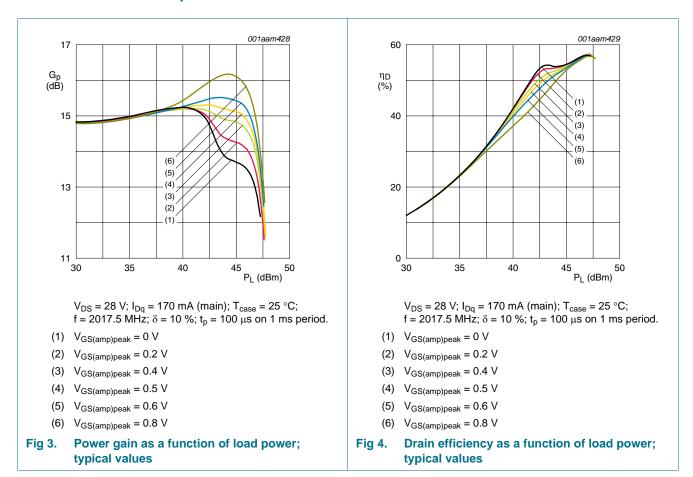
f	Z <sub>S</sub>	Z <sub>L</sub>
MHz	Ω	Ω
1995	3.5 – 12.3j	6.7 – 6.1j
2010	3.6 – 12.7j	6.7 – 6.1j
2017.5	3.6 – 12.7j	6.7 – 5.7j
2025	3.7 – 12.7j	6.4 – 5.2j
2040	4.0 – 12.9j	5.7 – 4.8j

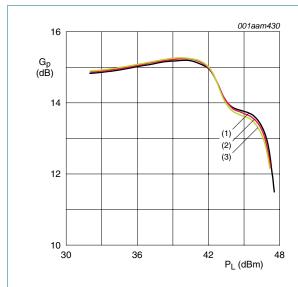


8.3 Performance curves

Performance curves are measured in a BLD6G21L-50 application circuit.

#### 8.3.1 CW pulsed

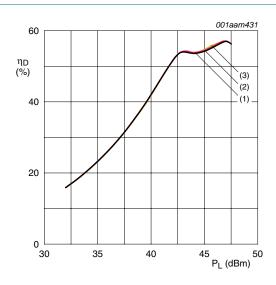




 $V_{DS}$  = 28 V;  $I_{Dq}$  = 170 mA (main);  $T_{case}$  = 25 °C;  $V_{GS(amp)peak}$  = 0 V;  $\delta$  = 10 %;  $t_p$  = 100  $\mu s$  on 1 ms period.

- (1) f = 2010 MHz
- (2) f = 2018 MHz
- (3) f = 2025 MHz

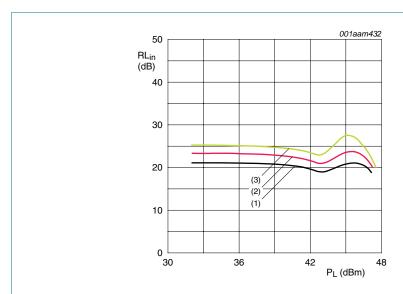
Fig 5. Power gain as a function of load power; typical values



$$\begin{split} V_{DS} = 28 \text{ V; } I_{Dq} = 170 \text{ mA (main); } T_{case} = 25 \text{ °C;} \\ V_{GS(amp)peak} = 0 \text{ V; } \delta = 10 \text{ %; } t_p = 100 \text{ } \mu\text{s on 1 ms period.} \end{split}$$

- (1) f = 2010 MHz
- (2) f = 2018 MHz
- (3) f = 2025 MHz

Fig 6. Drain efficiency as a function of load power; typical values

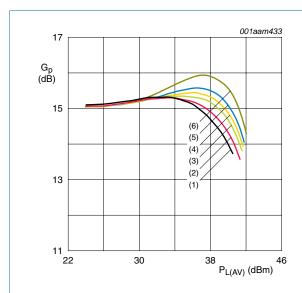


 $V_{DS} = 28 \text{ V}; \text{ I}_{Dq} = 170 \text{ mA}; \text{ V}_{GS(amp)peak} = 0 \text{ V}; \text{ T}_{case} = 25 \text{ °C}; \text{ } \delta = 10 \text{ \%}; \text{ } t_p = 100 \text{ } \mu s \text{ on 1 ms period.}$ 

- (1) f = 2010 MHz
- (2) f = 2018 MHz
- (3) f = 2025 MHz

Fig 7. Input return loss as a function of load power; typical values

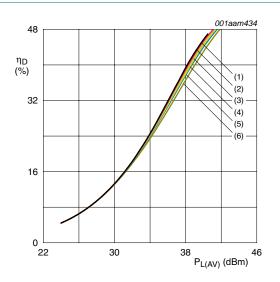
#### 8.3.2 TD-SCDMA



 $V_{DS}=28$  V;  $I_{Dq}=170$  mA (main);  $T_{case}=25\,^{\circ}\text{C};$  f=2017.5 MHz; 6-carrier TD-SCDMA; PAR = 10.8 dB at 0.01 % probability on CCDF.

- (1)  $V_{GS(amp)peak} = 0 V$
- (2)  $V_{GS(amp)peak} = 0.2 \text{ V}$
- (3)  $V_{GS(amp)peak} = 0.4 \text{ V}$
- (4)  $V_{GS(amp)peak} = 0.5 \text{ V}$
- (5)  $V_{GS(amp)peak} = 0.6 \text{ V}$
- (6)  $V_{GS(amp)peak} = 0.8 \text{ V}$

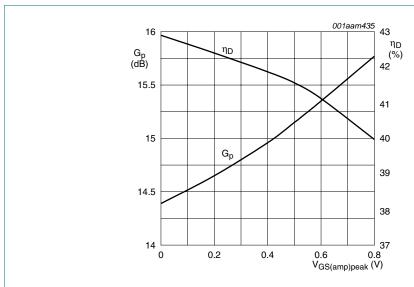
Fig 8. Power gain as a function of average load power; typical values



 $V_{DS}$  = 28 V;  $I_{Dq}$  = 170 mA (main);  $T_{case}$  = 25 °C; f = 2017.5 MHz; 6-carrier TD-SCDMA; PAR = 10.8 dB at 0.01 % probability on CCDF.

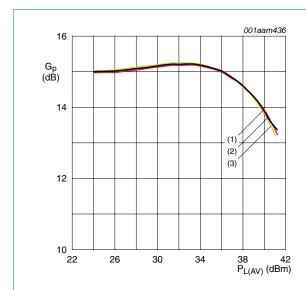
- (1)  $V_{GS(amp)peak} = 0 V$
- (2)  $V_{GS(amp)peak} = 0.2 \text{ V}$
- (3)  $V_{GS(amp)peak} = 0.4 \text{ V}$
- (4)  $V_{GS(amp)peak} = 0.5 V$
- (5)  $V_{GS(amp)peak} = 0.6 \text{ V}$
- (6)  $V_{GS(amp)peak} = 0.8 \text{ V}$

Fig 9. Drain efficiency as a function of average load power; typical values



 $V_{DS}=28~V;~I_{Dq}=170~mA;~P_{L(AV)}=8~W;~T_{case}=25~^{\circ}C;~f=2017.5~MHz;~6-carrier~TD-SCDMA;~PAR=10.8~dB~at~0.01~\%~probability~on~CCDF.$ 

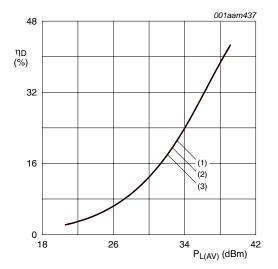
Fig 10. Power gain and drain efficiency as function of peak amplifier gate-source voltage; typical values



 $V_{DS}$  = 28 V;  $I_{Dq}$  = 170 mA (main);  $T_{case}$  = 25 °C;  $V_{GS(amp)peak}$  = 0 V; 6-carrier TD-SCDMA; PAR = 10.8 dB at 0.01 % probability on CCDF.

- (1) f = 2010 MHz
- (2) f = 2018 MHz
- (3) f = 2025 MHz

Fig 11. Power gain as a function of average load power; typical values

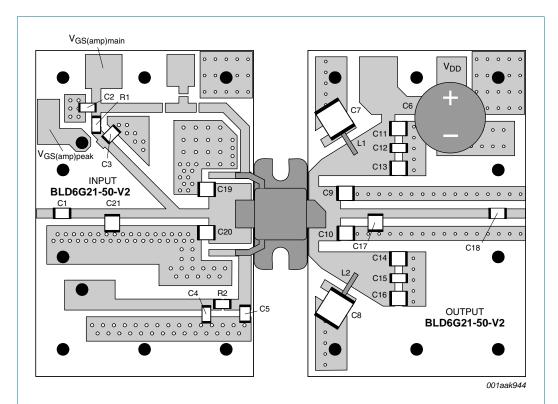


 $V_{DS}$  = 28 V;  $I_{Dq}$  = 170 mA (main);  $T_{case}$  = 25 °C;  $V_{GS(amp)peak}$  = 0 V; 6-carrier TD-SCDMA; PAR = 10.8 dB at 0.01 % probability on CCDF.

- (1) f = 2010 MHz
- (2) f = 2018 MHz
- (3) f = 2025 MHz

Fig 12. Drain efficiency as a function of average load power; typical values

### 9. Test information



The striplines are on a double copper-clad gold plated Rogers 4350B Printed-Circuit Board (PCB) with  $\epsilon_{\rm r}=3.5$  and thickness = 0.76 mm.

See Table 10 for list of components.

Fig 13. Component layout

**Table 10.** List of components See Figure 13 for component layout.

Component	Description	Value	Dimensions
C1, C3, C5, C18	multilayer ceramic chip capacitor	9.1 pF	[1]
C2, C4, C12, C15	multilayer ceramic chip capacitor	100 nF	
C6	electrolytic capacitor	470 $\mu F$ ; 63 V	
C7, C8	multilayer ceramic chip capacitor	10 μF	
C9, C10	multilayer ceramic chip capacitor	1.5 pF	[1]
C11, C13, C14, C16	multilayer ceramic chip capacitor	8.2 pF	[1]
C17	multilayer ceramic chip capacitor	1.2 pF	[1]
C19, C20	multilayer ceramic chip capacitor	0.7 pF	[1]
C21	multilayer ceramic chip capacitor	1.2 pF	[1]
L1, L2	copper wire	-	diameter = 0.8 mm; length = 8 mm
R1	SMD resistor	$3.6 \Omega$	1206
R2	SMD resistor	33 Ω	1206

<sup>[1]</sup> American Technical Ceramics type 100B or capacitor of same quality.

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# 10. Package outline

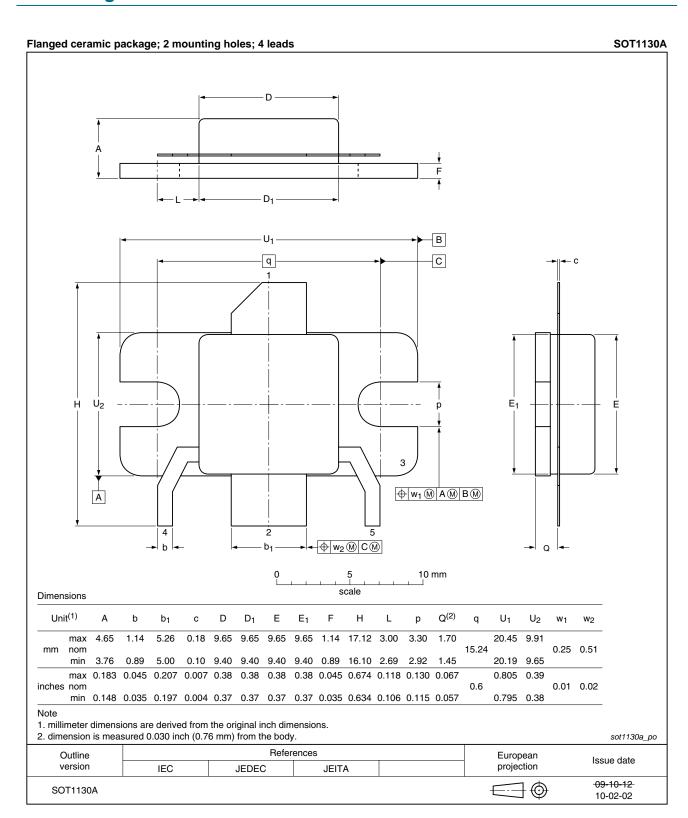


Fig 14. Package outline SOT1130A

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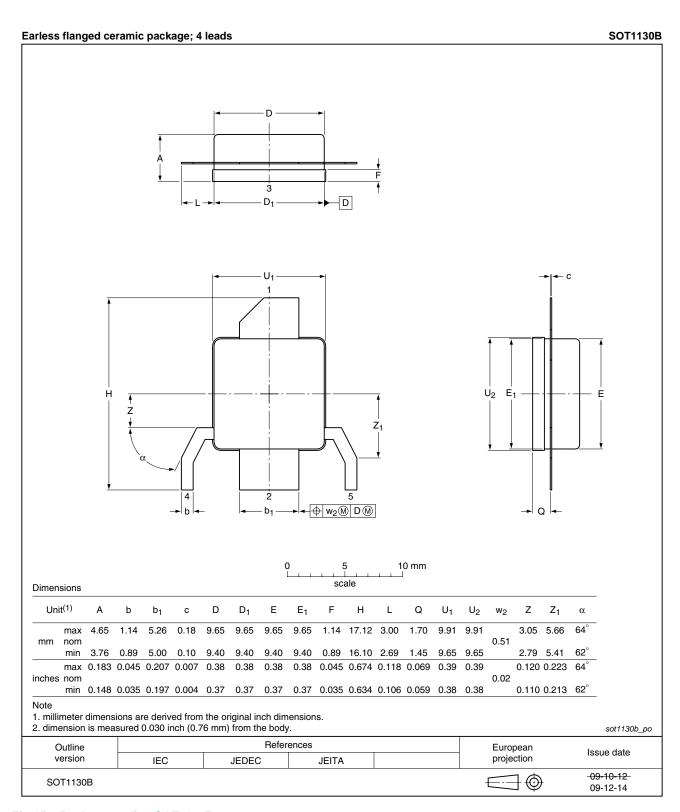


Fig 15. Package outline SOT1130B

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# 11. Abbreviations

Table 11. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
SMD	Surface Mounted Device
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
VSWR	Voltage Standing-Wave Ratio

# 12. Revision history

#### Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLD6G21L-50_BLD6G21LS-50 v.2	20100817	Product data sheet	-	BLD6G21L-50_ BLD6G21LS-50 v.1	
Modifications:	<ul> <li>Figure 1 on page 3: Some corrections have been made.</li> </ul>				
	<ul> <li><u>Table 5 on page 3</u>: The typical value of R<sub>th(j-case)</sub> has been changed.</li> </ul>				
	<ul> <li><u>Table 6 on page 3</u>: The values of I<sub>DSX</sub> have been changed.</li> </ul>				
	<ul> <li><u>Table 7 on page 4</u>: Several values have been changed or added.</li> </ul>				
	<ul> <li><u>Table 8 on page 4</u>: Table has been added.</li> </ul>				
	<ul> <li>Section 8.3 on page 5: Figures have been updated.</li> </ul>				
BLD6G21L-50_BLD6G21LS-50 v.1	20091028	Objective data sheet	-	-	

# BLD6G21L-50; BLD6G21LS-50

#### TD-SCDMA 2010 MHz to 2025 MHz fully integrated Doherty transistor

# 13. Legal information

#### 13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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#### TD-SCDMA 2010 MHz to 2025 MHz fully integrated Doherty transistor

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### **NXP Semiconductors**

# BLD6G21L-50; BLD6G21LS-50

# TD-SCDMA 2010 MHz to 2025 MHz fully integrated Doherty transistor

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