

PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2	86	DQ36	128	NC
3	DQ1	45	RAS2	87	DQ37	129	NC
4	DQ2	46	CAS2	88	DQ38	130	CAS6
5	DQ3	47	CAS3	89	DQ39	131	CAS7
6	Vcc	48	WE2	90	Vcc	132	NC
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ58
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	Vss	106	DQ53	148	Vss
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0	69	DQ28	111	NC	153	DQ64
28	CAS0	70	DQ29	112	CAS4	154	DQ65
29	CAS1	71	DQ30	113	CAS5	155	DQ66
30	RAS0	72	DQ31	114	NC	156	DQ67
31	OE0	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	NC	167	SA2
42	NC	84	Vcc	126	NC	168	Vcc

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SERIAL PD BYTE DEFINITION

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE
Byte 0	Number of Byte written during module production	15 Bytes	0Fh
Byte 1	Total Byte of Serial Presence Detect Device	256 Bytes	08h
Byte 2	Memory Type	EDO	02h
Byte 3	Number of ROW Addresses	11	0Bh
Byte 4	Number of COLUMN Addresses	11	0Bh
Byte 5	Number of Banks	1 Bank	01h
Byte 6	Module Data Width	72bit	48h
Byte 7	Module Data Width(Continued)	Not Used	00h
Byte 8	Module Interface Levels	LVTTTL	01h
Byte 9	tRAC	60ns	3Ch
		70ns	46h
		80ns	50h
Byte 10	tCAC	15ns	0Fh
		18ns	12h
		20ns	14h
Byte 11	Module Configuration Type	ECC	02h
Byte 12	Refresh Rate/Type	Normal(15.6μs)	00h
		SL-Part(125μs)	85h
Byte 13	Primary DRAM Width	x4	04h
Byte 14	Error Checking DRAM width	x4	04h
Byte 15 - 255	Undefined	Undefined	Undefined

NOTE:

1. Serial PD interface is standard IIC architecture.
2. Pull-up resistors(4.7K typical value) are required on all open collector bus devices (SCL and SDA).
3. Current sink capability on SCL and SDA (IOL max) must be at least 3ma to maintain a valid low level.

IIC BUS INTERFACE

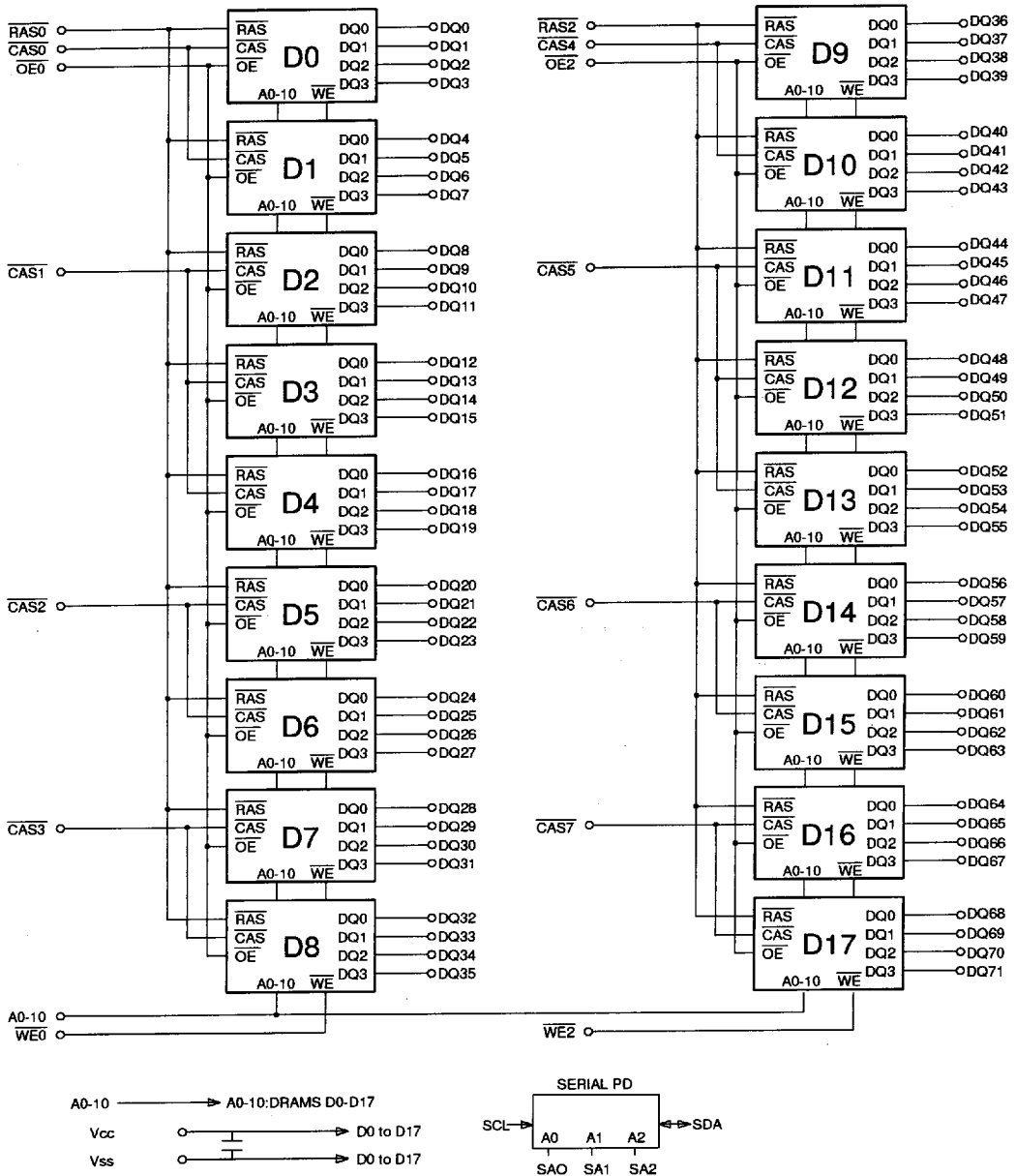
SYMBOL	RATING	NOTE
C _{MAX}	400pF	1
f _{MAX}	80 KHz(3.3V) 100 KHz(5.0V)	2
IOL _{MAX}	3mA	

NOTE:

1. The maximum number of devices connected on the IIC bus is controlled by the maximum allowable capacitance which is 400pF per line.
2. The maximum IIC system clock frequency depends on Vcc.

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 125	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-0.5 to 4.6	V
VCC	Voltage on VCC Relative to Vss	-0.5 to 4.6	V
Ios	Short Circuit Output Current	20	mA
Pd	Power Dissipation	18	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	3.0	3.3	3.6	V
VIH	Input High Voltage	2.0	-	VCC+ 0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

NOTE : All voltages are referenced to Vss.

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DC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 3.3V± 10%, Vss= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	Vss ≤ VIN ≤ Vcc + 1.0, other pins not under test = Vss		-180	180	μA	
ILO	Output Leakage Current (High Impedance State)	Vss ≤ VOUT ≤ Vcc, RAS & CAS at VIH		-10	10	μA	
Icc1	Vcc Supply Current, Operating	tRC= tRC (min.)	60 70 80	-	2160 1800 1620	mA	1,2,3
Icc2	Vcc Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ Vss		-	36	mA	
Icc3	Vcc Supply Current, RAS-only refresh	tRC= tRC (min.)	60 70 80	-	2160 1800 1620	mA	1,3
Icc4	Vcc Supply Current, EDO mode	tHPC= tHPC (min.)	60 70 80	-	1800 1620 1440	mA	1,2,3
Icc5	Vcc Supply Current, CMOS Standby	RAS & CAS ≥ Vcc - 0.2V	SL-part	-	18 7.2	mA	
Icc6	Vcc Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	60 70 80	-	2160 1800 1620	mA	1,3
Icc7	Vcc Supply Current, Battery Back Up (SL-part only)	tRC= 125μs CAS= CBR cycling or 0.2V WE= Vcc - 0.2V, A0-A10= Vcc - 0.2V or 0.2V DQ0-DQ71= Vcc - 0.2V, 0.2V or open	tRAS ≤ 300ns tRAS ≤ 1μs	-	6.3 10.8	mA	1,4,5
Icc8	Vcc Supply Current, Self Refresh (SL-part)	RAS & CAS= VIL OE & WE & A0-A10= Vcc 0.2V or 0.2V DQ0-DQ71= Vcc - 0.2V, or 0.2V or open		-	5.4	mA	5
VOL	Output Low Voltage	IOL= 2.0mA		-	0.4	V	
VOH	Output High Voltage	IOH= -2.0mA		2.4	-	V	

NOTE :

- Icc1, Icc3, Icc4, Icc6 and Icc7 depend on cycle rate.
- Icc1, Icc3, Icc4, and Icc6 depend on output loading. Specified values are obtained with the output open.
- Icc is specified as average current. For Icc1, Icc3 and Icc6, address can be changed maximum two times while RAS= VIL. For Icc4, address can be changed maximum once while CAS= VIH.
- tRAS(max.)= 1μs is only applied to refresh of battery backup but tRAS(max.)= 10μs is applied to normal functional operatin.
- Icc5(max.)= 7.2mA, Icc7 and Icc8 are applied to SL-part only (HYM5V72A414ASLKG/ASLTKG).

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AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM5V72A414A K-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	180	-	200	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	75	-	85	-	95	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	3	-	3	-	3	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	3	15	3	18	3	20	ns	5
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASp	RAS Pulse Width (EDO Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	RAS Hold Time	15	-	18	-	20	-	ns	
16	tCSH	CAS Hold Time	45	-	50	-	55	-	ns	
17	tCAS	CAS Pulse Width	11	10K	14	10K	17	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	17	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	12	-	14	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	12	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	50	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	50	-	55	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

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AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM5V72A414A K-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	40	-	45	-	50	-	ns	8
42	tRWD	RAS to WE Delay Time	80	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	50	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	10	-	10	-	ns	
49	tOEA	OE Access Time	-	15	-	18	-	20	ns	
50	tOED	OE to Data Delay	15	-	18	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	3	15	3	18	3	20	ns	5
52	tOEH	OE Command Hold Time	15	-	18	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	35	-	40	-	45	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	μs	
58	tRPS	RAS Precharge Time (Self Refresh Cycle)	90	-	110	-	130	-	ns	
59	tCHS	CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
60	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
61	tREZ	Output Buffer Turn-off Delay (RAS)	3	15	3	18	3	20	ns	5,15
62	tWEZ	Output Buffer Turn-off Delay (WE)	3	15	3	18	3	20	ns	5
63	tWPE	WE Pulse Width for Output Disable	5	-	8	-	10	-	ns	
64	tOEP	OE Pulse Width for Output Disable	5	-	8	-	10	-	ns	
65	tOCH	OE Low to CAS High Delay Time	0	-	0	-	0	-	ns	
66	tCHO	CAS High to OE High Hold Time	5	-	8	-	10	-	ns	
67	tWED	WE to Data Delay Time	15	-	18	-	20	-	ns	

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NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ -only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{\text{RAS}} = \text{Vss}$ during power-up, the HYM5V72A414A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. Refer to the HY51V17404A data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF. ($\text{VOH} = 2.0\text{V}, \text{VOL} = 0.8\text{V}$)
5. $\text{tCEZ}(\text{max.})$, $\text{tOEZ}(\text{MAX})$, $\text{tREZ}(\text{MAX})$ and $\text{tWEZ}(\text{MAX})$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either trCH or trRH must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in late write or read-modify-write cycles.
8. twCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $\text{twCS} \geq \text{twCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $\text{trCD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met. $\text{trCD}(\text{max.})$ is specified as a reference point only. If trCD is greater than the specified $\text{trCD}(\text{max.})$ limit, then access time is controlled by tCAC .
10. Operation within the $\text{trAD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met. $\text{trAD}(\text{max.})$ is specified as a reference point only. If trAD is greater than the specified $\text{trAD}(\text{max.})$ limit, then access time is controlled by tAA .
11. Measured with the specified current load and 100pF.
12. A burst of 2048 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles must be executed within 32ms after exiting self refresh (for SL-part).
13. If $\text{tcWD} \geq \text{twCS}(\text{MIN.})$, $\text{trWD} \geq \text{trWD}(\text{MIN.})$, $\text{tAWD} \geq \text{tAWD}(\text{MIN.})$ and $\text{tcpWD} \geq \text{tcpWD}(\text{MIN.})$, the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{\text{CAS}}$ goes back to VIH) is indeterminated.
14. In $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh mode.
 In case of using distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, refresh 2048 times during a 256ms after reset
 In case of using burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, refresh 2048 times during a 32ms after reset
 In case of using $\overline{\text{RAS}}$ only refresh, refresh against all refresh address during a 32ms after reset
15. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.

CAPACITANCE

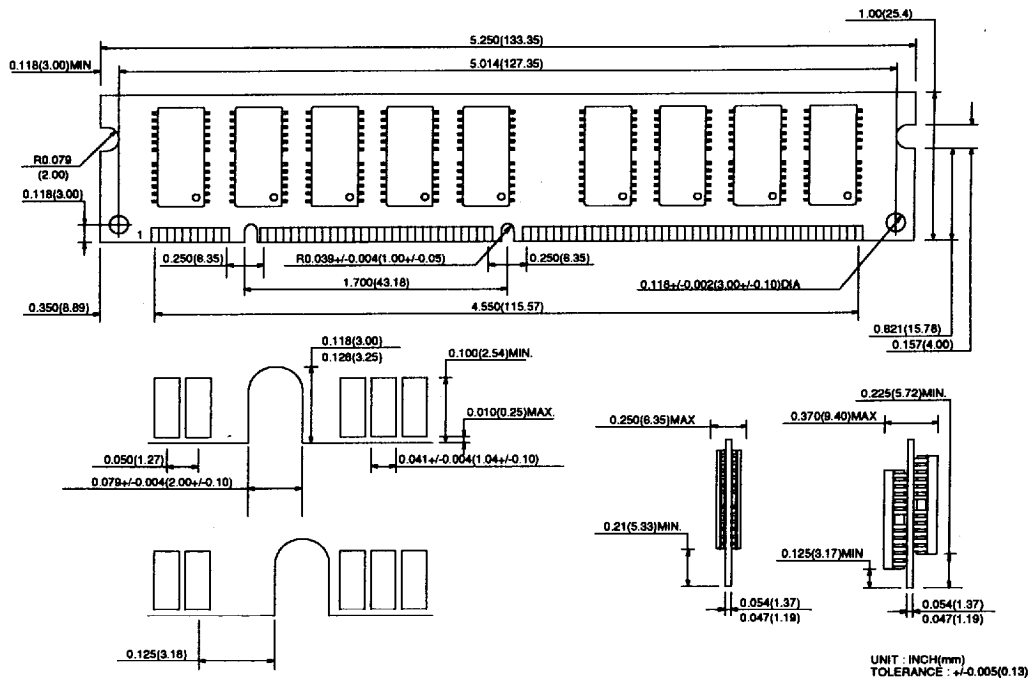
($\text{TA} = 25^\circ\text{C}$, $\text{Vcc} = 3.3\text{V} \pm 10\%$, $\text{Vss} = 0\text{V}$, $f = 1\text{MHz}$, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	100	pF
CIN2	Input Capacitance ($\overline{\text{WE}}0, \overline{\text{WE}}2, \text{OE}0, \text{OE}2$)	-	73	pF
CIN3	Input Capacitance ($\overline{\text{RAS}}0, \overline{\text{RAS}}2$)	-	70	pF
CIN4	Input Capacitance ($\overline{\text{CAS}}0 - \overline{\text{CAS}}7$)	-	13	pF
CDQ	Data Input/output Capacitance (DQ0-DQ71)	-	15	pF

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PACKAGE INFORMATION

168 pin Unbuffered Dual In-line Memory Module (KG ; Gold plated)



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ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V72A414AKG	60/70/80		DIMM	Gold
HYM5V72A414ASLKG	60/70/80	SL-part	DIMM	Gold
HYM5V72A414ATKG	60/70/80		DIMM	Gold
HYM5V72A414ASLTKG	60/70/80	SL-part	DIMM	Gold

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