

FPM DRAM

MT4C1M16C3, MT4LC1M16C3

For the latest data sheet revisions, please refer to the Micron Website: www.micron.com/datasheets

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts, and packages
- High-performance, low-power CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or 5V ±0.5V)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- Optional self refresh (S) for low-power data retention
- BYTE WRITE and BYTE READ access cycles
- 1,024-cycle refresh (10 row, 10 column addresses)
- FAST-PAGE-MODE (FPM) access

OPTIONS

- Voltage¹
3.3V
5V

Packages

Plastic SOJ (400 mil)
Plastic TSOP (400 mil)

Timing

50ns access -5
60ns access -6

Refresh Rates

Standard Refresh (16ms period) None
Self Refresh (128ms period) S²

Operating Temperature Range

Commercial (0°C to +70°C) None
Extended (-20°C to +80°C) ET³

MARKING

LC
C

DJ
TG

Part Number Example:

MT4LC1M16C3DJ-5

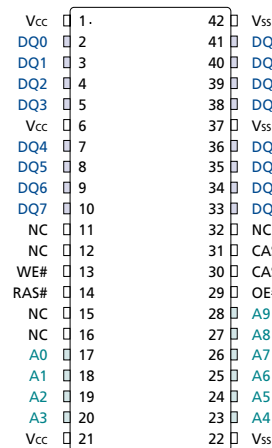
- NOTE: 1. The third field distinguishes the low voltage offering: LC designates Vcc = 3.3V and C designates Vcc = 5V.
2. Contact factory for availability.
3. Available only on MT4C1M16C3 (5V)

KEY TIMING PARAMETERS

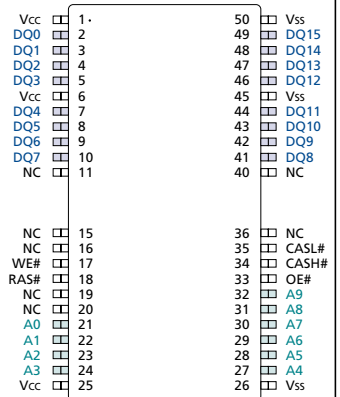
SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{RP}
-5	84ns	50ns	20ns	25ns	15ns	30ns
-6	110ns	60ns	35ns	30ns	15ns	40ns

PIN ASSIGNMENT (Top View)

42-Pin SOJ



44/50-Pin TSOP



NOTE: The # symbol indicates signal is active LOW.

1 MEG x 16 FPM DRAM PART NUMBERS

PART NUMBER	SUPPLY	PACKAGE	REFRESH
MT4LC1M16C3DJ-6	3.3V	SOJ	Standard
MT4LC1M16C3DJ-6 S	3.3V	SOJ	Self
MT4LC1M16C3TG-6	3.3V	TSOP	Standard
MT4LC1M16C3TG-6 S	3.3V	TSOP	Self
MT4C1M16C3DJ-6	5V	SOJ	Standard
MT4C1M16C3TG-6	5V	TSOP	Standard

GENERAL DESCRIPTION

The 1 Meg x 16 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x16 configuration. The 1 Meg x 16 DRAM has both BYTE WRITE and WORD WRITE access cycles via two CAS# pins (CASL# and CASH#). These function identically to a single CAS# on other DRAMs in that either CASL# or CASH# will generate an internal CAS#.

The CAS# function and timing are determined by the first CAS# (CASL# or CASH#) to transition LOW and

GENERAL DESCRIPTION (continued)

the last CAS# to transition back HIGH. Use of only one of the two results in a BYTE access cycle. CASL# transitioning LOW selects an access cycle for the lower byte (DQ0-DQ7), and CASH# transitioning LOW selects an access cycle for the upper byte (DQ8-DQ15).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered ten bits (A0-A9) at a time. RAS# is used to latch the first ten bits and CAS# the latter ten bits. The CAS# function is determined by the first CAS# (CASL# or CASH#) to transition LOW and the last one to transition back HIGH. The CAS# function also determines whether the cycle will be a refresh cycle (RAS#-ONLY) or an active cycle (READ, WRITE, or READ-WRITE) once RAS# goes LOW.

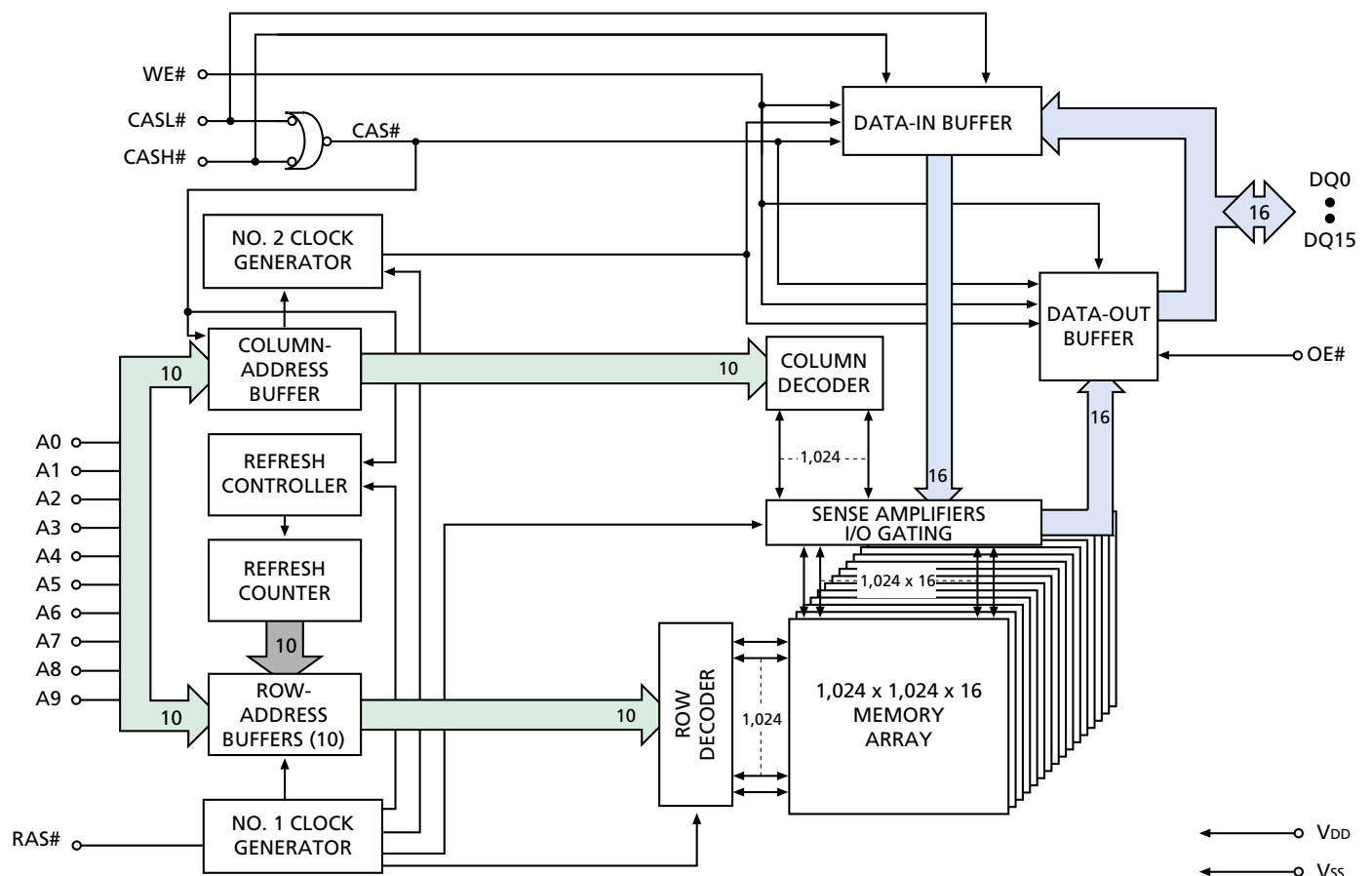
The CASL# and CASH# inputs internally generate a CAS# signal that functions identically to a single CAS# input on other DRAMs. The key difference is that each CAS# input (CASL# and CASH#) controls its corre-

sponding DQ tristate logic (in conjunction with OE# and WE#). CASL# controls DQ0-DQ7 and CASH# controls DQ8-DQ15. The two CAS# controls give the 1 Meg x 16 DRAM BYTE WRITE cycle capabilities.

A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS, whichever occurs last. Taking WE# LOW will initiate a WRITE cycle, selecting DQ0-DQ15. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle. If WE# goes LOW after CAS# goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS# and OE# remain LOW (regardless of WE# or RAS#). This late WE# pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE# and WE#.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION (continued)

The MT4LC1M16C3 must be refreshed periodically in order to retain stored data.

FAST PAGE MODE ACCESS

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power

and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS# ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS# addresses (A0-A9) are executed at least every 16ms (128ms on the "S" version), regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITES and BYTE READS are determined by the use of CASL# and CASH#. Enabling CASL# will select a lower byte access (DQ0-DQ7), while enabling CASH# will select an upper byte access (DQ8-DQ15). Enabling both CASL# and CASH# selects a WORD WRITE cycle.

The 1 Meg x 16 DRAM may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the CAS# inputs. Figure 1 illustrates the BYTE WRITE and WORD WRITE cycles. Figure 2 illustrates BYTE READ and WORD READ cycles.

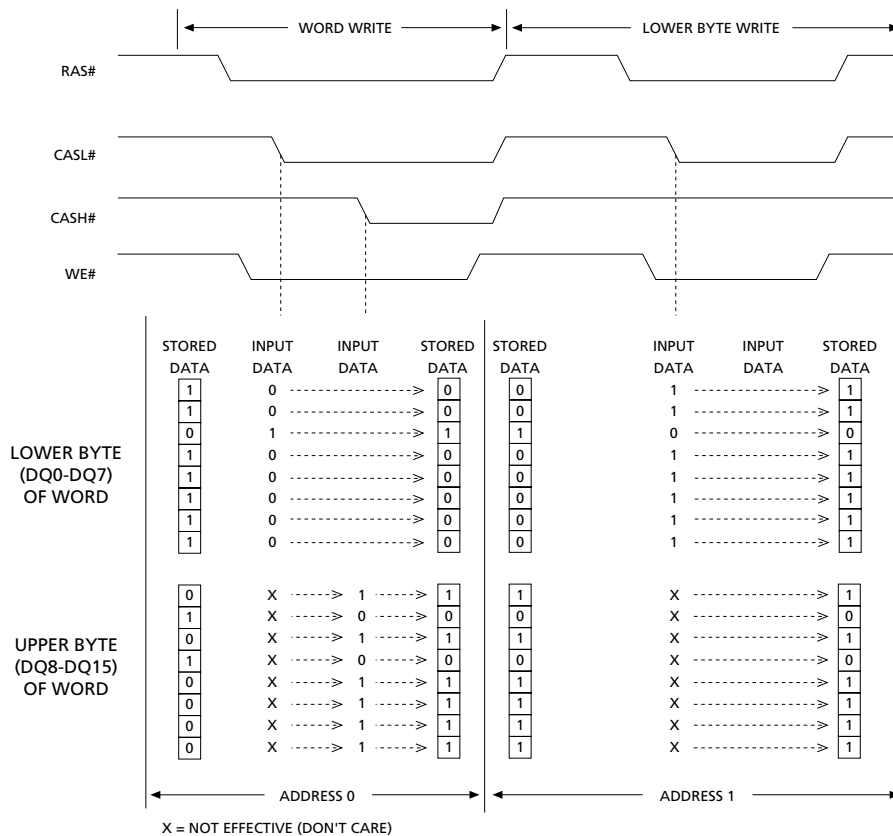


Figure 1
WORD and BYTE WRITE Example

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A CAS# precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte are not allowed during the same cycle. However, an EARLY WRITE on one byte and a LATE WRITE on the other byte, after a CAS# precharge has been satisfied, are permissible.

DRAM REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS# addresses are executed within $t_{REF}^{(MAX)}$, regardless of sequence. The CBR and EXTENDED and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS# addressing.

An optional self refresh mode is available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified t_{RASS} . The "S" option allows the user

the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, or 125 μ s per row, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of t_{RPS} . This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst CBR refresh sequence, all 1,024 rows must be refreshed using a minimum t_{RC} refresh rate prior to resuming normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

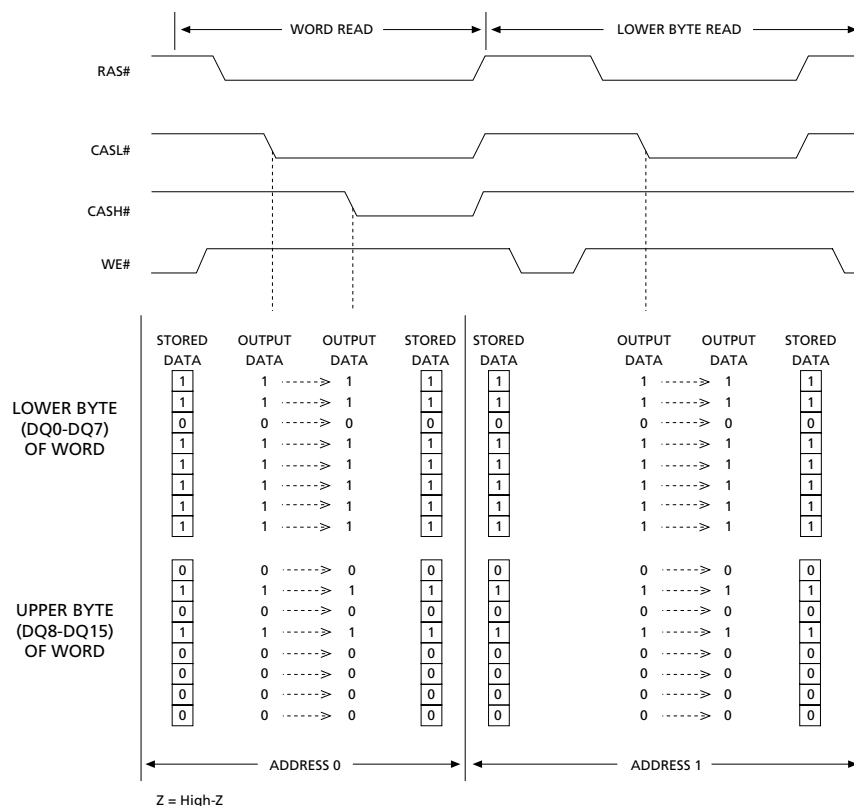


Figure 2
WORD and BYTE READ Example

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to V_{SS}
 3.3V -1V to +4.6V
 5V -1V TO +7V

Voltage on NC, Inputs or I/O Pins Relative to V_{SS}
 3.3V -1V to +5.5V
 5V -1V TO +7V

Operating Temperature
 T_A (commercial) 0°C to +70°C
 T_A (extended "ET") -20°C to +80°C

Storage Temperature (plastic) -55°C to +150°C

Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6; notes can be found on page 9); V_{CC} (MIN) ≤ V_{CC} ≤ V_{CC} (MAX)

PARAMETER/CONDITION	SYMBOL	3.3V		5V		UNITS	NOTES
		MIN	MAX	MIN	MAX		
SUPPLY VOLTAGE	V _{CC}	3	3.6	4.5	5.5	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V _{IH}	2	5.5	2.4	V _{CC} + 1	V	
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V _{IL}	-1.0	0.8	-0.5	0.8	V	
INPUT LEAKAGE CURRENT: Any input at V _{IN} (0V ≤ V _{IN} ≤ V _{CC} + 0.3V); All other pins not under test = 0V	I _I	-2	2	-2	2	μA	
OUTPUT HIGH VOLTAGE: I _{OUT} = -2mA	V _{OH}	2.4	-	2.4	-	V	
OUTPUT LOW VOLTAGE: I _{OUT} = 2mA	V _{OL}	-	0.4	-	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V _{OUT} [0V ≤ V _{OUT} ≤ V _{CC} (MAX)]; DQ is disabled and in High-Z state	I _{OZ}	-5	5	-5	5	μA	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

 (Notes: 1, 2, 3, 5, 6; notes can be found on page 9); $V_{CC} (MIN) \leq V_{CC} \leq V_{CC} (MAX)$

PARAMETER/CONDITION	SYMBOL	SPEED	3.3V	5V	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V _{IH})	I _{CC1}	ALL	1	2	mA	
STANDBY CURRENT: CMOS (non-"S" version only) (RAS# = CAS# = other inputs = V _{CC} - 0.2V)	I _{CC2}	ALL	500	500	μA	
STANDBY CURRENT: CMOS ("S" version only) (RAS# = CAS# = other inputs = V _{CC} - 0.2V)	I _{CC2}	ALL	150	150	μA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: t _{RC} = t _{RC} [MIN])	I _{CC3}	-5 -6	180 170	190 180	mA	23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V _{IL} , CAS#, address cycling: t _{PC} = t _{PC} [MIN])	I _{CC4}	-5 -6	110 90	120 110	mA	23
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V _{IH} : t _{RC} = t _{RC} [MIN])	I _{CC5}	-5 -6	180 170	190 180	mA	
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: t _{RC} = t _{RC} [MIN])	I _{CC6}	-5 -6	180 170	180 180	mA	4, 7
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = t _{RAS} (MIN); WE# = V _{CC} - 0.2V; A0-A11, OE# and D _{IN} = V _{CC} - 0.2V or 0.2V (D _{IN} may be left open)	I _{CC7}	ALL	300	300	μA	4, 7
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# t _{RASS} (MIN) and CAS# held LOW; WE# = V _{CC} - 0.2V; A0-A11, OE# and D _{IN} = V _{CC} - 0.2V or 0.2V (D _{IN} may be left open)	I _{CC8}	ALL	300	300	μA	4, 7

CAPACITANCE

(Note: 2; notes can be found on page 9);

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance: Addresses	C _{I1}	5	pF
Input Capacitance: RAS#, CASL#, CASH#, WE#, OE#	C _{I2}	7	pF
Input/Output Capacitance: DQ	C _{I0}	7	pF

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12; notes can be found on page 9); $V_{CC} (MIN) \leq V_{CC} \leq V_{CC} (MAX)$

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	t_{AA}		25		30	ns	
Column-address hold time (referenced to RAS#)	t_{AR}	38		45		ns	
Column-address setup time	t_{ASC}	0		0		ns	27
Row-address setup time	t_{ASR}	0		0		ns	
Column address to WE# delay time	t_{AWD}	42		49		ns	18
Access time from CAS	t_{CAC}		15		15	ns	29
Column-address hold time	t_{CAH}	8		10		ns	27
CAS# pulse width	t_{CAS}	8	10,000	10	10,000	ns	32, 35
CAS# LOW to "Don't Care" during Self Refresh	t_{CHD}	15		15		ns	
CAS# hold time (CBR Refresh)	t_{CHR}	8		10		ns	4, 28
Last CAS# going LOW to first CAS# to return HIGH	t_{CLCH}	10		10		ns	30
CAS# to output in Low-Z	t_{CLZ}	0		0		ns	26, 29
CAS# precharge time	t_{CP}	8		5		ns	30
Access time from CAS# precharge	t_{CPA}		28		35	ns	28
CAS# to RAS# precharge time	t_{CRP}	5		5		ns	28
CAS# hold time	t_{CSH}	38		45		ns	28
CAS# setup time (CBR Refresh)	t_{CSR}	5		5		ns	4, 27
CAS# to WE# delay time	t_{CWD}	28		35		ns	18, 27
WRITE command to CAS# lead time	t_{CWL}	8		10		ns	23, 29
Data-in hold time	t_{DH}	8		10		ns	19, 29
Data-in setup time	t_{DS}	0		0		ns	19, 29
Output disable	t_{OD}	0	12	0	15	ns	17, 26, 29
Output enable	t_{OE}		12		15	ns	22
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t_{OEH}	8		10		ns	20
Output buffer turn-off delay	t_{OFF}	0	12	0	15	ns	11, 17, 23
OE# setup prior to RAS# during HIDDEN Refresh cycle	t_{ORD}	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	20		25		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	47		56		ns	31
Access time from RAS#	t_{RAC}		50		60	ns	
RAS# to column-address delay time	t_{RAD}	9		12		ns	20
Row-address hold time	t_{RAH}	9		10		ns	
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	t_{RASP}	50	125,000	60	125,000	ns	
RAS# pulse width (Self Refresh)	t_{RASS}	100		100		μ s	
Random READ or WRITE cycle time	t_{RC}	84		104		ns	
RAS# to CAS# delay time	t_{RCD}	11		14		ns	14, 27
READ command hold time (referenced to CAS)	t_{RCH}	0		0		ns	16, 28
READ command setup time	t_{RCS}	0		0		ns	27
Refresh period (1,024 cycles)	t_{REF}		16		16	ms	
Refresh period (1,024 cycles) "S" version	t_{REF}		128		128	ms	
RAS# precharge time	t_{RP}	30		40		ns	
RAS# to CAS# precharge time	t_{RPC}	5		5		ns	
RAS# precharge time (Self Refresh)	t_{RPS}	90		105		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	16
RAS# hold time	t_{RSH}	13		15		ns	36
READ-WRITE cycle time	t_{RWC}	116		140		ns	

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12; notes can be found on page 9); $V_{CC} (MIN) \leq V_{CC} \leq V_{CC} (MAX)$

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
RAS# to WE# delay time	t_{RWD}	67		79		ns	18
WRITE command to RAS# lead time	t_{RWL}	13		15		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	
WRITE command hold time	t_{WCH}	8		10		ns	36
WRITE command hold time (referenced to RAS#)	t_{WCR}	38		45		ns	
WE# command setup time	t_{WCS}	0		0		ns	18, 27
WRITE command pulse width	t_{WP}	5		5		ns	
WE# hold time (CBR Refresh)	t_{WRH}	8		10		ns	
WE# setup time (CBR Refresh)	t_{WRP}	8		10		ns	

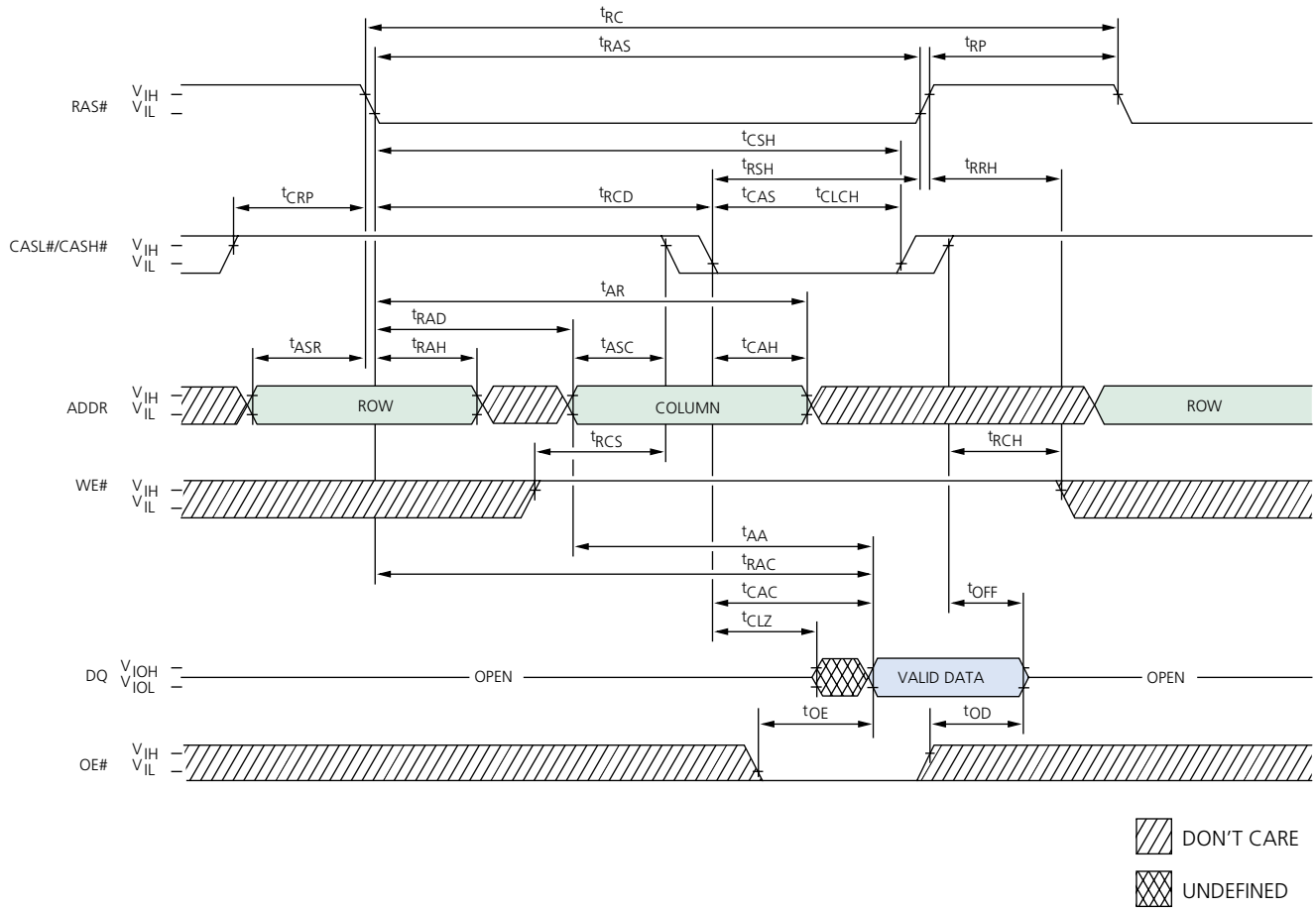
NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = +3.3V$ or $5.0V$; $f = 1$ MHz.
3. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}C \leq T_A \leq 70^{\circ}C$) for commercial and ($-20^{\circ}C \leq T_A \leq 80^{\circ}C$) for extended "ET" is ensured.
6. An initial pause of $100\mu s$ is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5ns$.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH} , data output is High-Z.
11. If CAS# = V_{IL} , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates, $100pF$ and $V_{OL} = 0.8V$ and $V_{OH} = 2V$.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS# must be pulsed HIGH for t_{CP} .
14. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} limit, t_{AA} and t_{CAC} must always be met.
15. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} , and t_{CAC} must always be met.
16. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
17. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL} .
18. t_{WCS} , t_{RWD} , t_{AWD} , and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data out-put will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (MIN), $t_{AWD} \geq t_{AWD}$ (MIN) and $t_{CWD} \geq t_{CWD}$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS# or OE# goes back to V_{IH}) is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. During a READ cycle, if OE# is LOW then taken HIGH before CAS# goes HIGH, Q goes open. If OE# is tied permanently LOW, LATE WRITE and READ-MODIFY-WRITE operations are not permissible and should not be attempted.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
22. All other inputs at $0.2V$ or $V_{CC} - 0.2V$.
23. Column address changed once each cycle.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OE} met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after t_{OE} is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
25. The DQs open during READ cycles once t_{OD} or t_{OFF} occur.
26. The $3ns$ minimum is a parameter guaranteed by design.
27. The first CASx edge to transition LOW.
28. The last CASx edge to transition HIGH.
29. Output parameter (DQx) is referenced to corresponding CAS# input; DQ0-DQ7 by CASL# and DQ8-DQ15 by CASH#.
30. Last falling CASx edge to first rising CASx edge.
31. Last rising CASx edge to next cycle's last rising CASx edge.

NOTES (continued)

- 32. Last rising CASx edge to first falling CASx edge.
- 33. First DQs controlled by the first CASx to go LOW.
- 34. Last DQs controlled by the last CASx to go HIGH.
- 35. Each CASx must meet minimum pulse width.
- 36. Last CASx to go LOW.
- 37. All DQs controlled, regardless CASL# and CASH#.
- 38. If OE# is tied permanently LOW, LATE WRITE, or READ-MODIFY-WRITE operations are not permissible and should not be attempted.

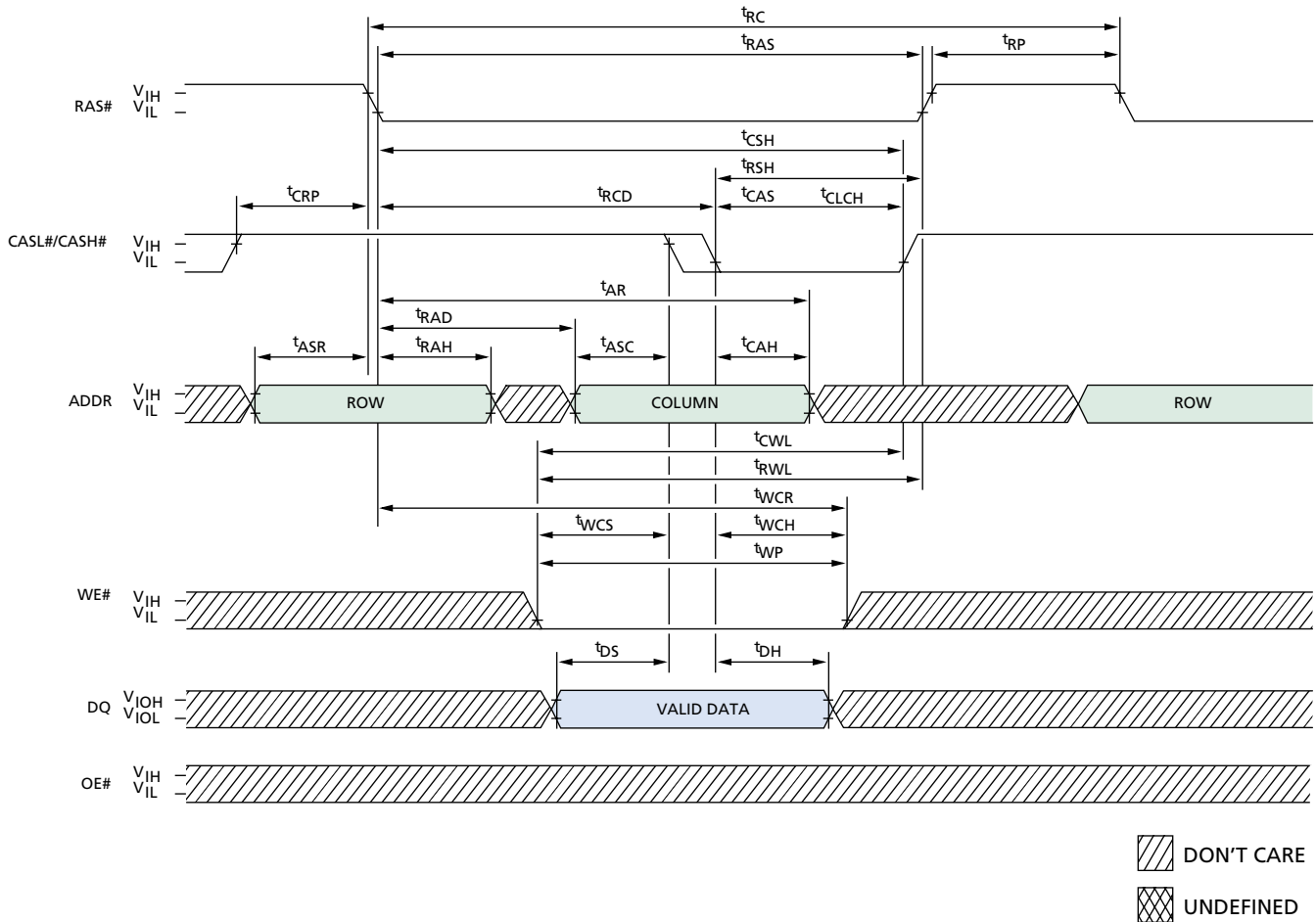
READ CYCLE



TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		15		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLCH}	10		10		ns
t_{CLZ}	0		0		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns

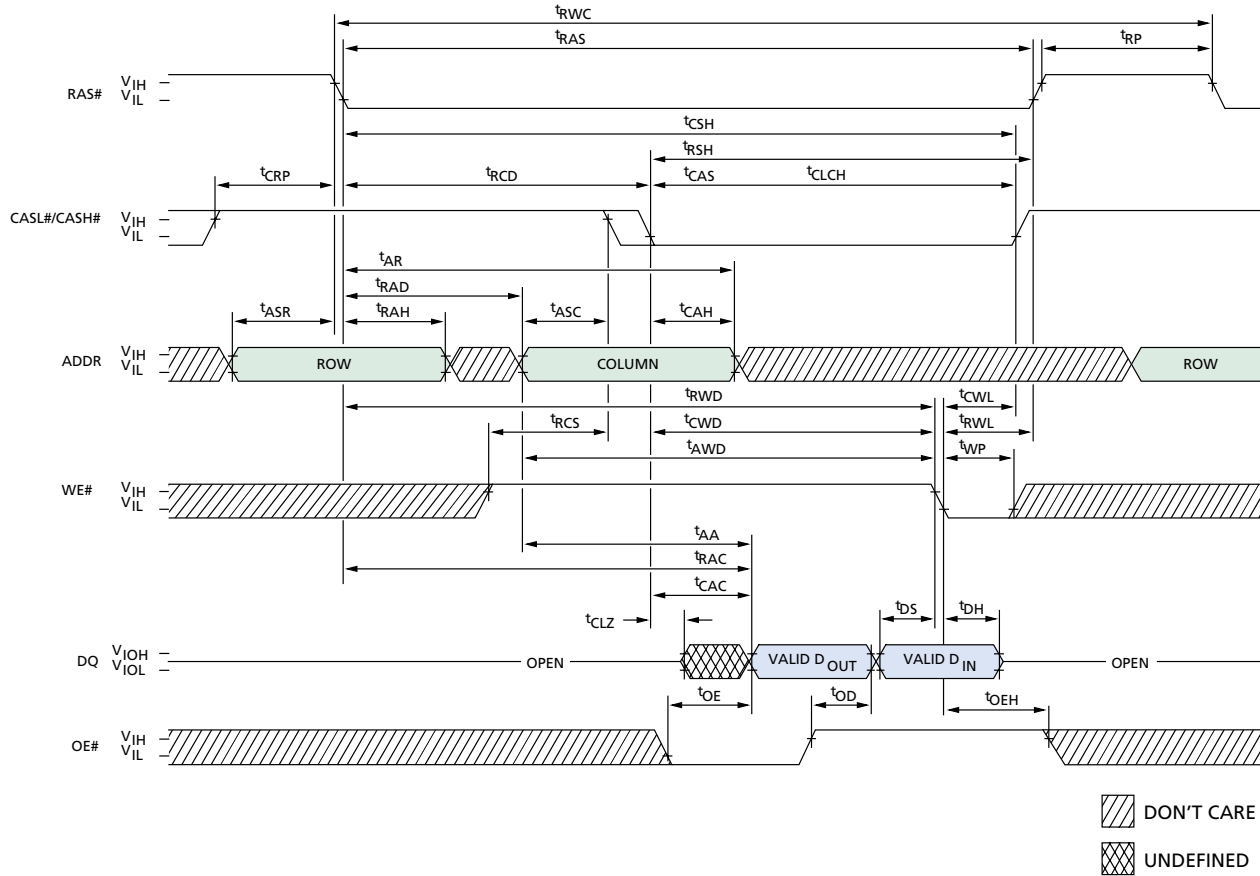
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OFF}	0	12	0	15	ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC}	84		104		ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RRH}	0		0		ns
t_{RSH}	13		15		ns

EARLY WRITE CYCLE

TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLCH}	10		10		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns
t_{RAD}	9		12		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC}	84		104		ns
t_{RCD}	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWL}	13		15		ns
t_{WCH}	8		10		ns
t_{WCR}	38		45		ns
t_{WCS}	0		0		ns
t_{WP}	5		5		ns

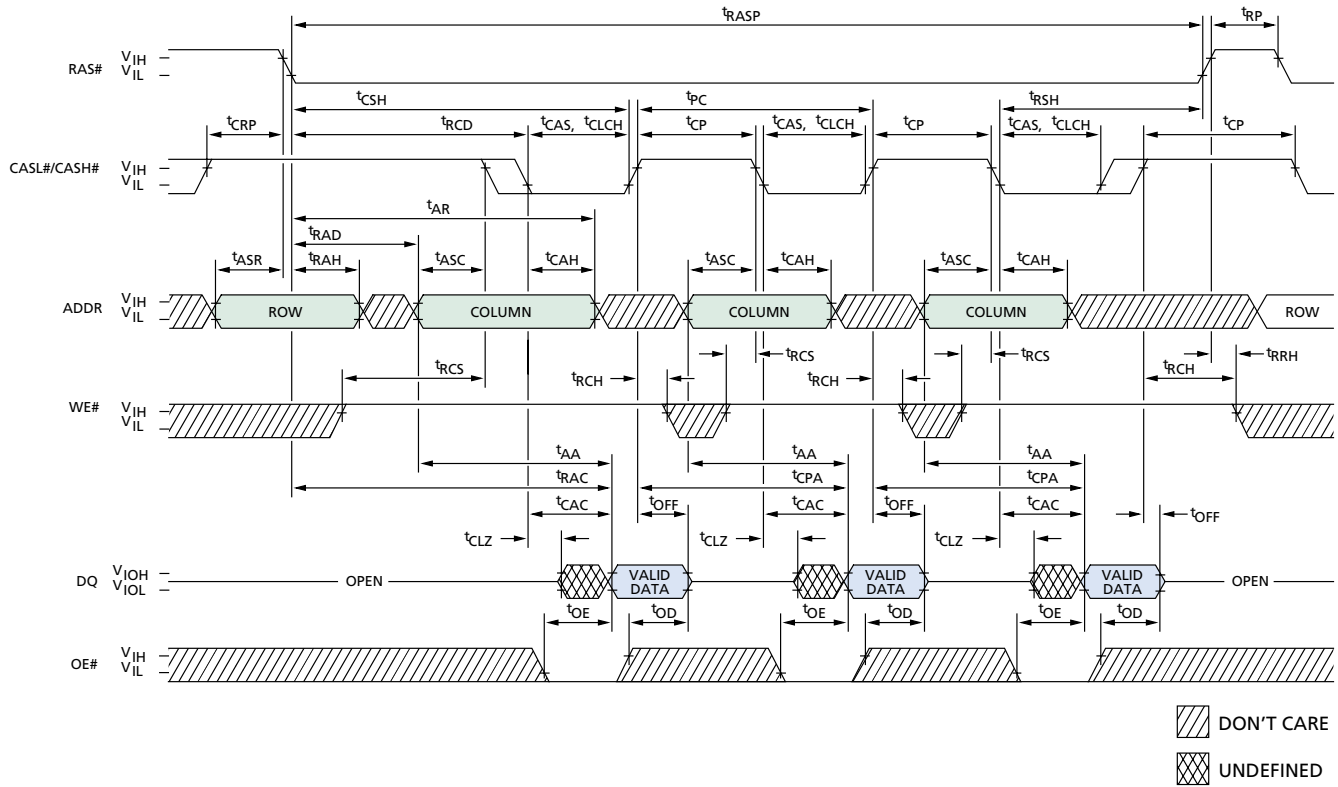
READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)



TIMING PARAMETERS

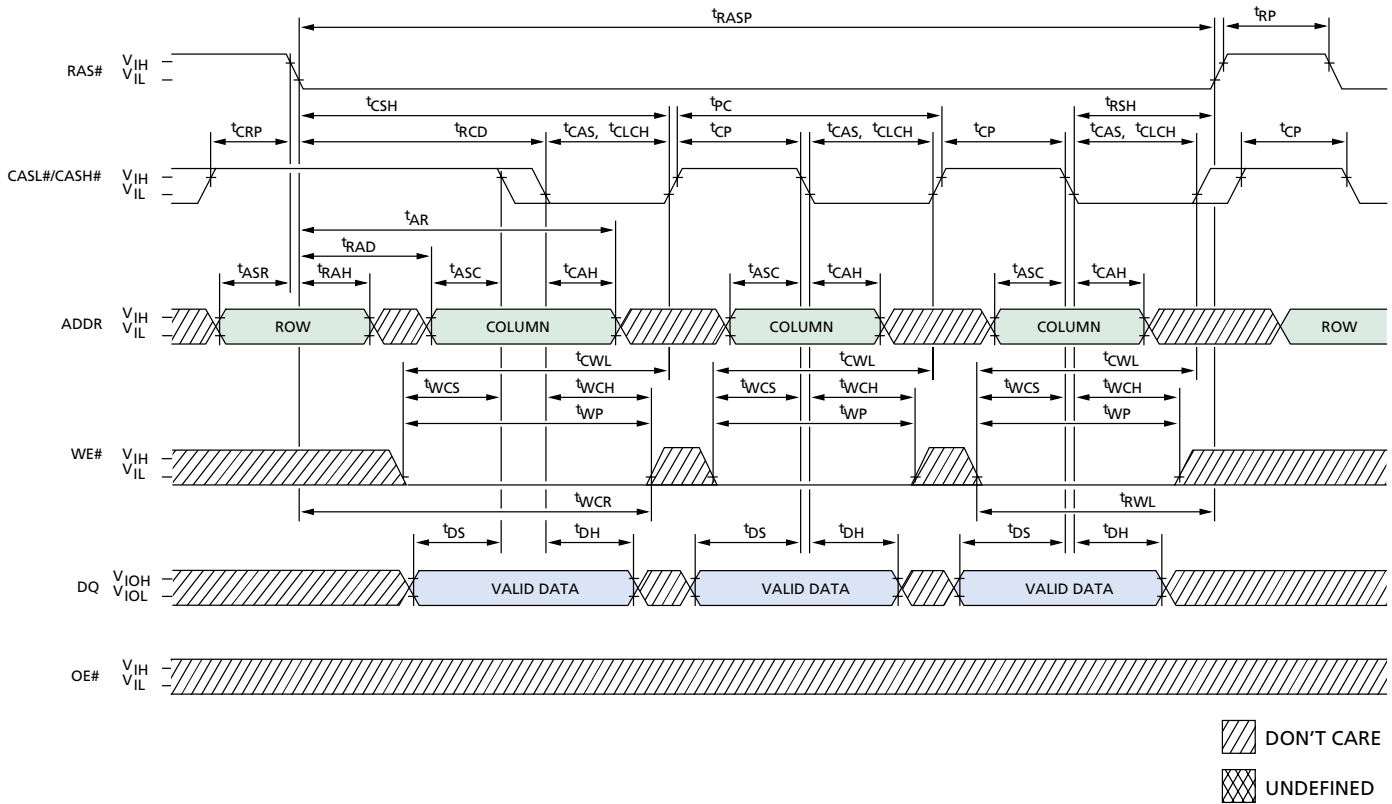
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		15		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	10		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC	116		140		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

FAST-PAGE-MODE READ CYCLE

TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		15		15	ns
t _{CAH}	8		10		ns
t _{CAS}	8	10,000	10	10,000	ns
t _{CLCH}	10		10		ns
t _{CLZ}	0		0		ns
t _{CP}	8		5		ns
t _{CPA}		28		35	ns
t _{CRP}	5		5		ns
t _{CSH}	38		45		ns
t _{OD}	0	12	0	15	ns

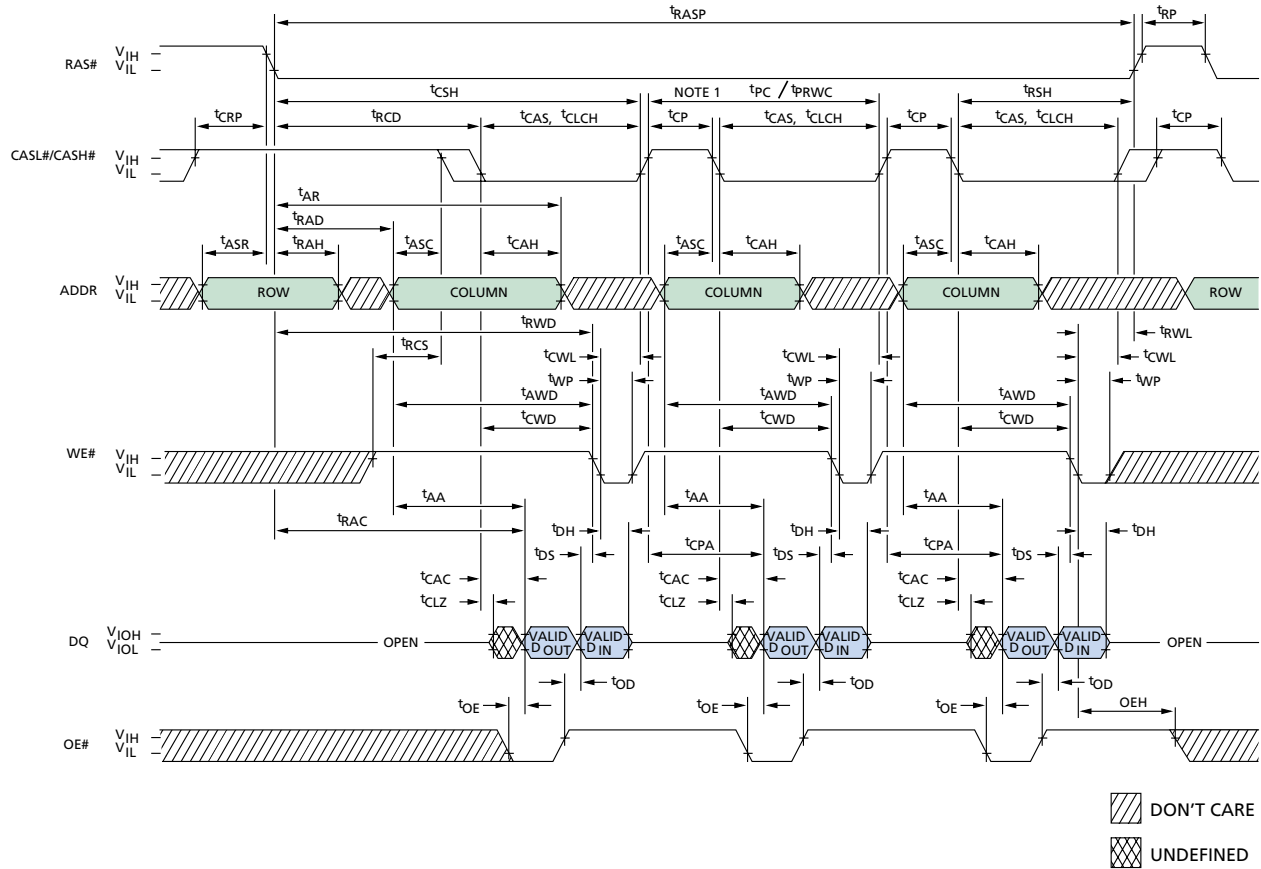
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OE}		12		15	ns
t _{OFF}	0	12	0	15	ns
t _{PC}	20		25		ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD}	11		14		ns
t _{RCH}	0		0		ns
t _{RCS}	0		0		ns
t _{RP}	30		40		ns
t _{RRH}	0		0		ns
t _{RSH}	13		15		ns

FAST-PAGE-MODE EARLY WRITE CYCLE

TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLCH}	10		10		ns
t_{CP}	8		5		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{PC}	20		25		ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RASP}	50	125,000	60	125,000	ns
t_{RCD}	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWL}	13		15		ns
t_{WCH}	8		10		ns
t_{WCR}	38		45		ns
t_{WCS}	0		0		ns
t_{WP}	5		5		ns

FAST-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)



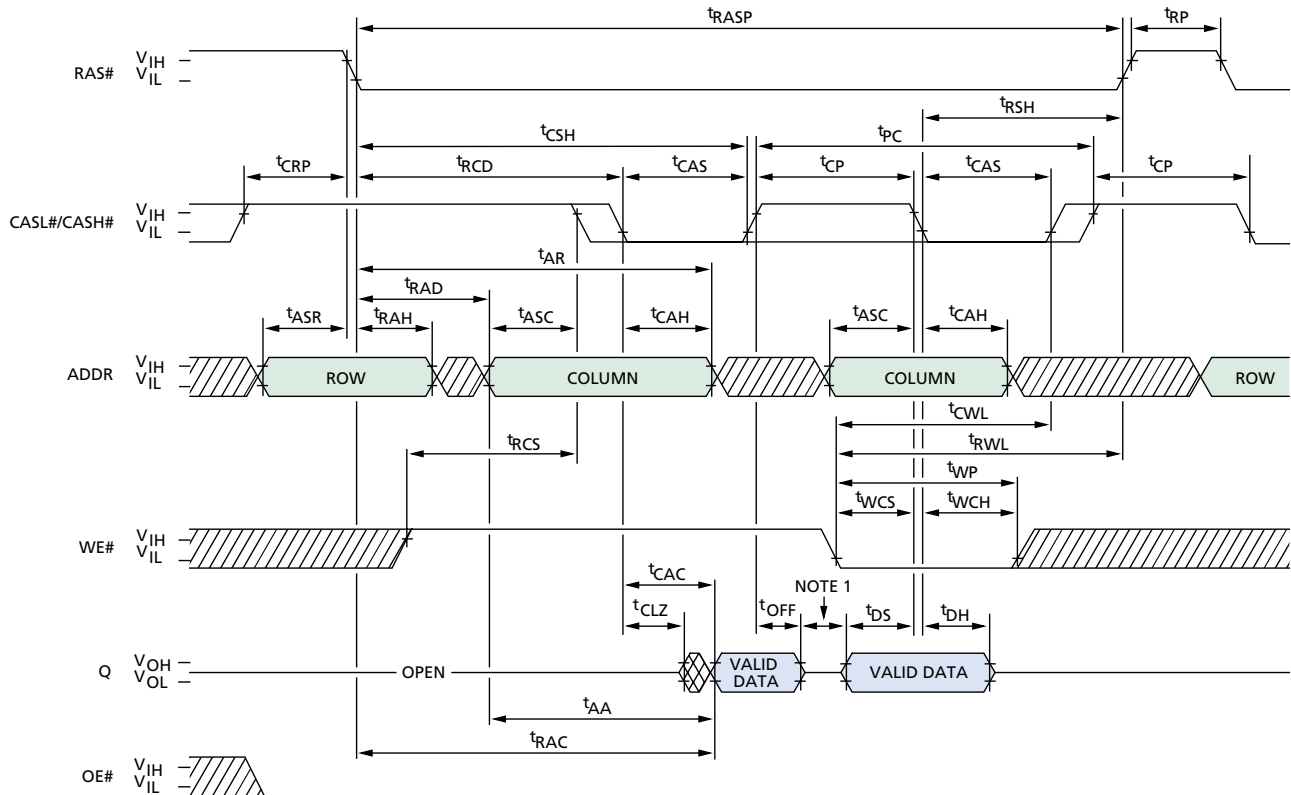
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{AWD}	42		49		ns
t _{CAC}		15		15	ns
t _{CAH}	8		10		ns
t _{CAS}	8	10,000	10	10,000	ns
t _{CLCH}	10		10		ns
t _{CLZ}	0		0		ns
t _{CP}	8		5		ns
t _{CPA}		28		35	ns
t _{CRP}	5		5		ns
t _{CSH}	38		45		ns
t _{CWD}	28		35		ns
t _{CWL}	8		10		ns
t _{DH}	8		10		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{DS}	0		0		ns
t _{OD}	0	12	0	15	ns
t _{OE}		12		15	ns
t _{OE_H}	8		10		ns
t _{PC}	20		25		ns
t _{PRWC}	47		56		ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD}	11		14		ns
t _{RCS}	0		0		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns
t _{RWD}	67		79		ns
t _{RWL}	13		15		ns
t _{WP}	5		5		ns

NOTE: 1. t_{PC} is for LATE WRITE only.

FAST-PAGE-MODE READ EARLY WRITE CYCLE (Pseudo READ-MODIFY-WRITE)



DON'T CARE
 UNDEFINED

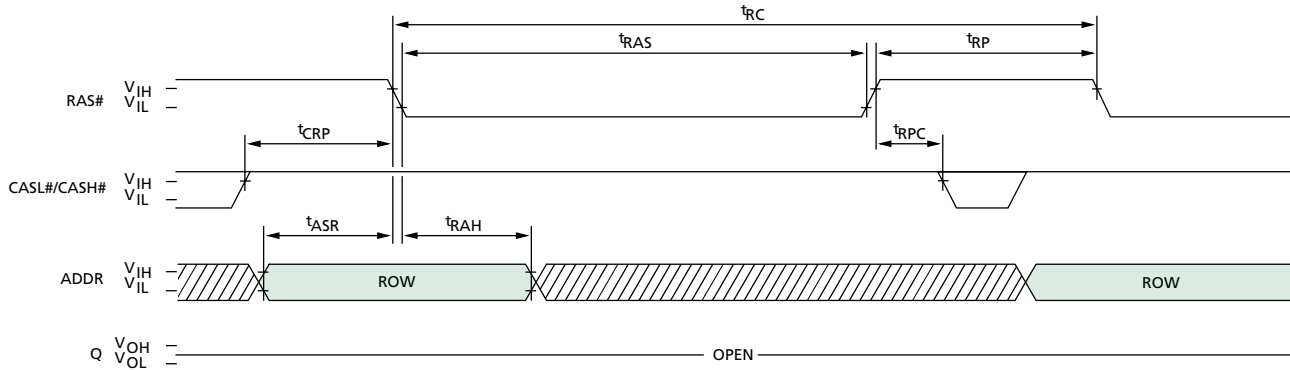
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		15		15	ns
t _{CAH}	8		10		ns
t _{CAS}	8	10,000	10	10,000	ns
t _{CLZ}	0		0		ns
t _{CP}	8		5		ns
t _{CRP}	5		5		ns
t _{CSH}	38		45		ns
t _{CWL}	8		10		ns
t _{DH}	8		10		ns
t _{DS}	0		0		ns

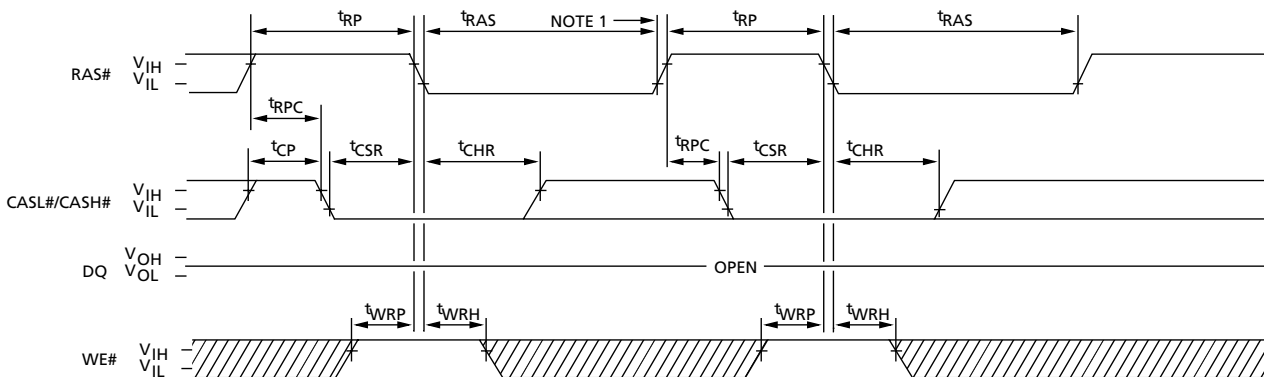
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OFF}	0	12	0	15	ns
t _{PC}	20		25		ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD}	11		14		ns
t _{RCS}	0		0		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns
t _{RWL}	13		15		ns
t _{WCH}	8		10		ns
t _{WCS}	0		0		ns
t _{WP}	5		5		ns

NOTE: 1. t_{PC} is for LATE WRITE only.

RAS#-ONLY REFRESH CYCLE (OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE (Addresses and OE# = DON'T CARE)



DON'T CARE
 UNDEFINED

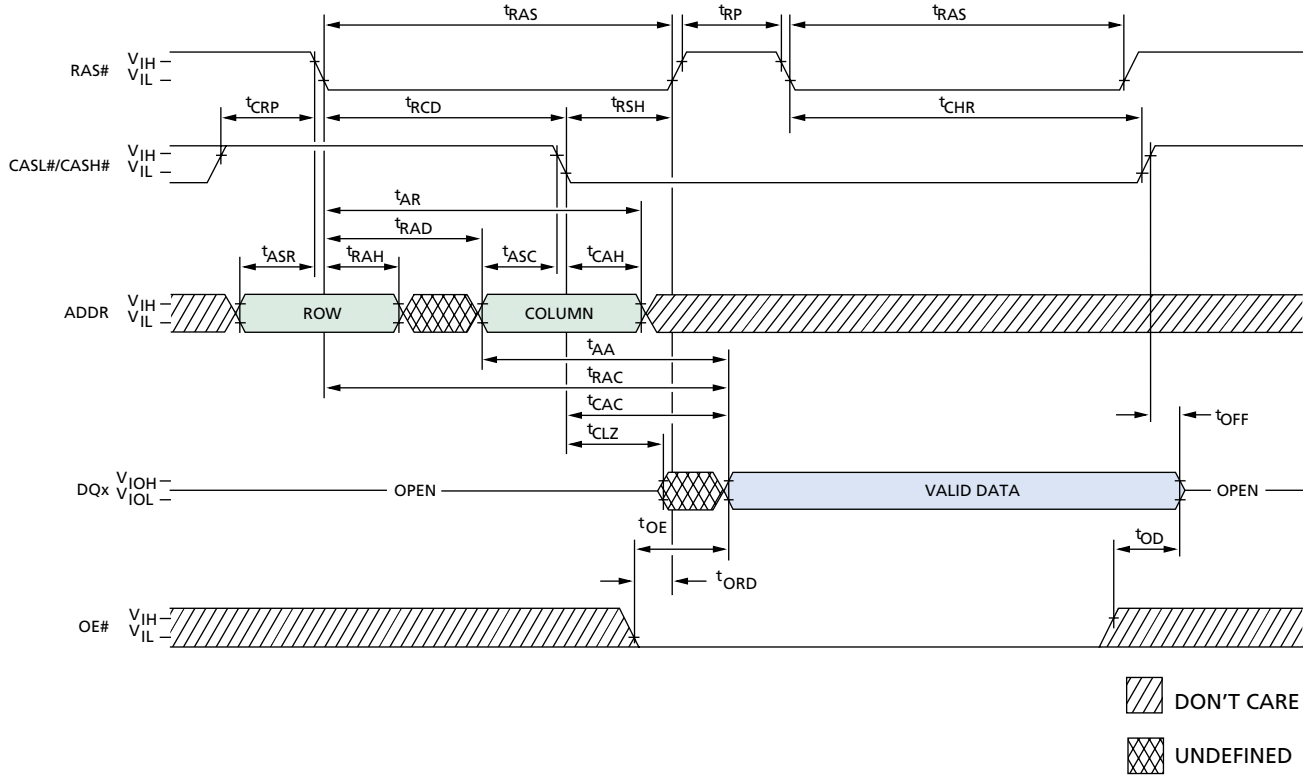
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{ASR}	0		0		ns
t_{CHR}	8		10		ns
t_{CP}	8		5		ns
t_{CRP}	5		5		ns
t_{CSR}	5		5		ns
t_{RAH}	9		10		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RAS}	50		60	10,000	ns
t_{RC}	84		104		ns
t_{RP}	30		40		ns
t_{RPC}	5		5		ns
t_{WRH}	8		10		ns
t_{WRP}	8		10		ns

NOTE: 1. End of CBR REFRESH cycle.

HIDDEN REFRESH CYCLE¹ (WE# = HIGH; OE# = LOW)



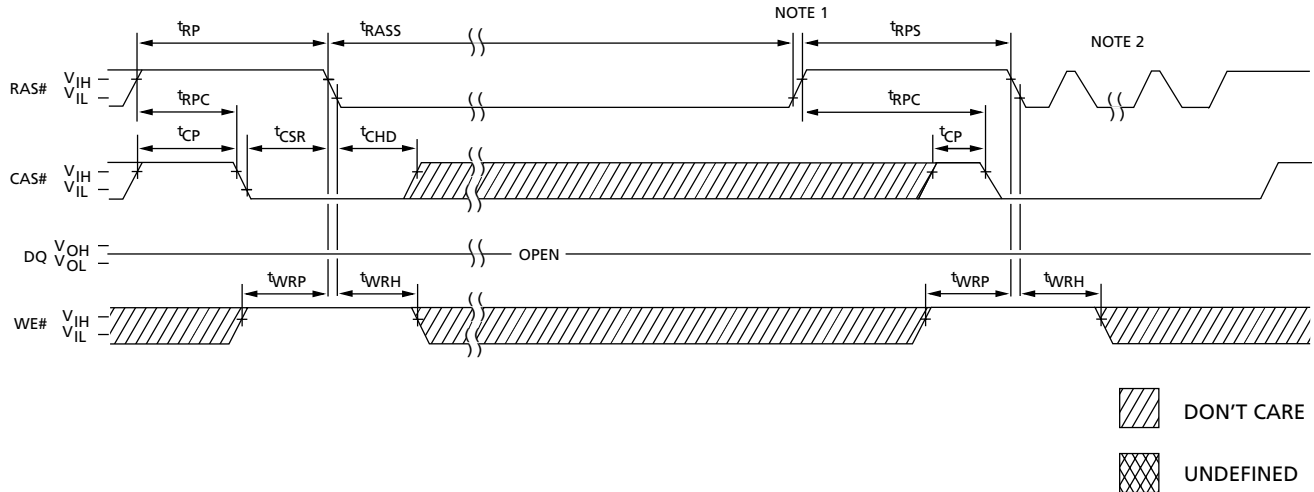
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		15		15	ns
t _{CAH}	8		10		ns
t _{CHR}	8		10		ns
t _{CLZ}	0		0		ns
t _{CRP}	5		5		ns
t _{OD}	0	12	0	15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OE}		12		15	ns
t _{OFF}	0	12	0	15	ns
t _{ORD}	0		0		ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RAS}	50	10,000	60	10,000	ns
t _{RCD}	11		14		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns

NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.

SELF REFRESH CYCLE (Addresses and OE# = DON'T CARE)

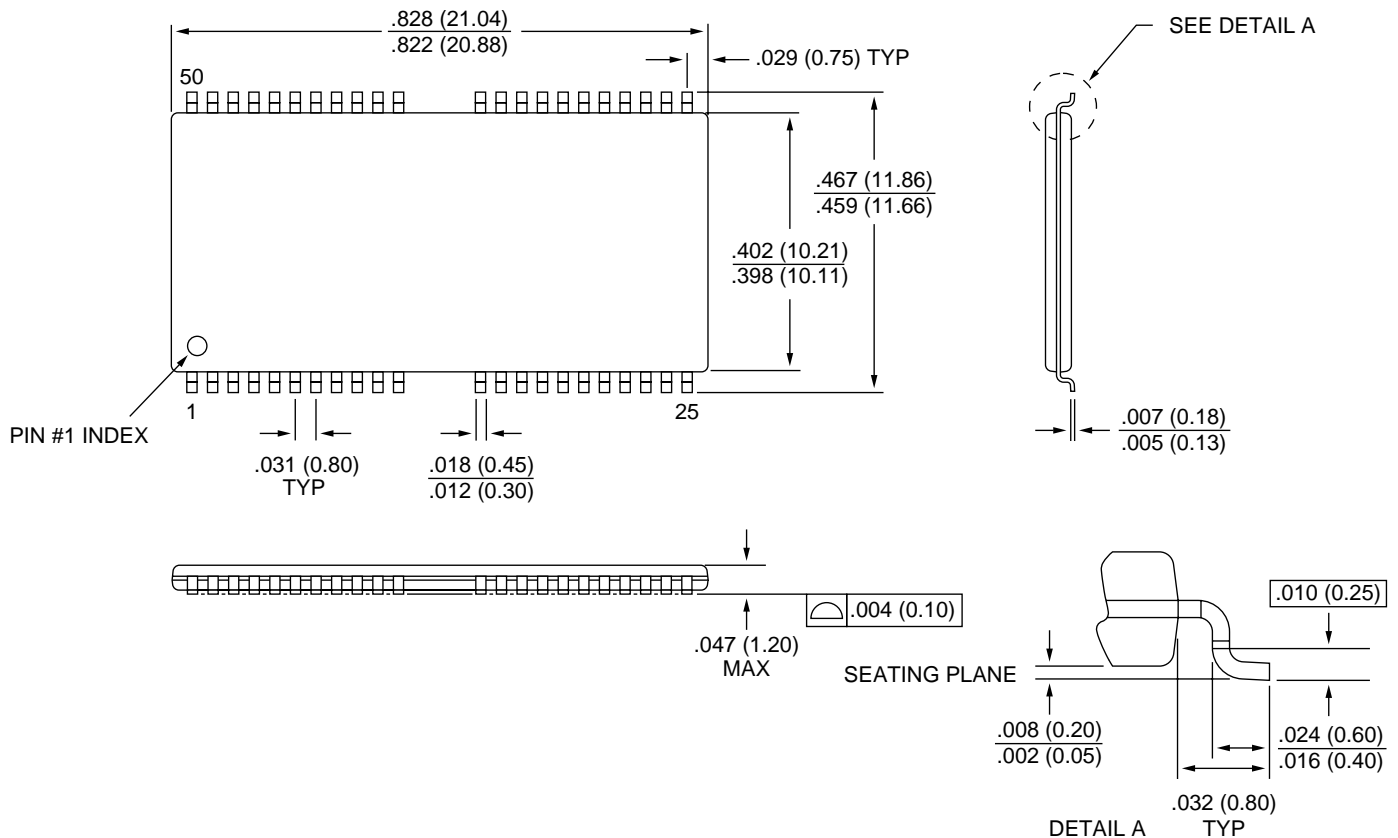


TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{CHD}	15		15		ns
t_{CLCH}	10		10		ns
t_{CP}	8		5		ns
t_{CSR}	5		5		ns
t_{RASS}	100		100		μ s

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RP}	30		40		ns
t_{RPC}	5		5		ns
t_{RPS}	90		105		ns
t_{WRH}	8		10		ns
t_{WRP}	8		10		ns

- NOTE:** 1. Once t_{RASS} (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once t_{RPS} is satisfied, a complete burst of all rows should be executed if RAS#-only or burst CBR refresh is used.

44/50-PIN PLASTIC TSOP (400 mil)


- NOTE:**
- All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 - Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.



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