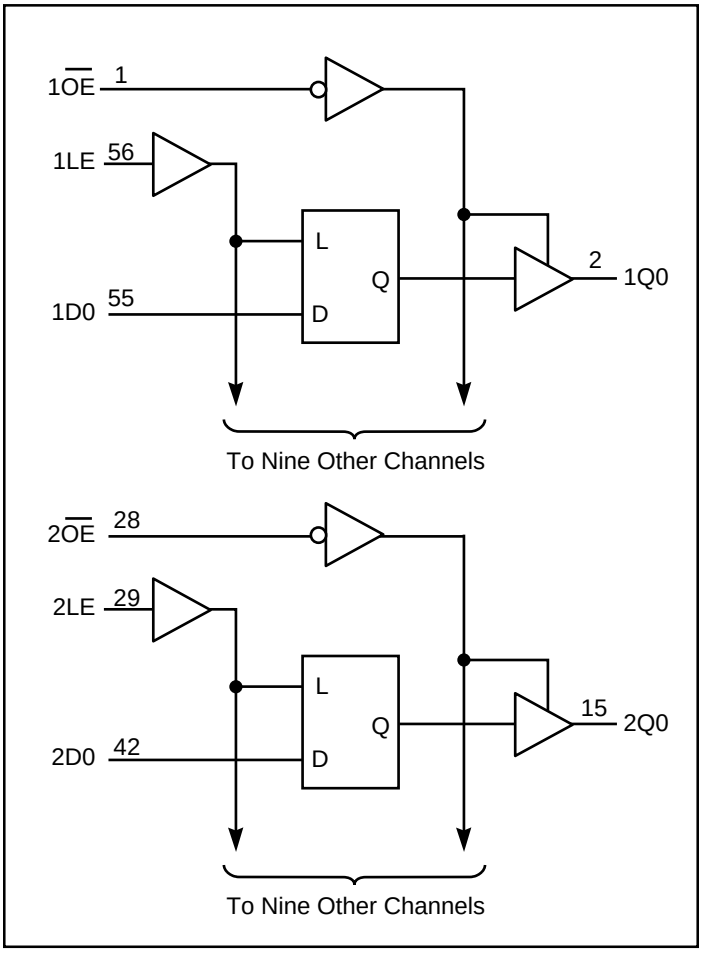
PI74ALVTC16841

2.5V 20-Bit Bus Interface D-Type Latch with 3-State Outputs

Product Features

- PI74ALVTC16841 is designed for low voltage operation, V_{DD} = 1.65V to 3.6V
- Supports Live Insertion
- 3.6V I/O Tolerant Inputs and Outputs
- Bus Hold
- High Drive, –32/64mA @ 3.3V
- Uses patented noise reduction circuitry
- Power-off high impedance inputs and outputs
- Industrial operation at –40°C to +85°C
- Packages available:
  - 56-pin 240-mil wide plastic TSSOP (A56)
  - 56-pin 173-mil wide plastic TVSOP (K56)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74ALVTC series of logic circuits are produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

The PI74ALVTC16841 features 3-State outputs designed specifically for driving highly capacitive or relatively low-impedence loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The device can be used as two 10-bit latches, or one 20-bit latch. The 20 latches are transparent D-type latches. The device has non-inverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follows the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedence state. In the high-impedence state, the outputs neither load nor drive the bus lines significantly.

The output enable ($\overline{OE}$) input does not affect the internal operation of the latches. Old data can be retained or new data or new data can be entered while the outputs are in the high-impedence state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{DD} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The family offers both I/O Tolerant, which allows it to operate in mixed 1.65/3.6V systems, and "Bus Hold," which retains the data input's last state preventing "floating" inputs and eliminating the need for pullup/down resistors.

Product Pin Description

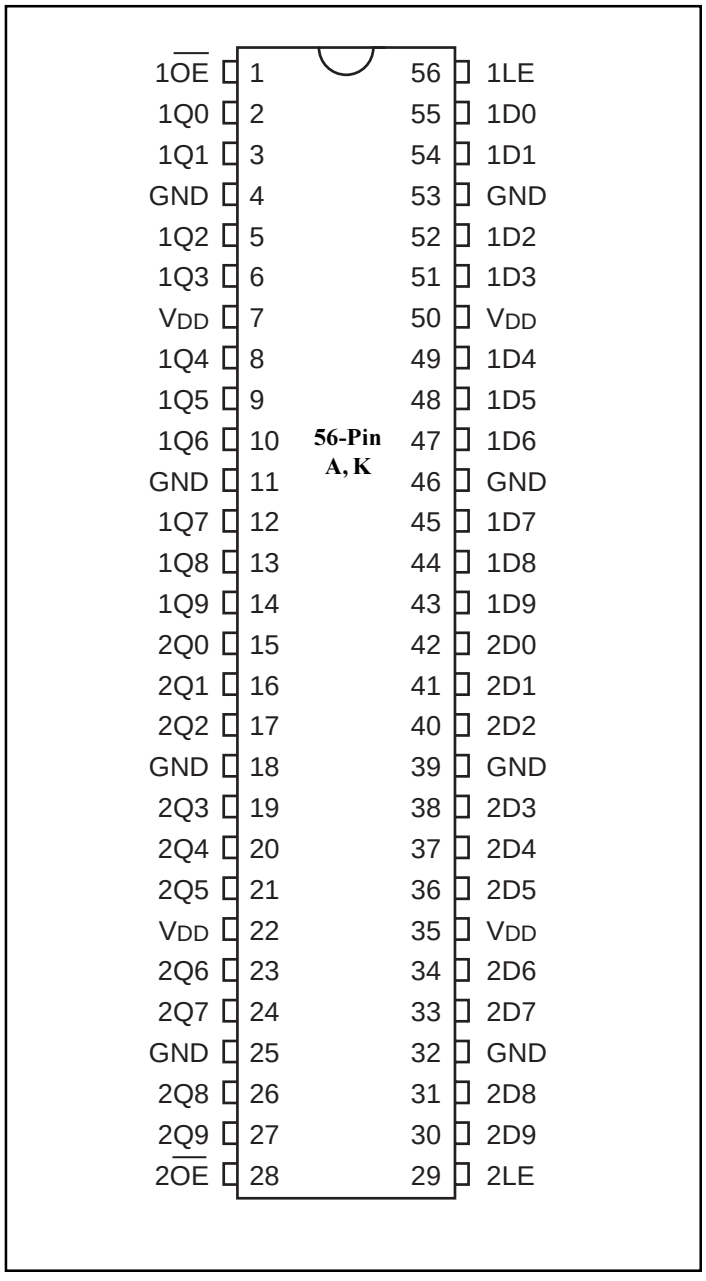
Pin Name	Description
n$\overline{OE}$	Output Enable Inputs (Active LOW)
nLE	Latch Enable Inputs (Active HIGH)
nDx	Data Inputs
nQx	3-State Outputs
GND	Ground
V_{DD}	Power

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Notes:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High-Impedance "OFF" state

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, V_{DD} ..... –0.5V to 4.6V
Input Voltage Range, V_I ..... -0.5V to 4.6V
Output Voltage Range, V_O (3-Stated) ..... -0.5V to 4.6V
Output Voltage Range, V_O[1] (Active) ..... –0.5V to V_{DD} +0.5V
DC Input Diode Current (I_{IK}) V_I < 0V ..... -50mA
DC Output Diode Current (I_{OK})
V_O < 0V ..... -50mA
V_O > V_{DD} ..... ±50mA
DC Output Source/Sink Current (I_{OH}/I_{OL}) ..... -64/128mA
DC V_{DD} or GND Current per Supply Pin (I_{CC} or GND) ..... ±100mA
Storage Temperature Range, T_{stg} ..... –65°C to 150°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions[2]

			Min.	Max.	Units
V_{DD}	Supply voltage	Operating	1.65	3.6	V
		Data Retention Only	1.2	3.6	
V_{IH}	High-level input voltage	V_{DD} = 2.7V to 3.6V	2.0		
V_{IL}	Low-level input voltage	V_{DD} = 2.7V to 3.6V		0.8	
V_I	Input voltage		–0.3	3.6	
V_O	Output voltage	Active State	0	V_{DD}	
		Off State	0	3.6	
	Output current in I_{OH}/I_{OL}	V_{DD} = 3.0V to 3.6V V_{DD} = 3.0V to 3.6V V_{DD} = 2.3V to 2.7V V_{DD} = 1.65V to 1.95V		–32/64 ±24 ±18 ±6	mA
$\Delta t/\Delta v$	Input transistion rise or fall rate[3]		0	10	ns/V
T_A	Operating free-air temperature		–40	85	C

Notes:
1. Absolute maximum of I_O must be observed.
2. Unused control inputs must be held HIGH or LOW to prevent them from floating.
3 As measured between 0.8V and 2.0V, V_{DD}=3.0V.

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted)

DC Characteristics ($2.7V < V_{DD} \leq 3.6V$)

	Parameter	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Diode	I_{IK} = –18mA	3.0			–1.2	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100µA	2.7 - 3.6	V_{DD} – 0.2			
		I_{OH} = –12mA	2.7	2.2			
		I_{OH} = –18mA	3.0	2.4			
		I_{OH} = –24mA		2.2			
		I_{OH} = –32mA		2.0			
V_{OL}	LOW Level Output Voltage	I_{OL} = 100µA	2.7 - 3.6			0.2	
		I_{OL} = 12mA	2.7			0.4	
		I_{OL} = 18mA	3.0			0.4	
		I_{OL} = 24mA				0.45	
		I_{OL} = 32mA				0.5	
		I_{OL} = 64mA				0.55	
I_I	Input Leakage Current	$V_I = V_{DD}$, or GND	3.6			±5.0	µA
I_{OZ}	3-State Output Leakage	V_O = 3.6V	2.7			±10	
I_{OFF}	Power-OFF Leakage Current	V_I or $V_O \leq$ 3.6V	0			10	
I_{HOLD}	Bus Hold Current A or B Outputs	V_I = 0.8V	3.0	75			
		V_I = 2.0V		–75			
		V_I = 0 to 3.6V	3.6			±500	
I_{DD}	Quiescent Supply Current	$V_I = V_{DD}$ or GND	2.7 - 3.6			50	
		$V_{DD} \leq (V_I, V_O) \leq$ 3.6V				±50	
ΔI_{DD}	Increase in I_{DD} per input	$V_{IH} = V_{DD}$ –0.6V, Other inputs at V_{DD} or Gnd				400	

Electrical Characteristics over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

(continued from previous page)

DC Characteristics ($2.3V \leq V_{DD} \leq 2.7V$)

Description	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Diode	I_{IK} = –18mA	2.3			–1.2	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100µA	2.3 -2.7	V_{DD}– 0.2			
		I_{OH} = –12mA	2.3	1.8			
		I_{OH} = –18mA		1.7			
V_{OL}	LOW Level Output Voltage	I_{OL} = 100µA	2.3 - 2.7			0.2	
		I_{OL} = 12mA	2.3			0.4	
		I_{OL} = 18mA				0.5	
		I_{OL} = 24mA				0.55	
I_I	Input Leakage Current	V_I = V_{DD} or GND	2.7			±5.0	µA
I_{OZ}	3-State Output Leakage	V_O = 3.6V	2.3			±10	
I_{OFF}	Power-OFF Leakage Current	V_I or $V_O \leq$ 3.6V	0			10	
I_{HOLD}(1)	Bus Hold Current A or B Outputs	V_I = 0.7V	2.5		90		µA
		V_I = 1.7V			–90		
I_{DD}	Quiescent Supply Current	V_I = V_{DD} or GND	2.3 - 2.7			40	
		$V_{DD} \leq (V_I, V_O) \leq$ 3.6V				±40	
ΔI_{DD}	Increase in I_{DD} per input	V_{IH} = V_{DD} –0.6V, Inputs at V_{DD} or Gnd				400	

Note:
1. Not Guaranteed

Electrical Characteristics over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

(continued from previous page)

DC Characteristics ($1.65V \leq V_{DD} \leq 1.95V$)

Description	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Diode	$I_{IK} = -18mA$	1.65			–1.2	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100\mu A$	1.65-1.95	$V_{DD} -0.2$			
		$I_{OH} = -6mA$	1.65	1.4			
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\mu A$				0.2	
		$I_{OL} = 6mA$				0.3	
I_I	Input Leakage Current	$V_I = V_{DD}$ or GND	1.95			±5.0	µA
I_{OZ}	3-State Output Leakage	$V_O = 3.6V$	1.65			±10	
I_{OFF}	Power-OFF Leakage Current	$V_I = V_O \leq 3.6V$	0			10	
I_{HOLD}(1)	Bus Hold Current A or B Outputs	$V_I = 0.4$	1.65		50		
		$V_I = 1.3$			–50		
I_{DD}	Quiescent Supply Current	$V_I = V_{DD}$ or GND	1.65-1.95			20	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				±20	
ΔI_{DD}	Increase in I_{DD} per input	$V_I = V_{DD} –06V$, Other inputs at V_{DD} or Gnd				400	

Note:
1. Not Guaranteed

AC Electrical Characteristics

Symbol	Parameter	T_A = –40°C to +85°C, C_L = 50pF, R_L = 500Ω						Units
		V_{DD} = 1.8V ±0.15V		V_{DD} = 2.5V ±0.2V		V_{DD} = 3.3V ±0.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Prop Delay, D to Q	1.5	4.0	1.0	3.2	0.5	2.7	ns
t_{PLH}, t_{PHL}	Prop Delay, LE to Q	2.0	5.0	1.5	4.2	1	3.1	
t_{PZH}, t_{PZL}	Output Enable Time	2.0	5.0	1.5	4.7	1.0	3.1	
t_{PHZ}, t_{PLZ}	Output Disable Time	2.0	5.0	1.5	4.0	1.5	3.7	
t_{OSHL} t_{OSLH}	Output to Output Skew(1)		0.5		0.5		0.5	

Note

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH or LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

AC Setup Requirements

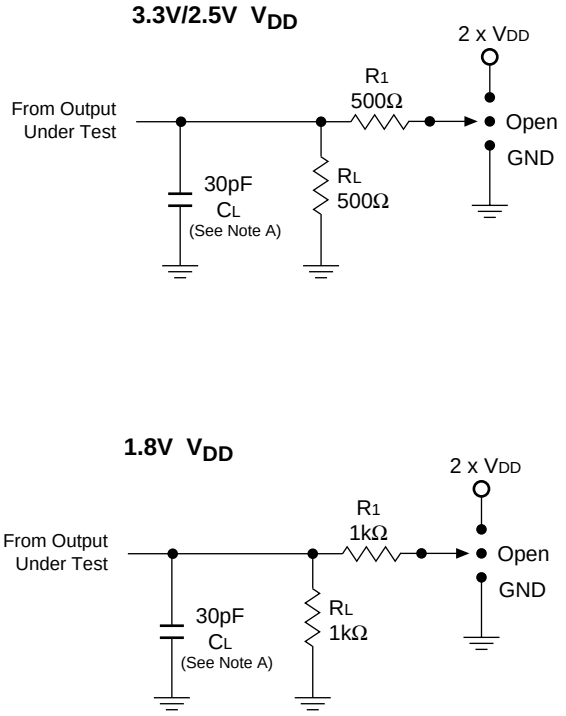
Symbol	Parameter	T_A = –40°C to +85°C, C_L = 50pF, R_L = 500Ω						Units
		V_{DD} = 1.8V ±0.15V		V_{DD} = 2.5V ±0.2V		V_{DD} = 3.3V ±0.3V		
		Min.	Typ.	Min.	Typ.	Min.	Typ.	
t_{SU}	Setup Time, D to LE	1.0		0.5		0.5		ns
t_H	Hold Time, D to LE	1.0		0.5		0.8		
t_W	LE Pulse Width, High	1.5		1.5		1.5		

Capacitance

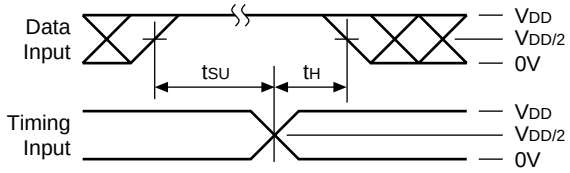
Symbol	Parameter	Conditions	T_A = +25°C Typical	Units
C_{IN}	Input Capacitance	V_{DD} = 1.8, 2.5V or 3.3V, V_I = 0V or V_{DD}	6	pF
C_{OUT}	Output Capacitance	V_I = 0V or V_{DD}, V_{DD} = 1.8V, 2.5V or 3.3V	7	
C_{PD}	Power Dissipation Capacitance	V_I = 0V or V_{DD}, F = 10 MHz V_{DD} = 1.8V, 2.5V or 3.3V	20	

Test Circuits and Switching Waveforms

Parameter Measurement Information (V_{DD} = 1.65V - 3.6V)



Setup, Hold, and Release Timing



Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

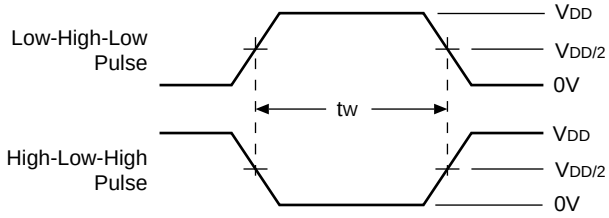
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2ns, t_f ≤ 2ns, ***measured from 10% to 90%, unless otherwise specified.***

D. The outputs are measured one at a time with one transition per measurement.

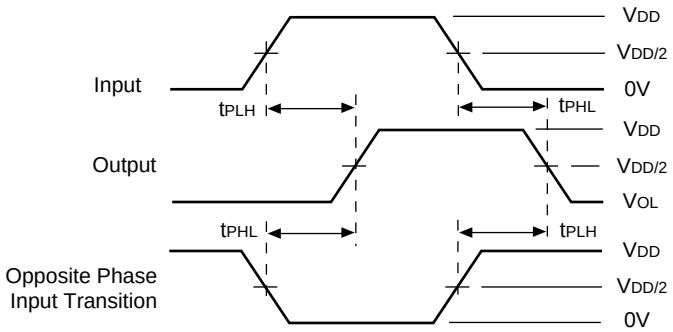
Switch Position

Test	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	GND

Pulse Width



Propagation Delay



Enable Disable Timing