EG&G RETICON

# RA1441A
## Solid State Image Sensor Array

## General Description

The RA1441A is a self-scanned area photodiode array containing 14 rows of 41 sensing elements each. The center-to-center spacing of the elements along each row is 4.1 mils; the center-to-center spacing between rows is 3.6 mils.

Scanning is accomplished by means of a static shift register which sequentially samples the diodes in each line with all 14 lines being read out in parallel. The shift register is driven by an externally-generated single-phase TTL level Clock which determines the sample frequency. The device is operated in the internal start mode; no additional timing signals are required. There is a "flyback" time of two sample periods between the completion of one scan and the beginning of the next, thus, the readout time is given by $43/f_S$, where $f_S$ is the clock frequency. An EOS output pulse is provided during the flyback time to indicate the completion of each scan.

## Package

The RA1441A is packaged in a standard 22-pin ceramic DIP with a ground and polished window. Package dimensions are approximately 0.4 x 1.1 inches. Pinout configuration is shown in Figure 1 and package dimensions are shown in Figure 5.

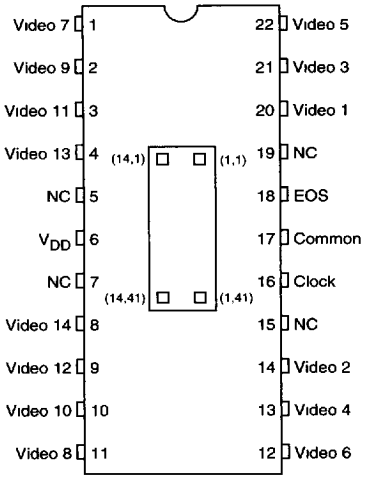


**Figure 1. Pinout Configuration**

## Performance

A test circuit which provides the clock input, load resistors and biasing is shown in Figure 2. Clock frequency is set by potentiometer $R_1$ and operation is guaranteed up to 400 kHz.

Typical spectral response is shown in Figure 3.

## Equivalent Circuit and Timing

Figure 4 is an equivalent circuit showing a 3 x 3 section of the RA1441A. To accomplish each scan, a sampling pulse is automatically loaded and clocked through the shift register so that each cell is accessed in sequence for one clock period. A source follower on each cell provides a high level boxcar type output across an external load resistor connected between each video line and common. Note that while a cell is being sampled, the previous cell is being reset to the negative supply voltage. Between the time it is reset and the time it is accessed on the next scan, the voltage on a cell will decay by an amount proportional to the exposure on that cell (light intensity times scan time). Thus, the remaining voltage on the cell when it is sampled is a measure of the light intensity. The output becomes more positive with increasing exposure, saturating at 0V (common). The EOS signal is normally obtained across a load resistor connected between the EOS output and $V_{DD}$.

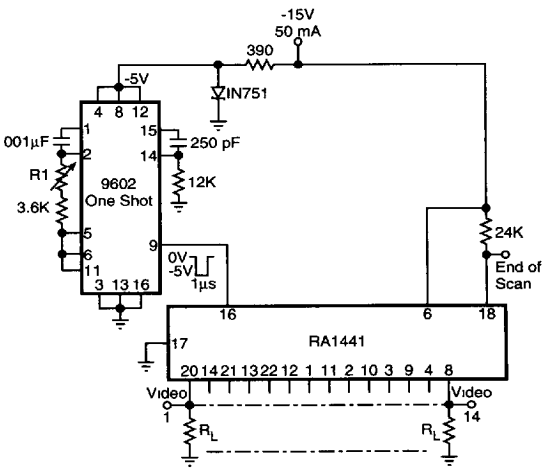


**Figure 2. Test Circuit Schematic**



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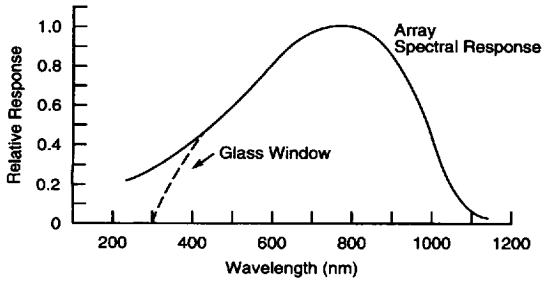


**Figure 3. Typical Spectral Response**

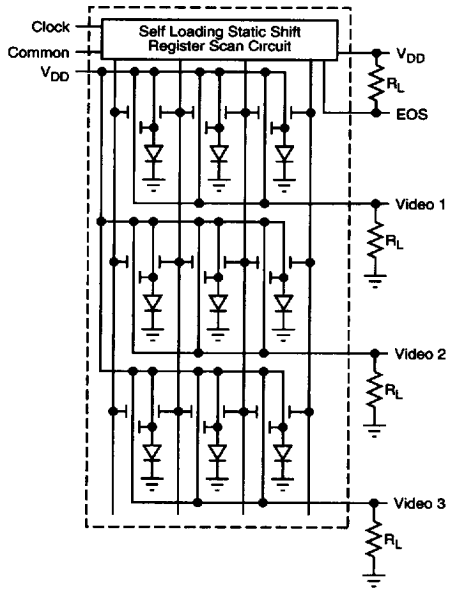


**Figure 4. Equivalent Circuit**

## RC0501A Evaluation Board for RA1441A Photodiode Array

This board, which mates with a standard 22-pin edge connector, provides appropriate interface circuits for evaluating the RA1441A. The circuit requires a single negative supply voltage and provides clock, sync, and all video outputs. As supplied, the clock frequency may be adjusted over the range 50 to 200 kHz using a trim pot. Higher or lower frequency ranges can be obtained by simply changing a capacitor on the board. If desired, an external clock may be used by changing in the INT-EXT jumper to external and connecting the external clock to pin 21.

The video outputs are taken across 51KΩ load resistors suitable for operation up to about 200 kHz. At higher frequencies (up to 400 kHz) lower value load resistors should be used. Output voltage swing (dark to saturation) is proportional to load resistance and $V_{DD}$, and is about 2V with 50KΩ loads and -17V. $V_{DD}$ can be operated between -12 to -17V. External capacitance should be kept below 50 pF on all outputs. Clock supplied on pin 22 of edge connector is inverted from that supplied to pin 16 of the array.

**Table 1. Electrical Characteristics (25°C) [1]**
**(Voltages with respect to common)**

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Supply voltage (single supply) | -12 | | -17 | V |
| Clock amplitude (single phase) | -5 | | -15 | V |
| Maximum scan rate | | | 400 | kHz |
| Average output voltage from saturation to dark (-15V supply, 51KΩ load, 100 kHz scan rate) | | -2.0 | | V |
| Timing | | | 43 | clock cycles per scan |

**Note:**
[1] Test Conditions:
a. $V_{DD}$ = -17V with respect to common
b. Clock swing = -12V with respect to common
c. Clock frequency = 250 kHz
d. Load resistance = 51KΩ
e. 2870°K Tungsten light source
f. Approximate 50% saturation level

**Table 2. Electro-Optical Characteristics [1,2]**

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Saturation exposure | .042 | .070 | .170 | $\mu J/cm^2$ |
| Dark level nonuniformity [2] | | | ±10 | % |
| Nonuniformity (per line) at 50% saturation [2] | | | ±12 | % |
| Line-to-line deviation | | | 10 | % |
| Dark level minimum diode | -2.25 | | -3.25 | V |

**Notes:**
[1] Test Conditions:
a. $V_{DD}$ = -17V with respect to common
b. Clock swing = -12V with respect to common
c. Clock frequency = 250 kHz
d. Load resistance = 51KΩ
e. 2870°K Tungsten light source
f. Approximate 50% saturation level
[2] Nonuniformity is defined as the difference in output voltage of the highest and lowest elements in each line divided by the average voltage swing between dark and saturation. The 41st element of each row is not included in nonuniformity measurements.

**Table 3. Mechanical Characteristics**

| | Typ | Units |
|---|---|---|
| Number of diodes | 574 | |
| Element spacing center-to-center | 4.1 along row | mils |
| | 3.6 between rows | mils |
| 22-Pin DIP package size | | |
| Width | 0.4 | inch |
| Length | 1.080 | inch |

## Absolute Maximum Rating

| | Min | Max | Units |
|---|---|---|---|
| Storage temperature | -25 | +85 | °C |
| Temperature under bias | 0 | +70 | °C |

22-pin Ceramic

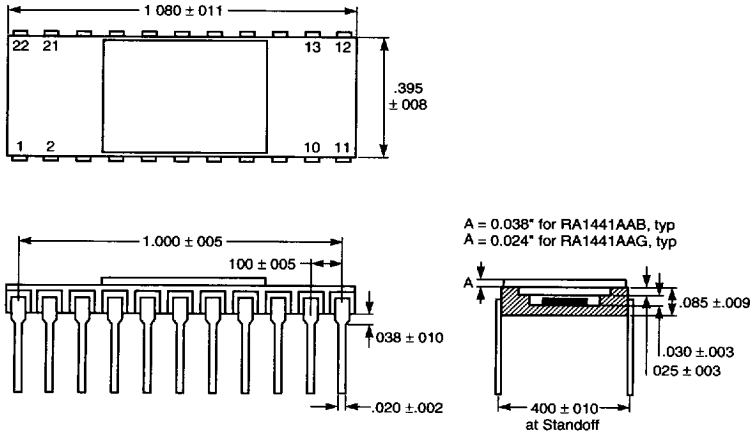


**Figure 5. Package Dimensions**

## Ordering Information *

| Part Number | Evaluation Circuit |
|---|---|
| RA1441AAB-011 | RC0501ANN-011 |

* Includes standard devices. For options, consult your local sales office.