PN CODER
STEL-1032

ASIC
Custom
Products
Division

STANFORD
TELECOM®

FEATURES

- **3 independent PN code generators**
- **Independent clocks, controls and outputs**
- **Microprocessor control interface**
- **Composite code generation capabilities**
- **Punctual, early and late outputs for code tracking**
- **30 MHz operation**
- **Low power CMOS**
- **Military and commercial temperature ranges available**

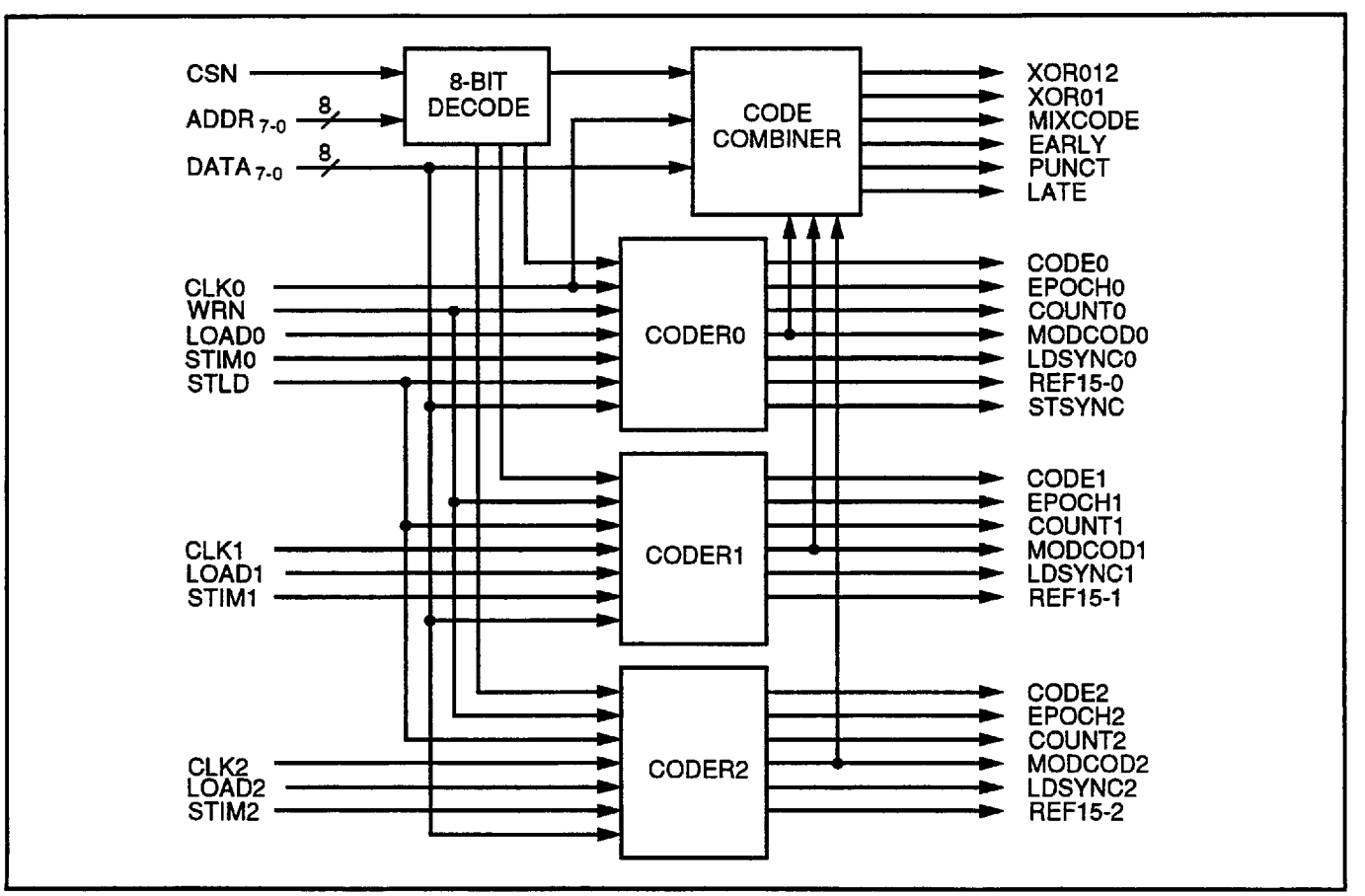
APPLICATIONS

- **Pseudorandom (PN) code generation**
- **Gold Code generation**
- **JPL Ranging Code generation**
- **Syncopated Code generation**

FUNCTIONAL DESCRIPTION

The STEL-1032 PN (Pseudo-Random Number) Coder provides the communications industry with a cost-effective and compact solution to code generation. The device's unique architectural design provides a power-efficient, high-speed code generator able to produce any 3 maximal or non-maximal length codes with up to 32 feedback taps per generator, and code lengths up to 2^{32}-1 (4,394,967,295) bits. Capabilities for modulo-2 addition (EXOR), code modulation, and nonlinear composite code generation are also provided in the device. The device can be programmed very easily via the microprocessor interface.

BLOCK DIAGRAM

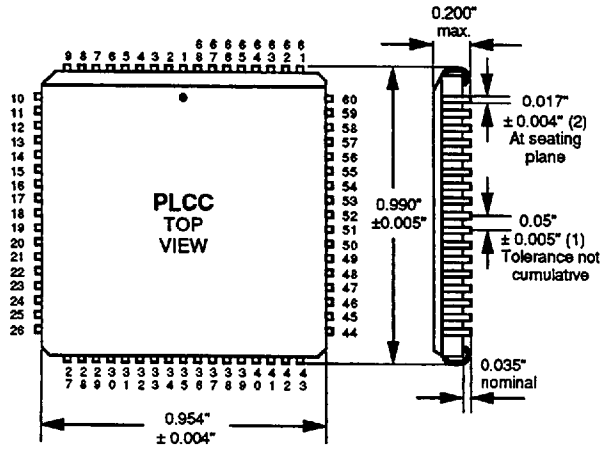


CIRCUIT DESCRIPTION

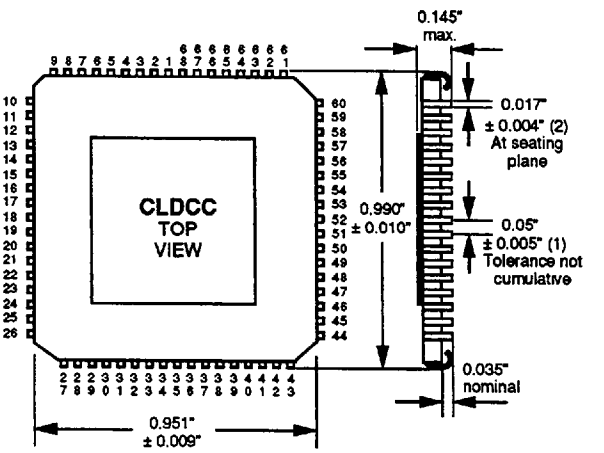
The STEL-1032 PN (Pseudo-Random Number) Coder generates the codes using three 32-bit registers. The feedback tap combinations are controlled by the MASK Registers, and any number of taps may be selected. In this way each of the three coders can independently generate all possible codes with lengths up to 2^{32}-1 (4,294,967,295). The codes can be started at any random point by loading the start code in the INIT Registers, and a specific position in any of the codes can be detected, according to the values stored in the EPOCH Registers. The codes can be made to restart at this point if desired. In addition to the three independent codes that can be generated, the outputs of code generators 0 and 1 can be EXORed together, and similarly the outputs of all three generators can be EXORed together, greatly expanding the lengths and versatilities of the codes. The output of code the combiner is also available both late and early by one half of a clock cycle relative to the punctual code, and nonlinear codes can be generated by means of an internal programmable lookup table.

PIN CONFIGURATION

Package: 68 pin PLCC
Thermal coefficient, θ_{ja} = 36° C/W



Package: 68 pin PLCC
Thermal coefficient, θ_{ja} = 34° C/W



PIN CONNECTIONS

1	CLK_1	15	$ADDR_6$	29	$REF15_0$	43	$CODE_2$	57	$DATA_4$
2	V_{DD}	16	$ADDR_7$	30	$MODCOD_0$	44	V_{SS}	58	$DATA_5$
3	V_{SS}	17	XOR012	31	$CODE_0$	45	V_{DD}	59	$DATA_6$
4	CSN	18	V_{DD}	32	$COUNT_1$	46	$LDSYNC_0$	60	$DATA_7$
5	CLK_0	19	V_{SS}	33	$EPOCH_1$	47	$LDSYNC_1$	61	TEST
6	STLD	20	XOR01	34	$REF15_1$	48	$LDSYNC_2$	62	$STIM_0$
7	STSYNC	21	MIXCODE	35	V_{SS}	49	WRN	63	$STIM_1$
8	$ADDR_0$	22	LATE	36	V_{DD}	50	RESET	64	$STIM_2$
9	$ADDR_1$	23	EARLY	37	$MODCOD_1$	51	V_{SS}	65	CLK_2
10	V_{SS}	24	PUNCT	38	$CODE_1$	52	V_{DD}	66	$LOAD_0$
11	$ADDR_2$	25	V_{DD}	39	$COUNT_2$	53	$DATA_0$	67	$LOAD_1$
12	$ADDR_3$	26	V_{SS}	40	$EPOCH_2$	54	$DATA_1$	68	$LOAD_2$
13	$ADDR_4$	27	$COUNT_0$	41	$REF15_2$	55	$DATA_2$		
14	$ADDR_5$	28	$EPOCH_0$	42	$MODCOD_2$	56	$DATA_3$		

INPUT SIGNALS

RESET

When the reset input is low, all the registers inside the coder are reset to zero. Normal operation will not commence until an initialization value has been loaded into the PN Generators from the corresponding INIT registers.

CLK_0-CLK_2

Clock inputs to Coders 0-2, respectively. All operations occur on the rising edges of the clocks, with the exception of the EARLY and LATE outputs, which change on the falling edges of CLK_0. The clocks should nominally be square waves, with a maximum frequency of 30 MHz.

WRN

Register write control. When this line is low data is written into the register(s) selected by the address lines and latched on the rising edge of WRN.

CSN

A low level on the Chip Select input enables the loading of data via the data bus.

$ADDR_0$-$ADDR_4$

Register select address inputs. The addressing of the registers is shown in the table below:

A4	A3	A2	A1	A0	Register Selected
0	0	0	0	0	MASK Register bits 0–7
0	0	0	0	1	MASK Register bits 8–15
0	0	0	1	0	MASK Register bits 16–23
0	0	0	1	1	MASK Register bits 24–31
0	0	1	0	0	INIT Register bits 0–7
0	0	1	0	1	INIT Register bits 8–15
0	0	1	1	0	INIT Register bits 16–23
0	0	1	1	1	INIT Register bits 24–31
0	1	0	0	0	EPOCH Register bits 0–7
0	1	0	0	1	EPOCH Register bits 8–15
0	1	0	1	0	EPOCH Register bits 16–23
0	1	0	1	1	EPOCH Register bits 24–31
0	1	1	0	0	COUNT Register bits 0–7
0	1	1	0	1	COUNT Register bits 8–15
0	1	1	1	0	COUNT Register bits 16–23
0	1	1	1	1	COUNT Register bits 24–31
1	0	0	0	0	MUX Register bits 0–4
1	0	0	0	1	CTL Register bits 0–7

$ADDR_5$-$ADDR_7$

Coder and code combiner select address inputs. The addressing of the registers is shown in the table below:

A7	A6	A5	Coder Selected
0	0	0	Coder 0
0	0	1	Coder 1
0	1	0	Coder 2
0	1	1	All coders
1	0	0	Code Combiner Lookup register

$DATA_0$-$DATA_7$

Data bus inputs, used to write data to the registers. $DATA_7$ is the MSB and $DATA_0$ is the LSB.

$LOAD_0$-$LOAD_2$

On the rising edge of the clock following the falling edge of a load input a load command is issued. This will cause the corresponding PN Generator register and Counter register are loaded with the contents of the corresponding INIT register and COUNT register, respectively.

$STIM_0$-$STIM_2$

Data applied to the $STIM_{0-2}$ inputs is modulo-2 added (EXORed) with the outputs of the corresponding PN Generator ($CODE_{0-2}$). The data is latched in on the falling edges of the STLD input.

STLD

The STLD signal is used to latch the data appearing on the $STIM_{0-2}$ inputs. The data is latched in on the falling edge of this signal, the stim load command.

OUTPUT SIGNALS

TEST

The TEST output is used for test purposes only. It should be left unconnected in normal use.

$CODE_0$-$CODE_2$

The $CODE_{0-2}$ outputs are the outputs of the PN Generators 0-2. The register bit in the PN Generator from which the output is derived is set by the Phase Multiplexer.

$MODCOD_0$-$MODCOD_2$

The $MODCOD_{0-2}$ outputs are the $CODE_{0-2}$ signals after modulation by the $STIM_{0-2}$ inputs. The register bit in the PN Generator from which the output is derived is set by the Phase Mux.

PUNCT

The PUNCT output is an exact replica of the MIXCODE output delayed by one clock cycle.

EARLY

The EARLY output is an exact replica of the PUNCT output advanced by half a clock cycle. This is achieved by clocking the signal into the output register on the falling edge of CLK_0. In order to make the advance exactly half a clock cycle, the duty cycle of CLK_0 must be exactly 50%. This also applies to the timing of the LATE signal.

LATE

The LATE output is an exact replica of the PUNCT output delayed by half a clock cycle. This is achieved by clocking the signal into the output register on the falling edge of CLK_0

$LDSYNC_0$-$LDSYNC_2$

A Loadsync output goes low for one clock cycle after the contents of the corresponding INIT register have been loaded into the corresponding PN Generator. This pulse indicates the clock cycle in which the PN Generator value is identical to that of the INIT register.

$REF15_0$-$REF15_2$

The $REF15_{0\text{-}2}$ outputs are reference codes derived from the fifteenth taps of the corresponding PN Generator. These outputs will be identical to the corresponding $CODE_{0\text{-}2}$ outputs when the data stored in the corresponding Phase Mux is 01110.

STSYNC

The STSYNC output is normally high and goes low for one clock cycle following a falling edge on the STLD signal. The result of the new modulation bits will appear on the output codes $MODCOD_{0\text{-}2}$ during this clock cycle.

$EPOCH_0$-$EPOCH_2$

The $EPOCH_{0\text{-}2}$ outputs are normally high and go low whenever the corresponding PN Generator code is equal to the code stored in the corresponding Epoch register. Note that this condition will not be detected, and the $EPOCH_n$ output will not go low, if this condition occurs within 2 clock cycles of a rising edge on the corresponding input.

$COUNT_0$-$COUNT_2$

The $COUNT_{0\text{-}2}$ outputs are delayed replicas of the $LDSYNC_{0\text{-}2}$ outputs. The length of the delay is equal (in clock cycles) to the value stored in the corresponding Count register.

XOR01

The XOR01 output is the result of the modulo-2 addition (XOR) of the $CODE_0$ and $CODE_1$ signals. The result is delayed by one clock cycle before appearing at the XOR01 output.

XOR012

The XOR012 output is the result of the modulo-2 addition (XOR) of the $CODE_0$, $CODE_1$ and $CODE_2$ signals. The result is delayed by one clock cycle before appearing at the XOR012 output.

MIXCODE

The $MODCOD_{0\text{-}2}$ signals are used to address the Code Combiner Lookup Register. The data bit stored in the location addressed by the three bits of $MODCOD_{0\text{-}2}$ is the MIXCODE output, as shown in the table:

M2	M1	M0	MIXCODE
0	0	0	Lookup Register Bit 0
0	0	1	Lookup Register Bit 1
0	1	0	Lookup Register Bit 2
0	1	1	Lookup Register Bit 3
1	0	0	Lookup Register Bit 4
1	0	1	Lookup Register Bit 5
1	1	0	Lookup Register Bit 6
1	1	1	Lookup Register Bit 7

FUNCTION BLOCKS

Each of the three separate coders contains a number of function blocks. The three coders are completely independent, except for the COUNT and EPOCH functions which go from every coder to every other coder's control logic block. This allows each coder to be controlled by either of the other two coders for the generation of syncopated functions.

PN CODE GENERATOR BLOCK

The 32-bit PN Code generator generates codes with programmable lengths and polynomials. The polynomials are set by programming the desired taps in the Mask register. Each bit in the Mask register which is set to a logic '1' enables the corresponding tap in the PN generator polynomial:

$G=1+D1(x)+D2(x^2)+D3(X^3)\cdots\cdots+D31(X^{31})+D32(X^{32})$

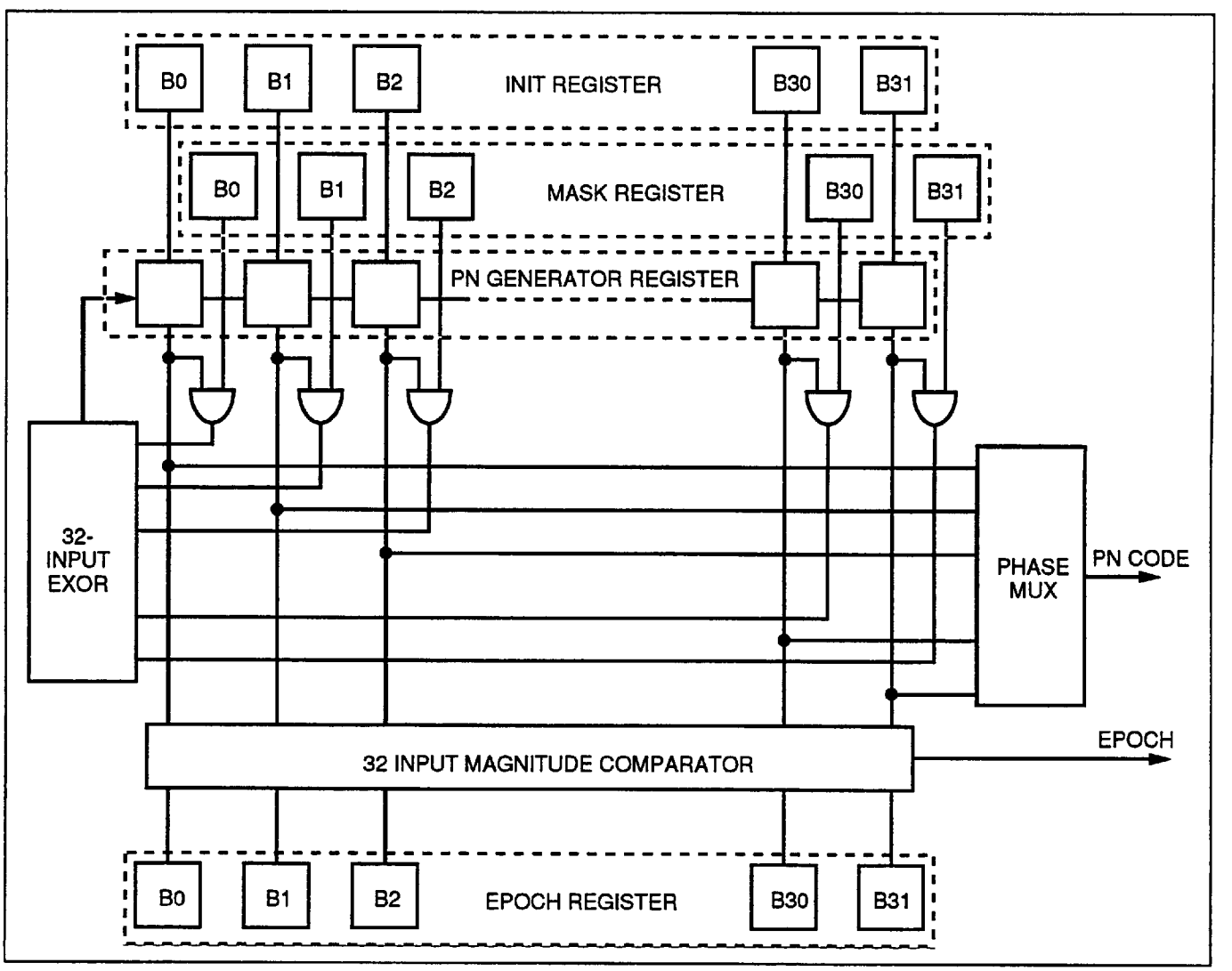
where D1 = Bit 0, D2 = Bit 1, D3 = Bit 2, etc.

A logic '0' disables the tap. Note that the most significant (i.e. last) tap set determines the effective length of the PN generator register. These are the active bits of the PN Generator. e.g., if the most significant tap set is D17 (i.e., D18 through D32 are all zero), then the maximum code length possible with that configuration will be 2^{17}-1 bits.

The start code of the PN sequence is set by loading the code into the INIT register. The code is loaded into the PN generator register under the control of the Control Logic block. This will happen a load command is issued, and also on an **EPOCH** or **COUNT** pulse, if one or both of the functions are programmed. The PN generators should not be re-initialized within 8 clock cycles of being initialized.

EPOCH DETECTOR BLOCKS

Every clock cycle the active bits of the output of the PN Generator are compared with the word stored in the EPOCH register. The **EPOCH** output pulses low each



time a match is found between the active bits in the PN generator and the corresponding bits of the word in the EPOCH register.

COUNTER BLOCK

The 32-bit Counter is programmed by means of the COUNT register. The counter can be started by any of the **COUNT** and **EPOCH** pulses, and once started will count up to the value stored in the COUNT register and then stop. The counter should not be restarted within 8 clock cycles of being started.

CONTROL LOGIC BLOCK

The control logic block performs the functions programmed in the CTL register. The **EPOCH** and **COUNT** outputs of all three coders, as well as the **LOAD** input, are the inputs of the control logic block. Depending on the contents of the CTL register, the PN Generator register may be reloaded from the INIT register, and/or the counter may be reloaded from the COUNT register each time any of these signals are activated.

PHASE MULTIPLEXER BLOCK

The Phase Mux block performs a one-out-of-thirty two selection function. The outputs of all thirty two bits of the PN generator register are fed into the phase mux, and the code stored in the MUX register is used to select one of these. This allows the phasing of the coder output to be varied.

MODULATOR BLOCK

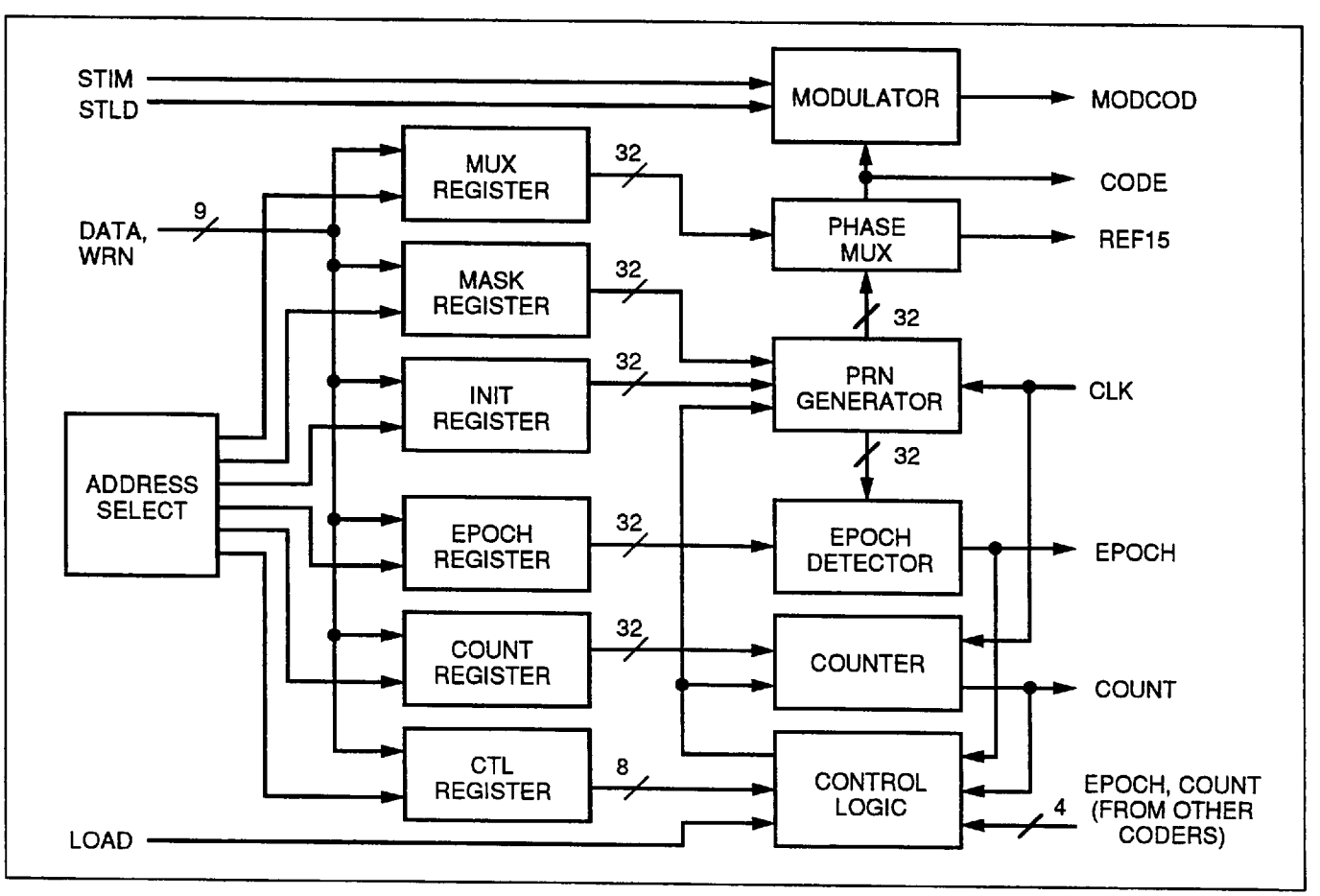
The modulator permits the **CODE** output to be modulated with the **STIM** signal. The modulation function is a logical exclusive-OR (EXOR). New **STIM** bits are loaded into the modulators on each STLD command.

REGISTER BLOCKS

The STEL-1032 is programmed by means of the data stored in the registers. Each of the three independent code generators has a complete set of these registers. The 8-bit data bus is mapped into the 32-bit registers by means of address inputs $\mathbf{ADDR_0}$ and $\mathbf{ADDR_1}$, as shown on page 4.

MASK Registers

The 32-bit Mask register is used to define the active feedback taps in the PN generators. Each bit set to a one enables the corresponding tap. The MASK register is not buffered, and any changes made will affect the PN generator polynomial immediately. Care should



be taken in modifying the contents of the MASK register while the generator is operating, since the bits can only be changed eight (one byte) at a time.

$INIT_{0-2}$ Register

The 32-bit Init register is used to define the start value of the code generated in the PN Generator. The contents of the INIT register are loaded into the PN generator by means of the Control logic. This occurs when a load command is issued, and whenever an **EPOCH** or **COUNT** pulse occurs, when these functions are enabled.

$EPOCH_{0-2}$ Register

The 32-bit Epoch register is used to define the distinct code value to be detected in the PN Generator. The EPOCH register is not buffered, and any changes made will affect the EPOCH detected immediately. Note that all bits of the EPOCH register beyond the most significant feedback tap in the PN generator (i.e. the most significant one in the corresponding MASK register), must always be set to zero, otherwise undesirable effects will occur. e.g. polynomial set by MASK register = 00000101 makes effective length of PN generator eight bits. In this case, bits 8 through 31 of the EPOCH register must be set to zero.

$COUNT_{0-2}$ Register

The 32-bit Count register is used to set the counter stop point. Once triggered, the counter will run for a number of clock cycles equal to the number stored in the COUNT register and then generate a **COUNT** pulse. The contents of the COUNT register are loaded into the counter by means of the Control logic. This occurs when a load command is issued, and whenever an **EPOCH** or **COUNT** pulse occurs, when these functions are enabled.

Phase MUX Register

The 5-bit Phase Mux register is used to select the PN generator register output bits used for the code outputs. The value stored in the Mux register is decoded and determines the tap number used. e.g.

Mux register value = 00000, tap number used =1

Mux register value = 11111, tap number used =32

CTL Register

The 8-bit CTL register is used to define the reloading of the coder and counter. The functions performed by the bits in the CTL register are shown in the tables:

B_7 B_6	Function
0 0	Counter is not reloaded on any EPOCH pulse
0 1	Counter is reloaded on $EPOCH_0$ pulse
1 0	Counter is reloaded on $EPOCH_1$ pulse
1 1	Counter is reloaded on $EPOCH_2$ pulse

B_5 B_4	Function
0 0	Counter is not reloaded on any COUNT pulse
0 1	Counter is reloaded on $COUNT_0$ pulse
1 0	Counter is reloaded on $COUNT_1$ pulse
1 1	Counter is reloaded on $COUNT_2$ pulse

B_3 B_2	Function
0 0	PN gen. is not reloaded on any EPOCH pulse
0 1	PN gen. is reloaded on $EPOCH_0$ pulse
1 0	PN gen. is reloaded on $EPOCH_1$ pulse
1 1	PN gen. is reloaded on $EPOCH_2$ pulse

B_1 B_0	Function
0 0	PN gen. is not reloaded on any COUNT pulse
0 1	PN gen. is reloaded on $COUNT_0$ pulse
1 0	PN gen. is reloaded on $COUNT_1$ pulse
1 1	PN gen. is reloaded on $COUNT_2$ pulse

The CTL register is not buffered, and all changes take place immediately.

CODE COMBINER

The STEL-1032 contains a single Code Combiner block in which the **MODCOD** outputs of the three modulators are used to address a lookup table to produce the **MIXCODE** output. This allows nonlinear codes to be generated.

PROGRAMMING EXAMPLES

1. Using the INIT, MASK, EPOCH and CTL registers to generate a truncated sequence with the polynomial:

$G = 1 + X^3 + X^4$

in generator 0. This polynomial generates the following sequence:

1	0	0	0	
0	1	0	0	
0	0	1	0	
1	0	0	1	
1	1	0	0	
0	1	1	0	
1	0	1	1	
0	1	0	1	
1	0	1	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	
0	1	1	1	
0	0	1	1	
0	0	0	1	(repeats)

Note that this is a maximal-length sequence, i.e., it contains every possible combination of four bits, except 0 0 0 0. The all-zeroes combination never exists in any PN sequence, it is a lockup condition since the all-zeroes combination will always generate a zero in an exclusive-OR function. In addition, any PN generator with an odd number of taps will also have the all-ones state as a lockup condition.

Since this is a 4-bit code only the first four bits of the registers will be considered in this example. It is assumed that all the other bits are set to zero in all the registers. By setting the MASK register to 0011 feedback taps three and four are selected, generating the desired polynomial. By setting the INIT register to 1001 the generator can be made to start at code 1001. By setting the EPOCH register to 0101 and the CTL register to XXXX01XX the generator can be made to detect the code 0101 and then reload the contents of the INIT register. It will then cycle through the following states:

1	0	0	1	
1	1	0	0	
0	1	1	0	
1	0	1	1	
0	1	0	1	(repeats)

Note that it is possible to start any of the PN generators when any specific code is detected in either in itself or in either of the other two generators. In this way it is possible to concatenate codes, as shown in the second example.

2. Syncopated codes. Assuming that generator 0 is set up to generate the same code as in the first example, set up generator 1 to generate the polynomial:

$G = 1 + X^2 + X^3 + X^5$

by setting the MASK register to 01101 (first five bits only, all others zero). This generates non-maximal length sequences, one of which is ten states long, and includes the sequence:

1	1	0	1	0
1	1	1	1	0
0	1	1	1	1
1	0	1	1	1
0	1	0	1	1

By setting the INIT register to 11010 and the EPOCH register to 01011 this sequence can be generated. If CTL register 0 is set to XXXX10X and CTL register 1 is set to XXXX01X the two generators will operate in a syncopated manner, each one restarting the other. Note that each one continues generating its own code until restarted.

3. Direct-sequence spread-spectrum modulation. By using the **STIM** input for the data, a spreading code can be added to the modulation pattern. The result is available at the corresponding **MODCOD** output.

4. Generating a nonlinear code using the Code Combiner block. By writing a data byte into the Code Combiner Lookup Register special codes can be generated. For example, by writing $E8_H$ into this register a code can be generated which produces a one whenever two or more of the **MODCOD** outputs are ones, and a zero at all other times, i.e., a majority function.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125 –65 to +150	°C (Plastic package) °C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD} + 0.3	volts
I_i	DC input current	± 10	mA

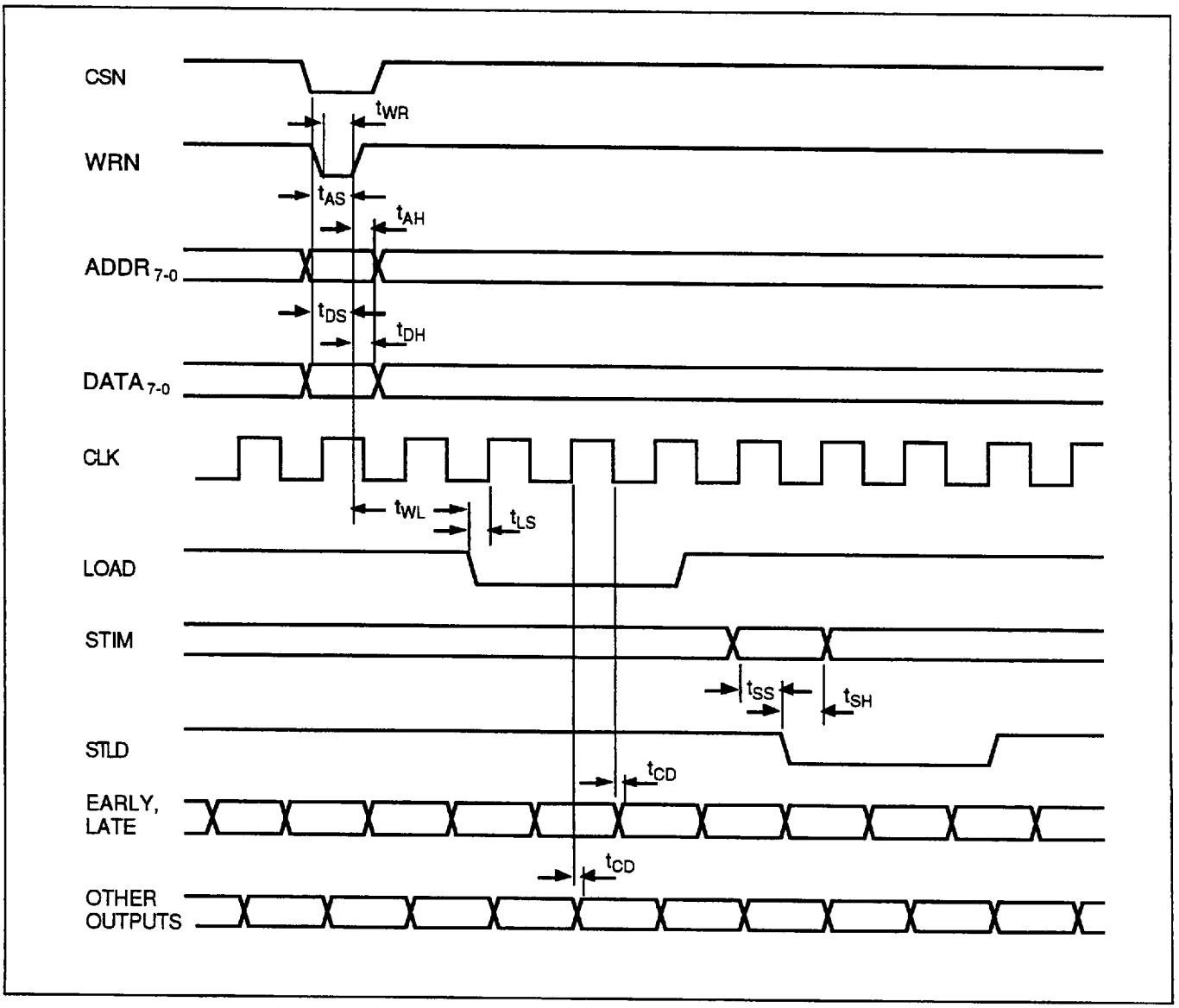
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units	
V_{DD}	Supply Voltage	+5 ± 5%	Volts	
T_a	Operating Temperature (Ambient)	0 to +70	°C	(Plastic package)
		–55 to +125	°C	(Ceramic package)

D.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 V ±5%, V_{SS} = 0 V, T_a = 0° to 70° C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			3.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current			10	µA	$V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current			–10	µA	$V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –4.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +4.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

TIMING DIAGRAM



A.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 V ±5%, V_{SS} = 0 V, T_a = 0° to 70° C)

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{DS}	Data Setup time	10		nsec.	
t_{AS}	Address Setup time	10		nsec.	
t_{DH}	Data Hold time	10		nsec.	
t_{AH}	Address Hold time	10		nsec.	
t_{LS}	Load Setup time	10		nsec.	
t_{WL}	Write to Load delay time	160		nsec.	
t_{DH}	STIM to STLD Setup time	10		nsec.	
t_{AH}	STIM to STLD Hold time	10		nsec.	
t_{CP}	Max. CLK frequency		30	MHz	
t_{LS}	CLK pulse width	10		nsec.	
t_{WR}	WRN pulse width	20		nsec.	
t_{CD}	Clock delay, CLK to any output	5	18	nsec.	Load = 20 pF

Note: The duty cycle of the CLK_0 signal must be 50% in order to achieve correct timing of the **EARLY** and **LATE** signals, since these outputs are latched on the falling edge of the clock and the **PUNCT** signal is latched on the rising edge.

FOR FURTHER INFORMATION

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