STEL-1377Q/S
Data Sheet

STEL-1377Q (Quadrature)

STEL-1377S (Single Channel)

32-Bit Resolution FM & PM Modulated Direct Digital Frequency Synthesizer

intel

FEATURES

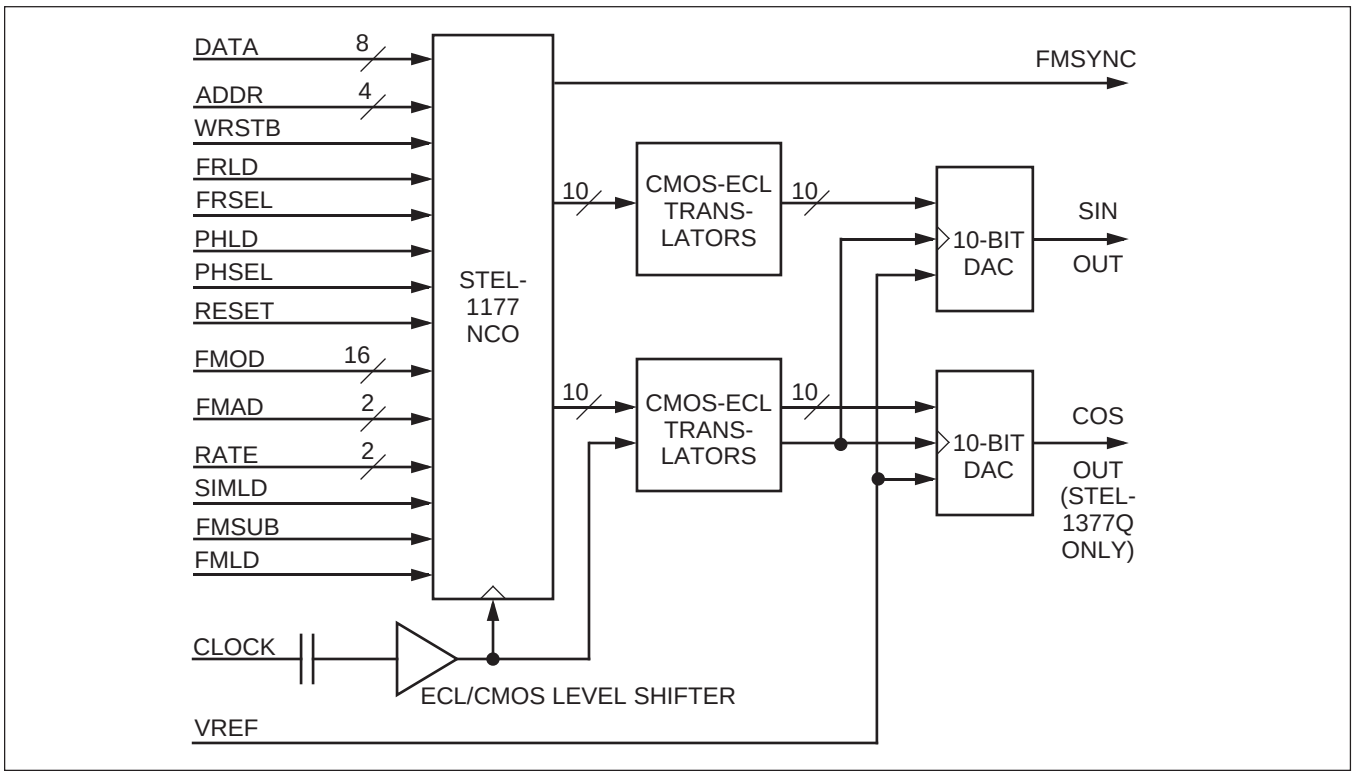
- **HIGH MAXIMUM CLOCK FREQUENCY**
  - **UP TO 60 MHz**
- **HIGH OUTPUT BANDWIDTH**
  - **UP TO 25 MHz OUTPUT FREQUENCY**
- **HIGH FREQUENCY–RESOLUTION**
  - **32 BITS, 14 milliHz @ 60 MHz**
- **HIGH SPEED FREQUENCY HOPPING OR MODULATION**
  - **MAXIMUM UPDATE RATE 15 MHz**
- **PRECISION PHASE MODULATION**
  - **12 BITS, 0.09° RESOLUTION CAN BE USED FOR LINEAR PM OR PULSE-SHAPED PSK AT UP TO 15 MHz**
- **PRECISION FREQUENCY MODULATION**
  - **16 BITS RESOLUTION, CAN BE USED FOR LINEAR FM OR PULSE-SHAPED FSK**
- **SINE AND COSINE OUTPUTS (STEL-1377Q) OR SINGLE ENDED OUTPUT (STEL-1377S) FOR LOWER POWER CONSUMPTION**
- **HIGH-SPEED, LOW GLITCH ECL DACS**
- **HIGH SPECTRAL PURITY**
  - **–65 dBc SPURIOUS TYPICAL**
- **3.75" BY 1.6" BY 0.4"**

The STEL-1377Q is a complete Quadrature Direct Digital Frequency Synthesizer (DDS) in a single DIL package measuring only 3.75 x 1.6". The STEL-1377S provides a single ended output only. The STEL-1377 makes it possible to use DDS technology in applications requiring quadrature outputs as well as frequency and phase modulation in a small package. The STEL-1377 is a printed circuit unit using the STEL-1177 PM and FM Numerically Controlled Oscillator (NCO) chip driving two high-speed 10-bit DACs (Sony CX20201A-1) to generate quadrature analog output signals. Surface mount technology (SMT) components are used throughout. The device is guaranteed to operate at clock frequencies up to 60 MHz over the temperature range of 0-70°C, giving an output frequency range of 0 to over 25 MHz, with a frequency resolution of 14 milliHz at a clock frequency of 60 MHz. In addition, the device features phase and frequency modulation capabilities at extremely high modulation rates, up to 25% of the clock frequency. For more detailed information on the STEL-1177 NCO please refer to the STEL-1177 data sheet. For more information on the DAC please refer to the Sony CX20201A-1 data sheet. The output frequency is directly related to the clock frequency by the following:

$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{32}}$$

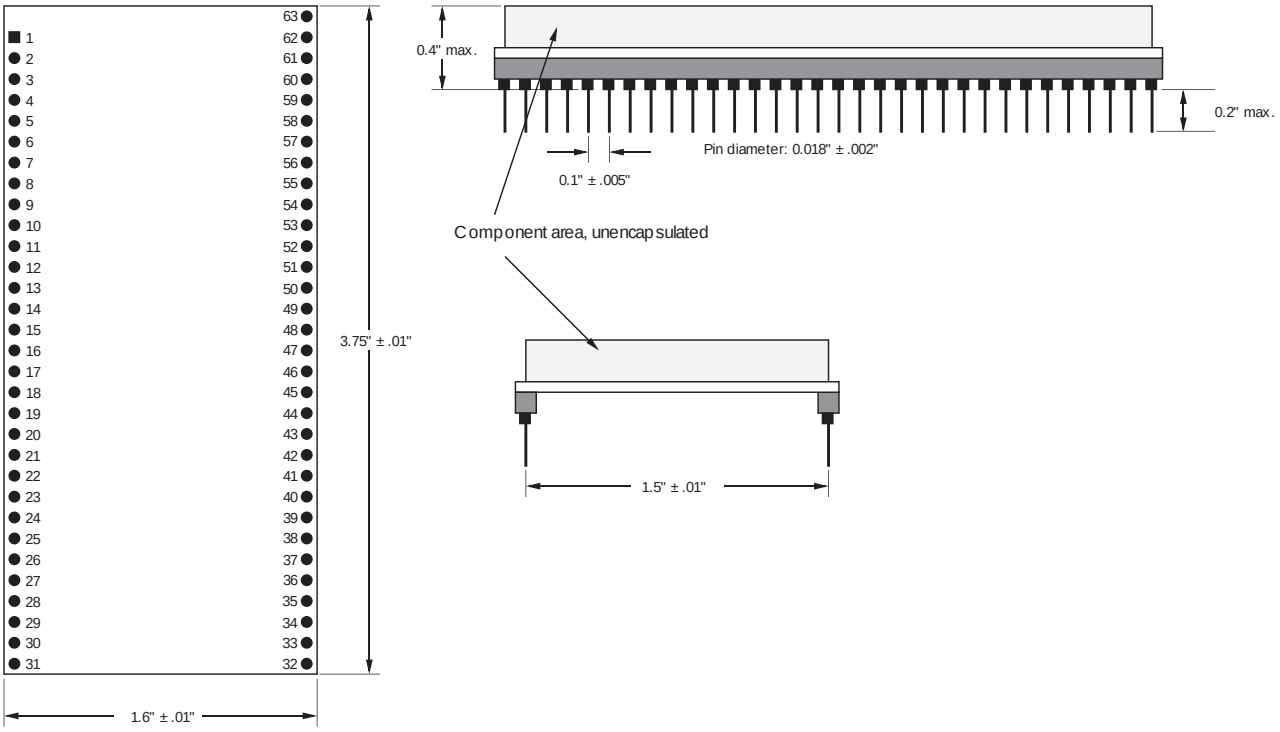
where: f_o is the frequency of the output signal
and: f_c is the clock frequency.

BLOCK DIAGRAM



PIN CONFIGURATION

Package: 63-pin DIP



PIN CONNECTIONS

1	CLOCK	17	$FMOD_8$	33	$DATA_6$	49	PHLD
2	V_{EE}	18	$FMOD_9$	34	$DATA_5$	50	WRSTB
3	$RATE_0$	19	$FMOD_{10}$	35	$DATA_4$	51	PHSEL
4	$RATE_1$	20	$FMOD_{11}$	36	$DATA_3$	52	V_{DD}
5	FMLD	21	$FMOD_{12}$	37	$DATA_2$	53	CSEL
6	FMSUB	22	$FMOD_{13}$	38	$DATA_1$	54	V_{SS}
7	$FMADDR_0$	23	$FMOD_{14}$	39	$DATA_0$	55	CIN
8	$FMADDR_1$	24	$FMOD_{15}$	40	$ADDR_0$	56	V_{DD}
9	$FMOD_0$	25	SIMLD	41	$ADDR_1$	57	$DV_{EE\ (DAC)}$
10	$FMOD_1$	26	N.C.	42	$ADDR_2$	58	$AV_{EE\ (DAC)}$
11	$FMOD_2$	27	N.C.	43	$ADDR_3$	59	V_{SS}
12	$FMOD_3$	28	N.C.	44	FRSEL	60	OUT (SIN)
13	$FMOD_4$	29	N.C.	45	FMSYNC	61	V_{EE}
14	$FMOD_5$	30	N.C.	46	V_{SS}	62	V_{REF}
15	$FMOD_6$	31	N.C.	47	FRLD	63	OUT (COS)
16	$FMOD_7$	32	$DATA_7$	48	RESET		(STEL-1377Q only)

CIRCUIT DESCRIPTION

The frequency of the NCO is determined by the number stored in the Δ-Phase register which is programmed from the interface bus. The number stored in the Δ-Phase register is added to the current contents of the accumulator every clock cycle to generate a monotonically increasing phase angle. By modulating this number the frequency of the NCO can be modulated. The NCO generates digitized sine and cosine functions by addressing sine and cosine lookup tables with the phase accumulator. Phase modulation data is added to the accumulator output before the lookup tables. Please refer to the STEL-1177 data sheet for information on programming the NCO.

The NCO output is passed through CMOS to ECL level translators and loaded synchronously into two high-speed 10-bit DACs. The full-scale outputs of the DACs is determined by the voltage on the VREF input, and this can be used to amplitude modulate the output signals.

FUNCTION BLOCK DESCRIPTION

NCO BLOCK

The NCO block is the core of the STEL-1377 DDS. It consists of a front-end which may be programmed from the control inputs. The NCO is described fully in the STEL-1177 data sheet. Please refer to this data sheet for more detailed information.

LEVEL TRANSLATOR BLOCK

The outputs of the NCO block are CMOS level digital signals. These are translated to ECL levels for optimum operation of the DAC.

CLOCK GENERATION BLOCK

The clock generation block generates the different clocks required for the NCO and DAC blocks from the incoming ECL or sinusoidal clock signal.

DAC BLOCK

The DAC block consists of the Sony CX20201A-1 digital to analog converters and the necessary supporting circuitry.

INPUT SIGNALS

RESET

The **RESET** input is asynchronous and active low, and clears all the registers in the device. When **RESET** goes low, all registers are cleared within 20 nsecs, and normal operation will resume after this signal returns high. The outputs will go to the zero level during the reset, and thereafter will remain at the value corresponding to zero phase until new frequency or modulation (either frequency or phase) data is loaded with the **FRLD**, **FMLD**, or **PHLD** inputs after the **RESET** returns high.

CLOCK

All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be a square wave or sine wave at a maximum frequency of 60 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 5 nanoseconds.

CSEL

The **C**hip **Sel**ect input is used to control the writing of data into the chip. It is active low. When this input is high all data writing via the $\mathbf{DATA_{7\text{-}0}}$ bus is inhibited.

$\mathbf{DATA_7}$ through $\mathbf{DATA_0}$

The 8-bit $\mathbf{DATA_{7\text{-}0}}$ bus is used to program the two 32-bit Δ-Phase Registers and the two 12-bit Phase Modulation Registers. $\mathbf{DATA_0}$ is the least significant bit of the bus. The data programmed into the Δ-Phase registers in this way determines the carrier frequency of the NCO.

$\mathbf{ADDR_3}$ through $\mathbf{ADDR_0}$

The four address lines $\mathbf{ADDR_{3\text{-}0}}$ control the use of the $\mathbf{DATA_{7\text{-}0}}$ bus for writing frequency data to the Δ-Phase Buffer Registers, and phase data to the Phase Buffer Registers, as shown in the table:

$\mathbf{ADDR_3}$	$\mathbf{ADDR_1}$	$\mathbf{ADDR_0}$	Register Field
0	0	0	Δ-Phase Bits 0 (LSB)–7
0	0	1	Δ-Phase Bits 8–15
0	1	0	Δ-Phase Bits 16–23
0	1	1	Δ-Phase Bits 24–31
1	0	0	Sine Bits 0(LSB)–3*
1	0	1	Sine Bits 4-11*
1	1	0	Cosine Bits 0(LSB)–3*
1	1	1	Cosine Bits 4-11*

$\mathbf{ADDR_3}$	$\mathbf{ADDR_2}$	Register Selected
0	0	Δ-Phase Buffer Register 'A'
0	1	Δ-Phase Buffer Register 'B'
1	X	Phase Buffer Registers

Note: The Phase Buffer Registers are 12-bit registers. When the least significant bytes of these registers are selected ($\mathbf{ADDR_{3\text{-}0}}$ =1XX0), $\mathbf{DATA_{7\text{-}4}}$ is written into

Bits 3–0 of the registers. In all cases, it is not necessary to reload unchanged bytes, and the byte loading sequence may be random.

WRSTB
The **Wr**ite **St**ro**b**e input is used to latch the data on the $\mathbf{DATA_{7-0}}$ bus into the device. On the rising edge of the **WRSTB** input, the information on the 8-bit data bus is transferred to the buffer register selected by the $\mathbf{ADDR_{3-0}}$ bus.

FRSEL
The **F**requency **R**egister **Sel**ect line is used to control the mux which selects the Δ-Phase Buffer Register in use. When this signal is high Δ-Phase Buffer Register 'A' is selected as the source for the Δ-Phase ALU, and the frequency corresponding to the data stored in this register will be generated by the NCO after the next falling edge on the **FRLD** input. When this line is low, Δ-Phase Buffer Register 'B' is selected as the source.

FRLD
The **Fr**equency **Loa**d input is used to control the transfer of the data from the Δ-Phase Buffer Registers to the Δ-Phase ALU. The data at the output of the Mux Block must be valid during the clock cycle following the falling edge of **FRLD**. The data is then transferred during the subsequent cycle. The frequency of the NCO output will change 19 clock cycles after the **FRLD** command due to pipelining delays.

PHSEL
The **Ph**ase Source **Sel**ect input selects the sources of data for the Phase ALUs. When it is high the sources are the Sine and Cosine Phase Buffer Registers. They are loaded from the $\mathbf{DATA_{7-0}}$ bus by setting address line $\mathbf{ADDR_3}$ high, as shown in the tables. When **PHSEL** is low, the sources for the phase modulation data are the $\mathbf{DATA_{7-0}}$ and $\mathbf{ADDR_{3-0}}$ inputs, and the data will be loaded independently of the states of **WRSTB** and **CSEL**. The data on these 12 lines is presented directly as a parallel 12-bit word to both Phase ALUs, allowing high-speed phase modulation. The 12-bit value is latched into the Phase ALUs by means of the **PHLD** input. The data on the $\mathbf{ADDR_{3-0}}$ lines is mapped onto Phase Bits 3 to 0 and the data on the $\mathbf{DATA_{7-0}}$ lines are mapped onto Phase Bits 11 to 4 in this case. When using the parallel phase load mode **CSEL** and/or **WRSTB** should remain high to ensure that the phase data is not written into the phase and frequency buffer registers of the STEL-1377.

PHLD
The **Ph**ase **Loa**d input is used to control the latching of the Phase Modulation data into the Phase ALUs. The 12-bit data at the output of the Phase Modulation Control Block must be valid during the clock cycle following the falling edge of **PHLD**. The data is then transferred during the subsequent cycle. The 12-bit phase data is added to the 12 most significant bits of the accumulator output, so that the MSB of the phase data represents a 180° phase change. The source of this data will be determined by the state of **PHSEL**. The phase of the NCO output will change 12 clock cycles after the **PHLD** command, due to pipelining delays.

$\mathbf{FMOD_{15}}$ through $\mathbf{FMOD_0}$
The **F**requency **Mod**ulation bus is a 16-bit bus on which the FM data is loaded into the STEL-1177. The data should be a 16-bit unsigned number.

FMSUB
The **FM Sub**tract input controls the Add/Subtract operation of the Δ-Phase ALU. When it is high the FM data on the $\mathbf{FMOD_{15-0}}$ bus will be subtracted from the carrier frequency, and when it is low the FM data will be added to the carrier frequency. In this way the FM data can be treated as a 17-bit signed-magnitude number, where the **FMSUB** signal is the sign bit.

$\mathbf{FMADDR_1}$ through $\mathbf{FMADDR_0}$
The two inputs $\mathbf{FMADDR_{1-0}}$ set the deviation of the frequency modulation by controlling the significance of the FM data in relation to the carrier frequency data. The FM data word will be multiplied by 2^0, 2^4, 2^8, or 2^{12} according to the state of $\mathbf{FMADDR_{1-0}}$, and the consequent resolution and maximum values of the deviation are shown in the table below. The deviations and resolutions shown are for a clock frequency of 60 MHz.

FM-ADDR$_1$	**FM-ADDR$_0$**	Mult. factor of FM data	Maximum deviation	Resol-ution
0	0	2^0	± 915 Hz	14 mHz
0	1	2^4	± 14.6 KHz	0.22 Hz
1	0	2^8	± 234 KHz	3.6 Hz
1	1	2^{12}	± 3.75 MHz	57 Hz

FMLD
The **FM Loa**d input controls the writing of the frequency modulation data on the $\mathbf{FMOD_{15-0}}$ bus and the **FMSUB** input into the device. When $\mathbf{RATE_{1-0}} = 00$ the data at the output of the Frequency Modulation Control Block must be valid during the clock cycle following the falling edge of **FMLD**. The data is then transferred during the subsequent cycle. When $\mathbf{RATE_{1-0}} = 01$, 10 or 11 are selected the FM data will be loaded automatically without the use of the **FMLD** input. Note that **FMLD** must be held low during automatic operation, otherwise the loading will be inhibited.

SIMLD
The **Sim**ultaneous **Loa**d input allows the carrier frequency data from the Mux Block and the FM data to be updated simultaneously. When **SIMLD** is low, only the FM data will be updated after a falling edge on **FMLD**. When this input is high, both the FM data and carrier frequency data will be updated simultaneously. When **SIMLD** is low at least four clock cycles are required between falling edges of **FMLD** and **FRLD** to ensure glitch-free changes in the outputs.

$RATE_{1-0}$
The $RATE_{1-0}$ signals control the rate at which the FM data on the $FMOD_{15-0}$ bus is added to or subtracted from the carrier frequency, as shown in the table below:

$RATE_1$	$RATE_0$	Modulation Update Rate
0	0	Manual, with **FMLD** signal
0	1	Every 4th clock cycle
1	0	Every 8th clock cycle
1	1	Every 16th clock cycle

CIN
The **C**arry **In**put is an arithmetic carry to the least significant bit of the Accumulator. Normal operation of the NCO requires that **CIN** be set at a logic 0. When **CIN** is set at a logic 1 the effective value of the Δ-Phase register is increased by one. This allows the resolution of the accumulator to be expanded for higher frequency resolution.

OUTPUT SIGNALS

OUT (SIN) AND OUT (COS)
The signals appearing on the **OUT** pins are the analog outputs of the DACs. They are stepped sinewaves, where the number of steps in each cycle of the output is equal to the ratio of the clock frequency to the output frequency. When this number is not an integer the steps will not repeat from one cycle to the next, but the fundamental component of the output signal will always be a sinewave at the desired frequency. There will be a DC offset on the output signal. The outputs can be capacitively coupled if operation down to very low frequencies is not required, otherwise offset compensation should be provided externally.

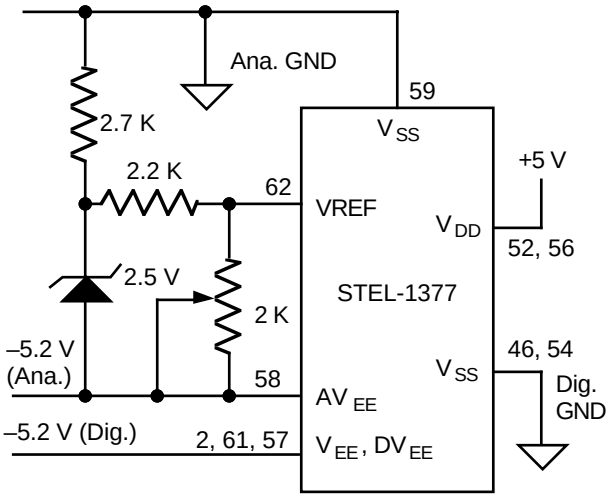
FMSYNC
The FM Sync output indicates the instant in time when the FM data on the FMOD bus is written into the device. The **FMSYNC** output is normally high and goes low for one clock cycle at a frequency depending on the state of the $RATE_{1-0}$ inputs. In the automatic modulation modes ($RATE_{1-0} \neq 00$) the data on the $FMOD_{15-0}$ bus will be written into the FM Buffer Register on the rising edge of the clock following the falling edge of **FMSYNC**. This signal can be used to synchronize the updating of the FM data externally.

APPLICATIONS INFORMATION

Since the STEL-1377 combines high-speed digital and analog circuits, care must be taken to minimize the effects of noise from the digital circuit on the analog output. The following precautions will help in this area:

1. Use ground and power planes on the printed circuit board. Separate analog and digital ground planes will also help.
2. Decouple the DV_{EE} (DAC) and AV_{EE} (DAC) line from the V_{EE} supply with 0.3 to 1 µH inductors.
3. Decouple all the power supply pins and the VREF pin to the appropriate ground plane with 1000 pF and 0.1 µF ceramic capacitors mounted as closely as possible to the pins.

The clock input can be either a sine wave or a square wave, the input buffer will square up a sinusoidal input. The input is capacitively coupled internally. An ECL level signal or a sine wave at about –5 to +5 dBm (50 Ω) is recommended. The bias circuit shown can be used to generate a stable VREF. If high stability, which translates directly into output level stability, is not a requirement a much simpler circuit can be realized by replacing the 2.7KΩ and 2.2KΩ resistors and the reference diode with a single 8.2KΩ resistor from VREF to the analog ground. The output level can be varied by adjusting the bias voltage with the 2KΩ pot in either case.



Recommended bias circuit for VREF

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–65 to +150	°C
T_a	Operating Temperature	–40 to +85	°C
V_{DDmax}	Max. voltage between V_{CC} and V_{SS}	+7 to –0.7	volts
V_{EEmax}	Max. voltage between V_{EE} and V_{SS}	–7 to +0.7	volts
$V_{I/O(max)}$	Max. voltage on any input pin	V_{DD}+0.7	volts
$V_{I/O(min)}$	Min. voltage on any input pin	V_{SS}–0.7	volts

RECOMMENDED OPERATING CONDITIONS (The V_{SS} pins should be connected to ground)

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage, +5 volts	+5 ± 10%	volts
V_{EE}	Supply Voltage, –5.2 volts	–5.2 ± 10%	volts
T_a	Operating Temperature (Ambient)	0 to +70	°C

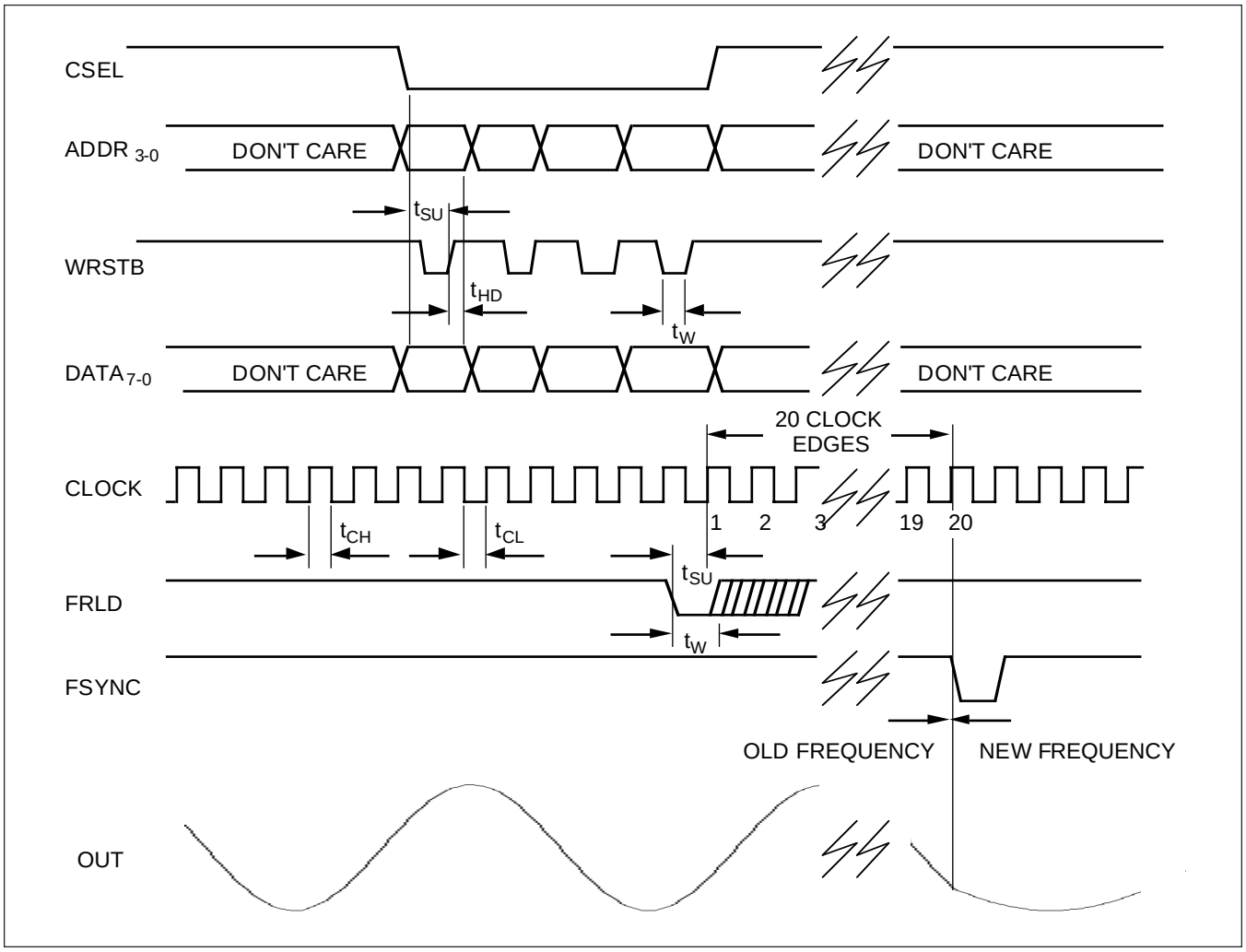
D.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 V ±5%, V_{EE} = –5.2 V ±5%, T_a = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{DD}	Supply Current, +5 volts		700		mA	@ 60 MHz clock (/Q)
I_{EE}	Supply Current, –5.2 volts		950		mA	@ 60 MHz clock (/Q)
$V_{IH(min)}$	Min. High Level Input Voltage	2.0			volts	Guaranteed Logic '1'
$V_{IL(max)}$	Max. Low Level Input Voltage			0.8	volts	Guaranteed Logic '0'
$I_{IH(max)}$	Max. High Level Input Current			10	µA	V_{IN} = +5.0 volts
$I_{IL(max)}$	Max. Low Level Input Current			–10	µA	V_{IN} = 0 volts
V_{CLK}	Clock Input Voltage	0.4		1.0	volts	peak to peak

OUTPUT CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$P_{O(max)}$	Max. Output Power	–5			dBm	
TC_{FS}	Full-scale output Temp. coefficient		0.06	0.12	%	50 Ω load
GE	Output glitch energy		15		pV.sec.	
$Err_{(i)}$	Output integral linearity	–0.1		+0.1	%	of full-scale output
V_{SPUR}	Spurious signal level		–65		dBc	$f_{OUT} < .25 \times f_{CLK}$
V_{SPUR}	Spurious signal level		–62		dBc	$.25 \times f_{CLK} < f_{OUT} < .33 \times f_{CLK}$
V_{SPUR}	Spurious signal level		–60		dBc	$.33 \times f_{CLK} < f_{OUT} < .45 \times f_{CLK}$

DDS FREQUENCY CHANGE SEQUENCE

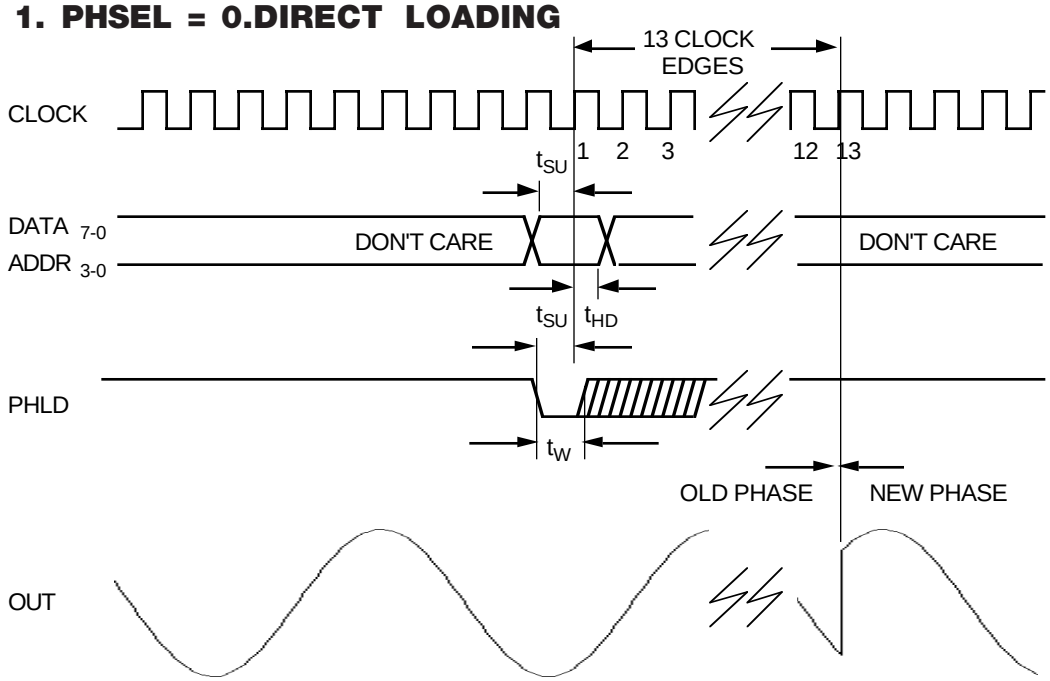


A.C. CHARACTERISTICS (Operating Conditions: V_{DD}=5.0 V ±5%, V_{EE}=–5.2 V ±5%, T_a=25°C)

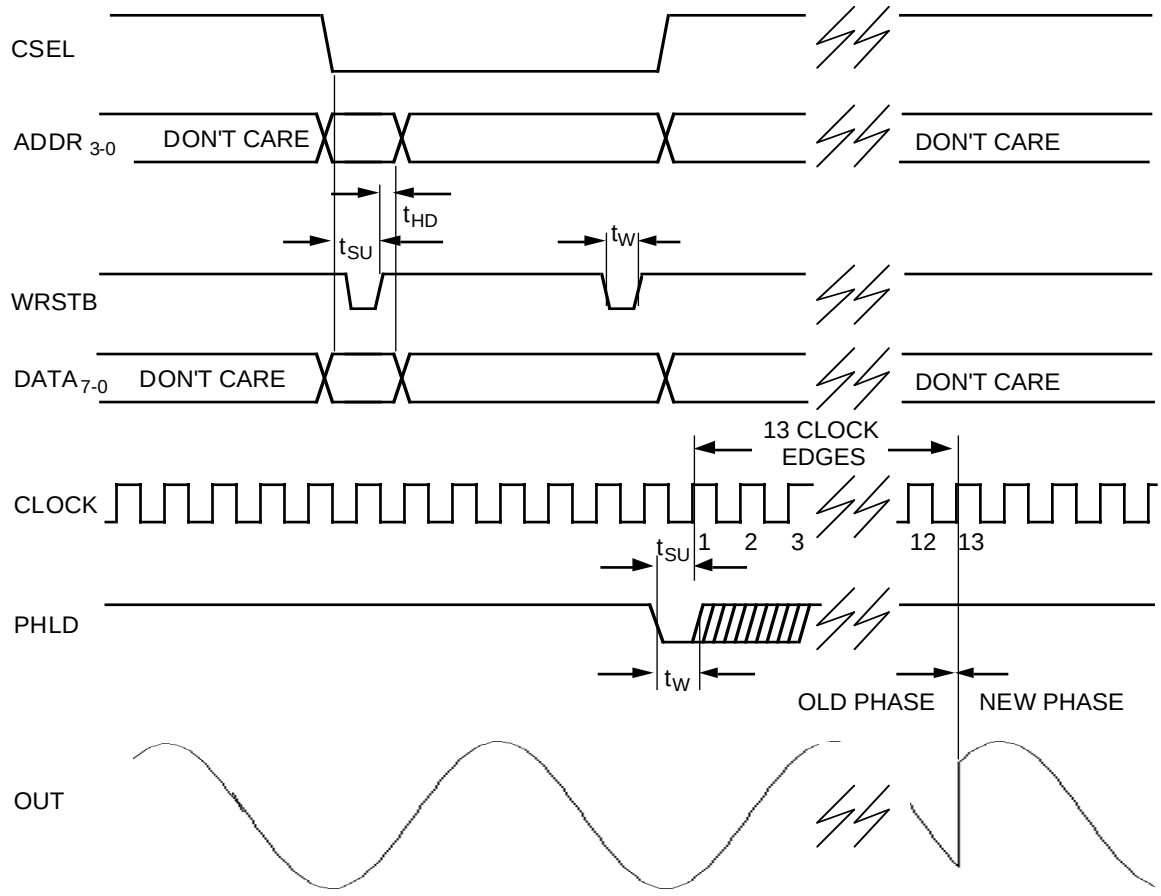
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{RS}	Reset Pulse Width	20			nsec.	
t_{SU}	**DATA**, **ADDR** or **CSEL** to **WRSTB** or **PHLD** Setup and **FRLD**, **PHLD**, **FMLD** or **FMOD** to **CLOCK** Setup	5			nsec.	
t_{HD}	**DATA**, **ADDR** or **CSEL** to **WRSTB** or **PHLD** Setup and **FRLD**, **PHLD**, **FMLD** or **FMOD** to **CLOCK** Hold	5			nsec.	
t_{CH}	**CLOCK** high	5			nsec.	f_{CLK}= 60 MHz
t_{CL}	**CLOCK** low	5			nsec.	f_{CLK}= 60 MHz
t_W	**WRSTB**, **FRLD**, **PHLD** or **FMLD** pulse width	5			nsec.	

DDS PHASE CHANGE SEQUENCE

1. PHSEL = 0.DIRECT LOADING

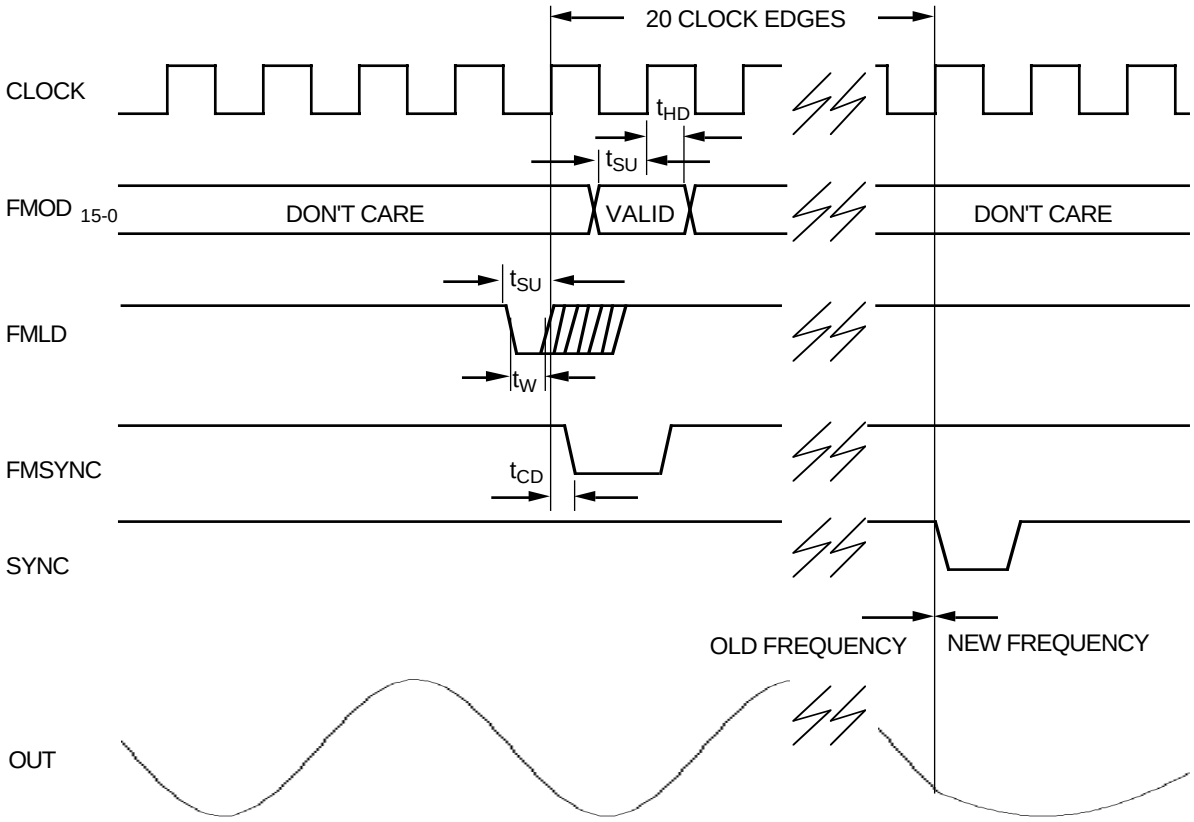


2. PHSEL = 1.BUS LOADING

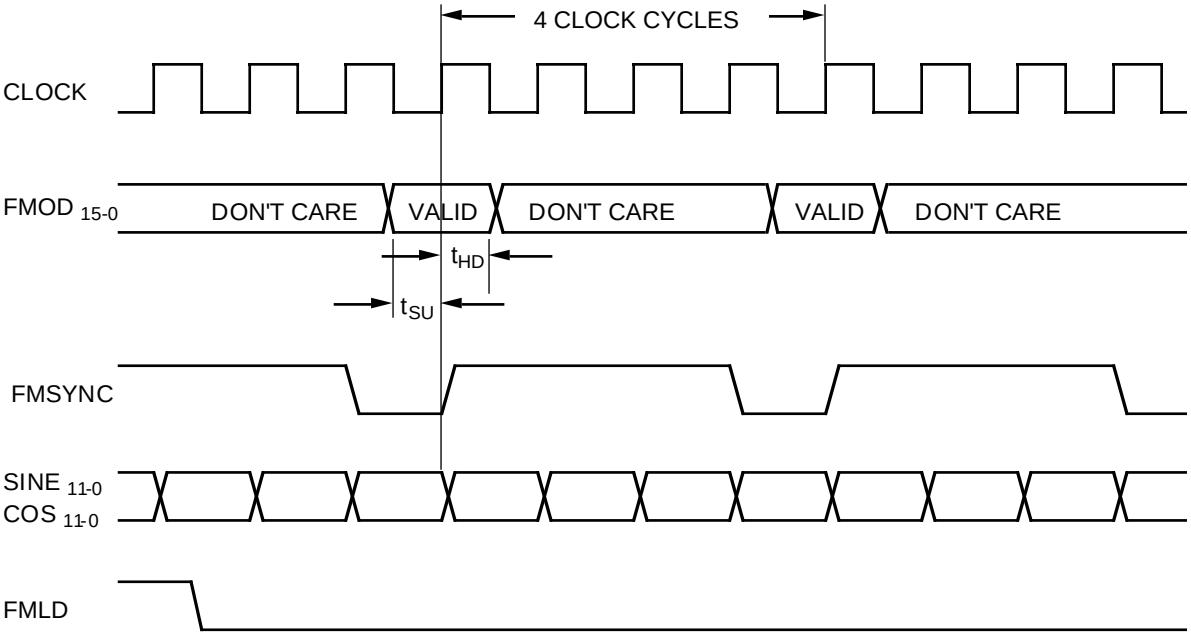


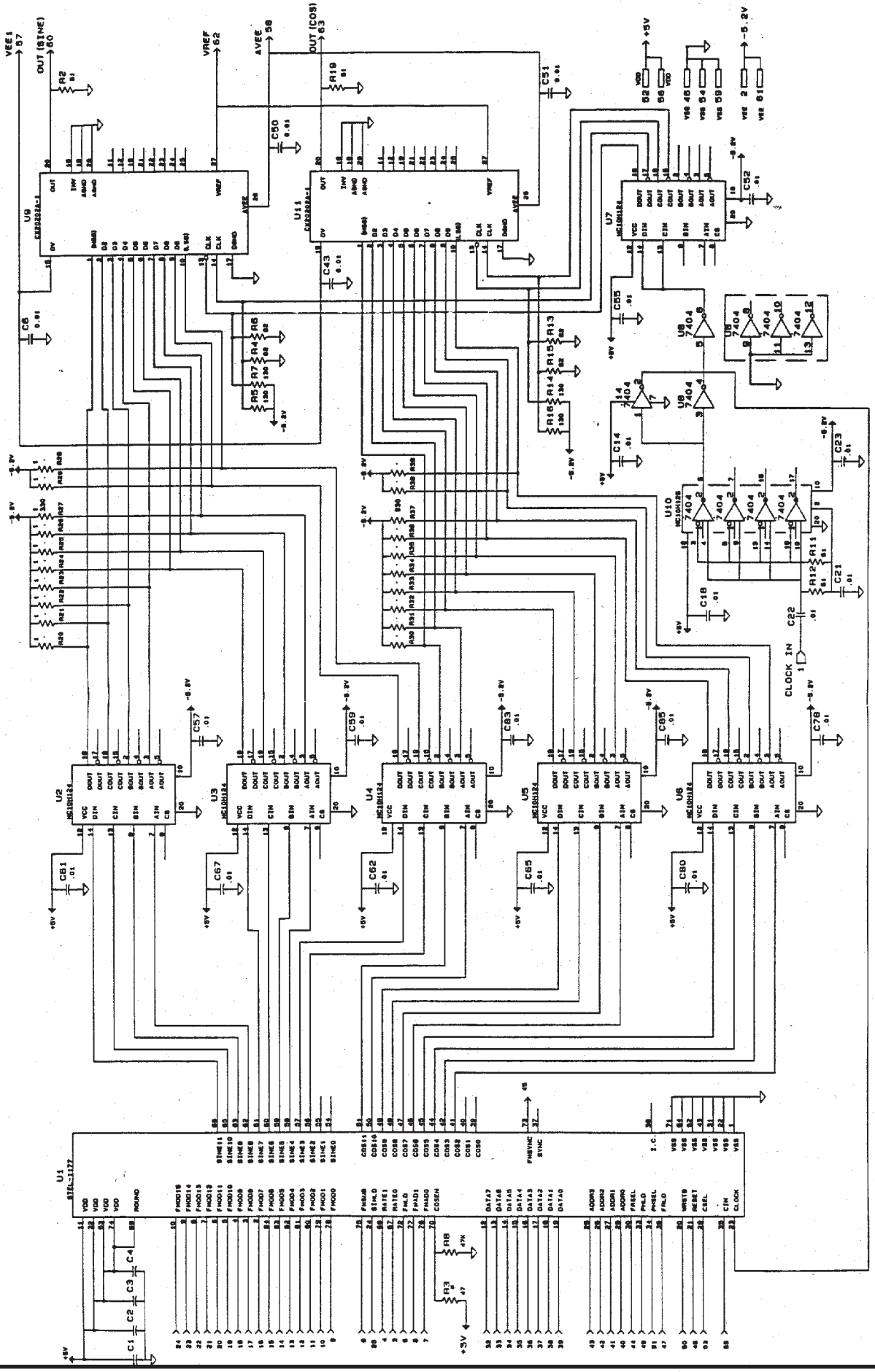
NCO FREQUENCY MODULATION SEQUENCE

1. RATE = 00.MANUAL LOADING



2. RATE ≠ 00.AUTOMATIC LOADING (RATE = 01 shown)





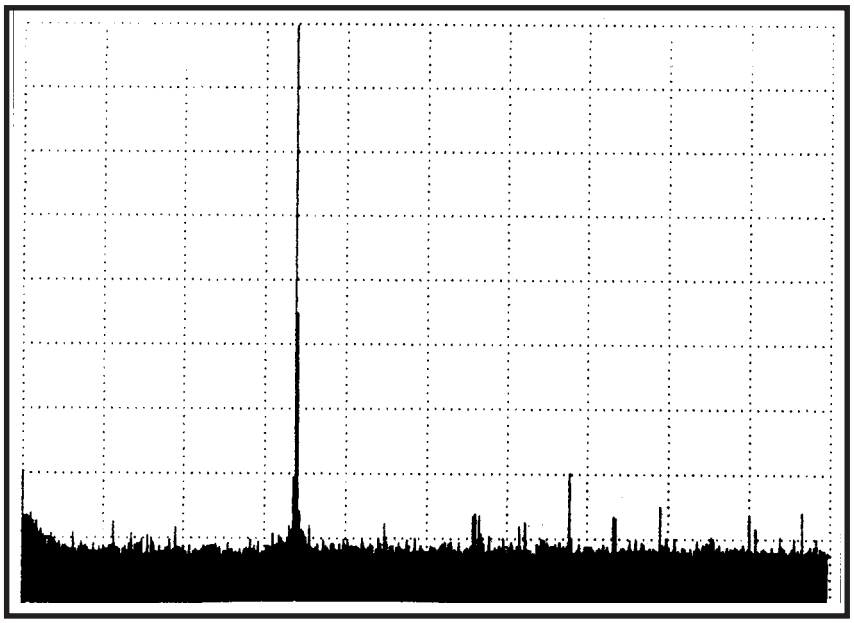
SPECTRAL PURITY

When an NCO is used with a digital to analog converter (DAC) to generate an analog waveform the spectral purity of the synthesized waveform is a function of many variables, including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC. The sine signals generated by the STEL-1177 have 12 bits of amplitude resolution and 13 bits of phase resolution which results in spurious levels which are theoretically at least 75 dB down. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency f_o of the NCO approaches $f_c/2$, the "image" spur at $f_c - f_o$ (created by the sampling process) also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this image spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

A spectral plot of the NCO output after conversion with a DAC (Sony CX20202A-1) is shown below. In this case, the clock frequency is 60 MHz and the output frequency is programmed to 6.789 MHz. The maximum non-harmonic spur level observed over the output frequency range shown in this case is –70 dBc. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the frequency $f_c - 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. The same phenomenon occurs with the third harmonic when the frequency crosses through $f_c/4$.

TYPICAL SPECTRUM

Center Frequency:	10.0 MHz
Frequency Span:	20.0 MHz
Reference Level:	–5 dBm
Resolution Bandwidth:	1 KHz
Scale:	Log, 10 dB/div
Output frequency:	6.789 MHz
Clock frequency:	60 MHz



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