NEC
μPD2118
μPD2118-2
μPD2118-3
PRELIMINARY

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

3

DESCRIPTION

The μPD2118 is a single +5V power supply, 16384 word by 1 bit Dynamic MOS RAM. The μPD2118 achieves high speed with low power dissipation by the use of single transistor dynamic storage cell design and advanced dynamic circuitry. This circuit design results in the minimizing of current transients typical of dynamic RAMS. This in turn results in high noise immunity of the μPD2118 in a system environment. By using a multiplexing technique, the μPD2118 can be packaged in an industry standard 16-Pin Dip utilizing 7 address input pins for the 14 address bits required. The two 7 bit address words are referred to as the ROW and COLUMN address. Two TTL clocks, ROW address strobe ($\overline{RAS}$) and COLUMN address strobe ($\overline{CAS}$) latch these two words into the μPD2118. Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ permit high systems performance without placing difficult constraints upon the multiplexing control circuitry.

The μPD2118 has a three-state output controlled by $\overline{CAS}$, independent of $\overline{RAS}$. Following a valid read or read-modify-write cycle, data will be held in the output by holding $\overline{CAS}$ low. Returning $\overline{CAS}$ to a high state will result in the data out pin reverting to the high impedance mode. Use of this $\overline{CAS}$ controlled output means that the μPD2118 can perform hidden refresh by holding $\overline{CAS}$ low to maintain latch data output while using $\overline{RAS}$ to execute $\overline{RAS}$-only-refresh cycles.

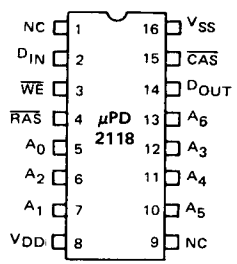
The use of single transistor storage cell circuitry requires that data be periodically refreshed. Refreshing can be accomplished by performing $\overline{RAS}$-only-refresh cycles, hidden refresh cycles or normal read or write cycles on each of the 128 address combinations of A0 through A6 during a 2 ms period. The write cycle will refresh stored data on all bits of the selected row, except that the bit which is addressed will be modified to reflect the data input.

FEATURES

- Single +5V Supply, ±10% Tolerance
- Low Power: 138 mW Max Operating
  16 mW Max Standby
- Low VDD Current Transients
- All Inputs, Including Clocks, TTL Compatible
- Non-Latched Output is Three-State
- $\overline{RAS}$-Only-Refresh
- 128 Refresh Cycles Required
- Page Mode Capability
- $\overline{CAS}$ Controlled Output Allows Hidden Refresh

P/N	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD2118	150 ns	320 ns	410 ns
μPD2118-2	120 ns	270 ns	345 ns
μPD2118-3	100 ns	235 ns	295 ns

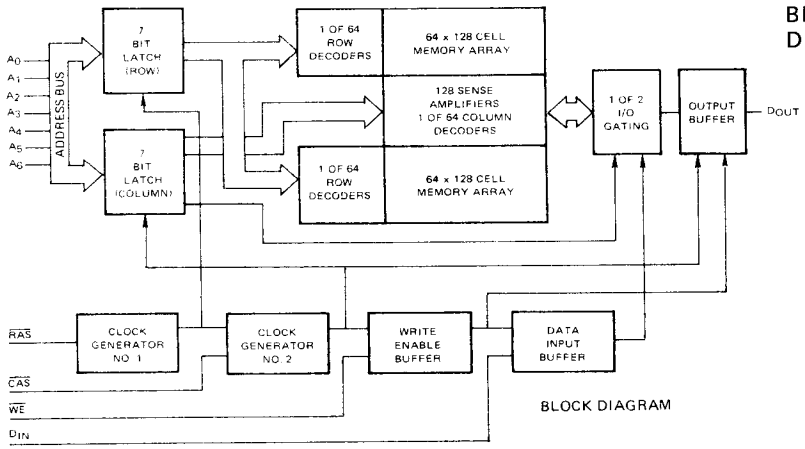
PIN CONFIGURATION



PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
$\overline{RAS}$	ROW ADDRESS STROBE
V_{DD}	POWER (+5V)
V_{SS}	GROUND

BLOCK DIAGRAM



BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin Relative to VSS	−2.0 to +7.5V
Data Out Current	50 mA
Power Dissipation	1.0W

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS READ, WRITE, AND READ MODIFY WRITE CYCLES ①

T_a = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER		SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS	NOTES
Input Load Current		I_{LI}		10	μA	V_{IN} = V_{SS} to V_{DD}	
Output Leakage Current for High Impedance State		I_{LO}		10	μA	Chip Deselected $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
V_{DD} Supply Current (Standby)		I_{DD1}		3	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	
V_{DD} Supply Current (Operating)	μPD2118-3	I_{DD2}		25	mA	TRC = TRC Min	②
	μPD2118-2	I_{DD2}		22	mA		
	μPD2118-0	I_{DD2}		22	mA		
V_{DD} Supply Current (RAS-Only Cycle)	μPD2118-3	I_{DD3}		20	mA		
	μPD2118-2	I_{DD3}		18	mA		②
	μPD2118-0	I_{DD3}		18	mA	TRC = TRC Min	
V_{DD} Supply Current Page Mode, Maximum t_{PC} Minimum t_{CAS}	μPD2118-3	I_{DD4}		20	mA		
	μPD2118-2	I_{DD4}		17	mA		②
	μPD2118-0	I_{DD4}		15	mA		
V_{DD} Supply Current (Standby, Output Enabled)		I_{DD5}		4	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	②
Input Low Voltage		V_{IL}	−2.0	0.8	V		
Input High Voltage		V_{IH}	2.4	7.0	V		
Output Low Voltage		V_{OL}		0.4	V	I_{OL} = 4.2 mA	
Output High Voltage		V_{OH}	2.4			I_{OH} = −5 mA	

Notes: ① All voltages referenced to V_{SS}.

② I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} Max is measured with the output open.

CAPACITANCE ①

T_a = 25°C, VDD = 5V ± 10%, VSS = 0V, unless otherwise noted.

SYMBOL	PARAMETER	TYP	MAX	UNIT
CI1	Address, Data In	3	5	pF
CI2	$\overline{RAS}$, $\overline{WE}$	4	7	pF
CI3	$\overline{CAS}$	6	10	pF
C0	Data Out	4	7	pF

NOTES: ① Capacitance measured with Boonton meter or effective capacitance calculated from the Equation $C = I\Delta T/\Delta V$ with ΔV equal to 3V and power supplies at nominal levels.

AC CHARACTERISTICS①②③*

T_a = 0°C to 70°C; V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

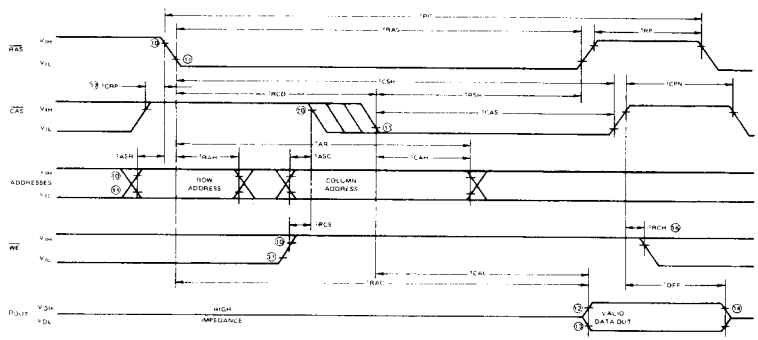
READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

SYMBOL	PARAMETER	μPD2118-3		μPD2118-2		μPD2118-0		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RAC}	Access Time From $\overline{RAS}$		100		120		150	ns	④ ⑤
t_{CAC}	Access Time From $\overline{CAS}$		50		65		80	ns	④ ⑤ ⑥
t_{REF}	Time Between Refresh		2		2		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	110		120		135		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time (non-page-mode cycles)	50		55		70		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	55	25	70	ns	⑦
t_{RSH}	$\overline{RAS}$ Hold Time	65		85		105		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	110		135		165		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	Column Address Hold Time	15		15		20		ns	
t_{AR}	Column Address Hold Time, to $\overline{RAS}$	65		70		90		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	⑧
t_{OFF}	Output Buffer Turn Off Delay	0	45	0	50	0	60	ns	
	READ AND REFRESH CYCLES								
t_{RC}	Random Read Cycle Time	235		270		320		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	115	10,000	140	10,000	175	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	80	10,000	95	10,000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
	WRITE CYCLE								
t_{RC}	Random Write Cycle Time	235		270		320		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	115	10,000	140	10,000	175	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	80	10,000	95	10,000	ns	
t_{WCS}	Write Command Set-Up Time	0		0		0		ns	⑨
t_{WCH}	Write Command Hold Time	30		35		45		ns	
t_{WCR}	Write Command Hold Time, to $\overline{RAS}$	80		90		115		ns	
t_{WP}	Write Command Pulse Width	35		40		50		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	70		90		110		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	65		85		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	
t_{DH}	Data-In Hold Time	30		35		45		ns	
t_{DHR}	Data-In Hold Time, to $\overline{RAS}$	80		90		115		ns	
	READ-MODIFY-WRITE CYCLE								
t_{RWC}	Read-Modify-Write Cycle Time	295		345		410		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	175	10,000	215	10,000	265	10,000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	120	10,000	155	10,000	185	10,000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		150		ns	⑨
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	50		65		80		ns	⑨
	PAGE MODE CYCLE								
t_{PC}	Page Mode Read or Write Cycle	130		160		190		ns	
t_{PCM}	Page Mode Read-Modify-Write	190		235		280		ns	
t_{CP}	$\overline{CAS}$ Precharge Time, Page Cycle	60		70		85		ns	
t_{RPM}	$\overline{RAS}$ Pulse Width, Page Mode	125	10,000	150	10,000	175	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	80	10,000	95	10,000	ns	

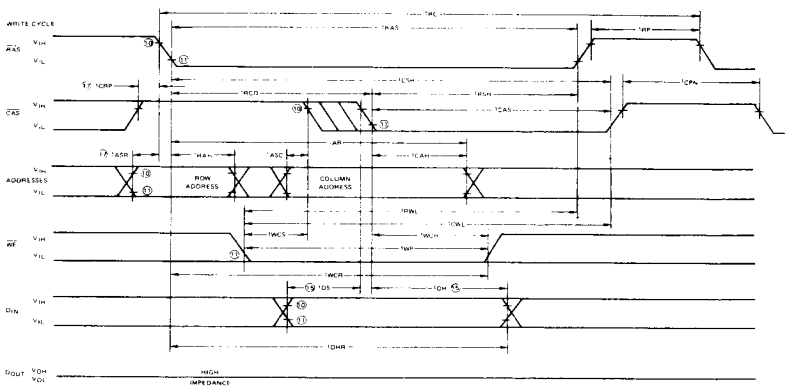
*NOTES: See page 7.

TIMING WAVEFORMS

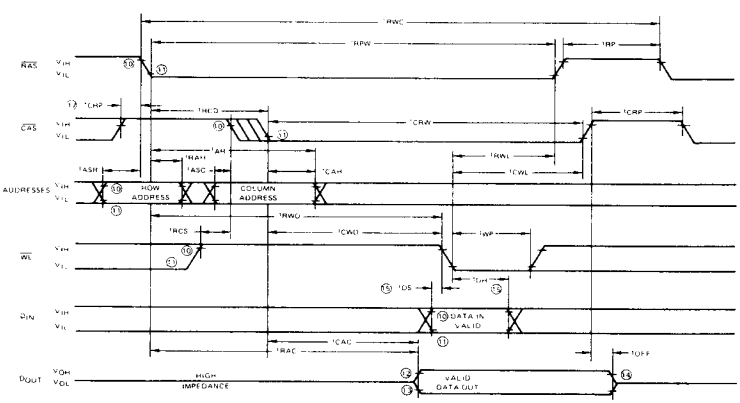
READ CYCLE



WRITE CYCLE

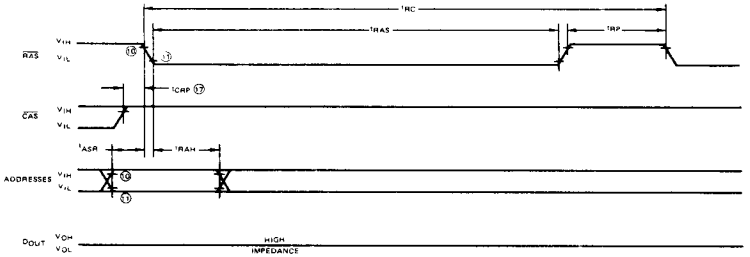


READ-MODIFY-WRITE CYCLE

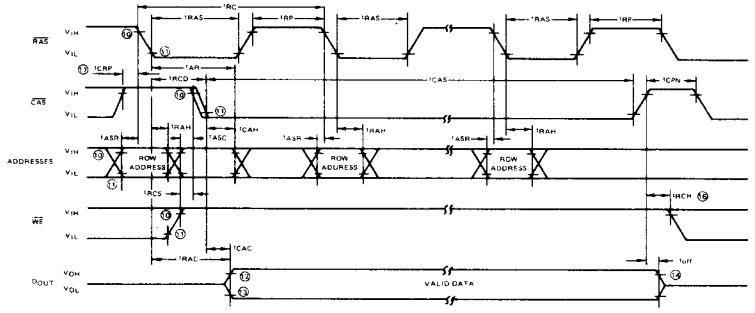


NOTES: See page 7.

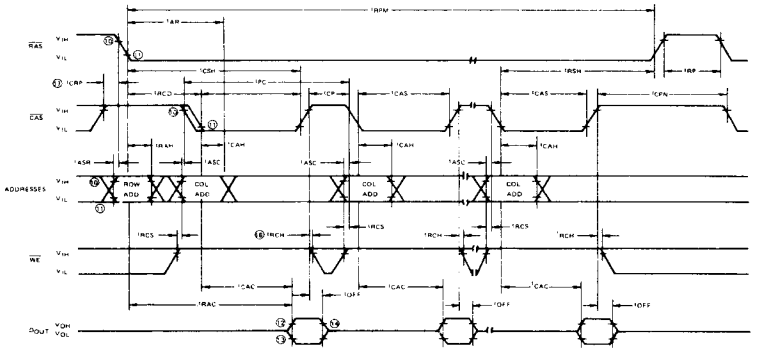
RAS-ONLY REFRESH CYCLE



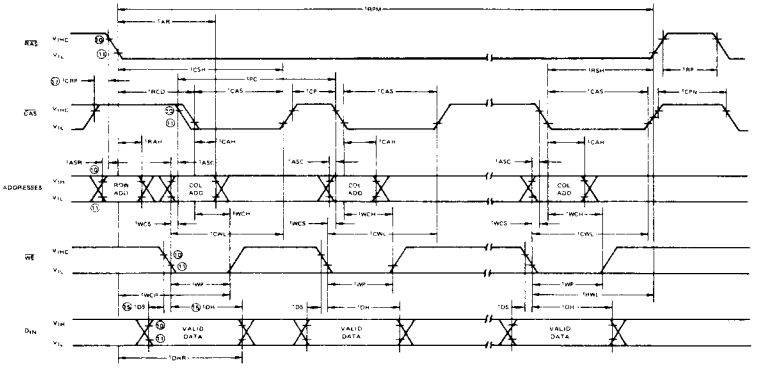
HIDDEN REFRESH CYCLE



PAGE MODE READ CYCLE

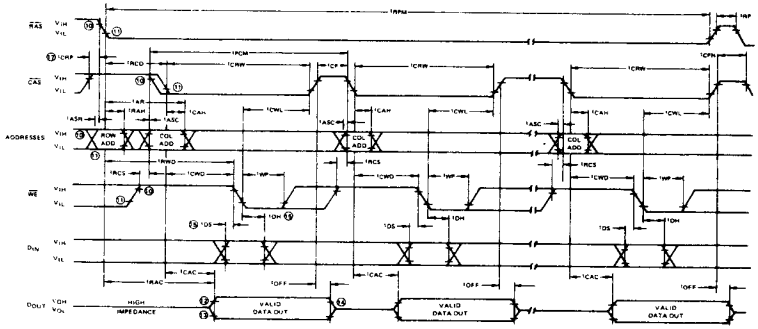


PAGE MODE WRITE CYCLE



TIMING WAVEFORMS (CONT.)

PAGE MODE READ-MODIFY-WRITE CYCLE



Notes:
① All voltages referenced to V_{SS}.
② Eight cycles are required after power-up or prolonged periods greater than 2 ms of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
③ AC Characteristics assume t_T = 5 ns.
④ Assume that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than t_{RCD} (max), then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).
⑤ Load = 2 TTL loads and 100pF.
⑥ Assumes $t_{RCD} \geq t_{RCD}$ (max).
⑦ t_{RCD} (max) is specified as a reference point only: if t_{RCD} is less than t_{RCD} (max) access time is t_{RAC}. If t_{RCD} is greater than t_{RCD} (max) access time is $t_{RCD} + t_{CAC}$.
⑧ t_T is measured between V_{IH} (min) and V_{IL} (max).
⑨ If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
⑩⑪ V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals.
⑫⑬ V_{OH} min and V_{OL} max are reference levels for measuring timing of D_{OUT}.
⑭ t_{OFF} is measured to $|I_{OUT}| < |I_{LO}|$.
⑮ t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
⑯ t_{RCH} is referenced to the trailing edge of $\overline{CAS}$ or $\overline{RAS}$, whichever occurs first.
⑰ t_{CRP} requirements is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a CAS-only cycle (i.e., for systems where CAS has not been decoded with RAS).

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}/\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time. Device access time, t_{ACC}, is the longer of the two calculated intervals $t_{ACC} = t_{RAC}$ or $t_{ACC} = t_{RCD} + t_{CAC}$.

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe delay time, t_{RCD}, are system dependent timing parameters. For example, substituting the device parameters of the μPD2118-3 yields $t_{ACC} = t_{RAC} = 100$ nsec for 20 nsec $\leq t_{RCD} \leq 50$ nsec, but $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 50$ for $t_{RCD} > 50$ nsec.

Note that if 20 nsec $\leq t_{RCD} \leq 50$ nsec device access time is determined by the first equation and is equal to t_{RAC}. If $t_{RCD} > 50$ nsec, access time is determined by the second equation. This 30 nsec interval (shown in the t_{RCD} inequality in the first equation) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$.

REFRESH CYCLES

Each of the 128 rows of the μPD2118 must be refreshed every 2 milliseconds to maintain data. Any memory cycle (read, write, or $\overline{RAS}$ only) refreshes the selected row as defined by the low order ($\overline{RAS}$) addresses. Any Write cycle, of course, may change the state of the selected cell. Using a Read, Write, or Read-Modify-Write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the D_{OUT} in the high impedance state with a typical power reduction of 20% over a Read or Write cycle.

$\overline{RAS}$/$\overline{CAS}$ TIMING

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle once begun by bringing $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle can not begin until the minimum precharge time, t_{RP}, has been met.

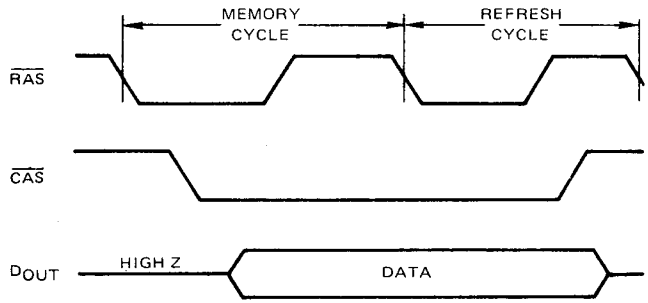
DATA OUTPUT OPERATION

Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}) the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Type of Cycle	D_{OUT} State
Read Cycle	Data From Addressed Memory Cell
Early Write Cycle	HI-Z
$\overline{RAS}$-Only Refresh Cycle	HI-Z
$\overline{CAS}$-Only Cycle	HI-Z
Read/Modify/Write Cycle	Data From Addressed Memory Cell
Delayed Write Cycle	Indeterminate

HIDDEN REFRESH

A feature of the μPD2118 is that refresh cycles may be performed while maintaining valid data at the output pin. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}) executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

POWER ON

The μPD2118 requires no power on sequence. After the application of the V_{DD} supply, or after extended periods of bias (greater than 2 ms) without clocks, the device must perform a minimum of eight (8) initialization cycles (any combination of cycles containing a $\overline{RAC}$ clock such as $\overline{RAS}$-only refresh) prior to normal operation.

The V_{DD} current (I_{DD}) requirement of the μPD2118 during power on is, however, dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If the input levels of these clocks are at V_{IH} or V_{DD}, whichever is lower, the I_{DD} requirement per device is I_{DD1} (I_{DD} standby). If the input levels for the two clocks are lower than V_{IH} or V_{DD}, the I_{DD} requirement will be greater than I_{DD1}. For large systems, this current requirement for I_{DD} could be substantially more than that for which the system has been designed. A system which has been designed assuming the majority of devices to be operating in the refresh/standby mode may produce sufficient I_{DD} loading such that the power supply might current limit. To assure that the system will not experience such loading during power on, a pullup resistor for each clock input to V_{DD} to maintain the non-selected current level (I_{DD1}) for the power supply is recommended.

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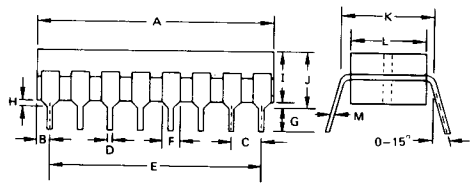
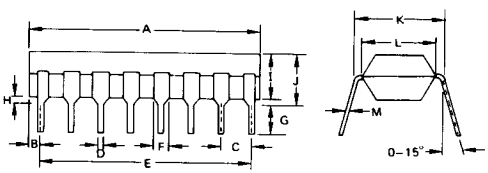
PACKAGE OUTLINE μPD2118D



Cerdip

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

μPD2118C



Plastic

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

2118DS-12-80-CAT