

FEATURES

“Right Sized” Transport of 10GE-LAN signals through OTN Network

- Two different flow-control options used on client to allow for 10GE-LAN signal to be packed into OTU-2.
- Proprietary 10GE-LAN map to OTU-2 without transport rate increase or client flow control.

Superb I/O flexibility with industry standard SFI4P1 support on both line and client ports of device.

- Proven CMOS I/O from AMCC.
- Provides up to 705Mbps per I/O, covering 11.1GHz operation for full bandwidth 10GE-LAN client in an OTUk formatted signal and 11.27GHz operation for 10G Fibre Channel client in an OTUk formatted signal.
- Provides port swapping and output dual feed features for 1 + 1 line protection scheme.

Integrated Patented Dispersion Compensation Control Circuitry for Client and Line interfaces (second generation of AMCC’s DispersionXX solution)

- Proven in AMCC’s DispersionXX solution (NIAGARA and S3094).
- Available with the use of the S3394.
- Available on both client and line interfaces of Rubicon.
- Best-in-class optical fidelity solution providing longest reach without regeneration.

Easy software migration from industry leading AMCC NIAGARA FEC device

- Significant reuse of the Niagara register map in Rubicon.
- Minimal effort and maximum benefit upgrade path from original DispersionXX (NIAGARA and S3094) solution.

G.709 ODU-2 Synchronous and Asynchronous mapping

- 1 x OC192/STM-64 mapping (239,237) per G.709.
- Direct map (239,238) into ODU – 2.

G.709 ODU-1 Synchronous and Asynchronous mapping

- 1 x OC48/STM-16 mapping (239,238) per G.709.
- Direct map (239,238) into ODU-1.

G.709 Overhead processing

- Bi-directional add-drop ODU-1, ODU-2.
- Bi-direction G.709 Overhead Processing and optional OTU2 Fixed Stuff Columns access.
- Dedicated GCC ports.

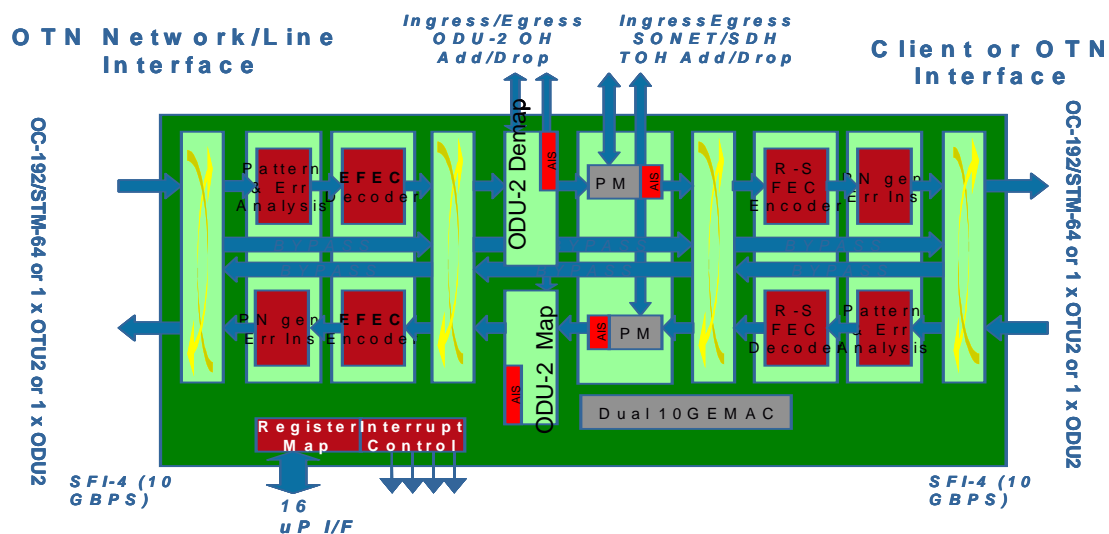
Ingress and Egress Client Data Performance Monitoring

- 1 x OC192/48/12/3 TOH add-drop and processing.
- 8B/10B Monitoring.
- 10GE Monitoring.
- SONET/SDH section and line termination.
- TOH add-drop port.
- LOS, OOF, LOF detection.
- B1, B2 monitoring with programmable Signal Degrade and Signal Fail thresholds.
- J0 Monitoring, SDH and SONET modes.
- K1, K2 monitoring for APS changes, line AIS and line RDI.
- Automatic, interrupt-driven, or manual AIS insertion.
- Frame boundary output.

Industry Standard RS(255,239) Forward Error Correction with 6.2 dB Coding Gain (at 10⁻¹⁵ CER)

- G.709 Compliant Frame Structure.
- Compatible with AMCC’s S19203 (HUDSON) and S19208 (NIAGARA).

Figure 1: Block Diagram



FINAL/Production Release Information - The information contained in this document is about a product that has been fully tested, characterized, and is produced released. All features described herein are supported. Contact AMCC for updates to this document and the latest product status.

Enhanced Gain Forward Error Correction with G.709 ODU

- 10.71, 10.66, 11.1, 11.27Gbps enhanced FEC with >8dB coding gain.
- G.709 overhead processing and nominal rate expansion.
- Comprehensive channel statistics gathering.
- Corrected bits, bytes.
- Corrected zeros, ones (with outputs).
- Uncorrectable sub-frame count.

Broad Interface Compatibility

- 16-bit 622 Mbps LVDS interface (MSA compliant) 10 Gbps interface.
- Compatible with AMCC HUDSON, GANGES, KHATANGA, COLUMBIA, MAROS, MEKONG, NIAGARA, S3091/92, S3097/98, S19235, S3394 and S3485.

Client and Line side loopback

- Client side and line side loopback on the Rubicon.

Support For System Test and Diagnostics

- Can synthesize SONET frame.
- Error injection capability for verification of remote error reporting.
- Test-set compliant pseudo-random sequence generation/analysis.

General Purpose Processor Interface

- Glueless 16-bit interface to MPC860, 25 MHz to 66 MHz.
- Dual mode interface also supports Intel processors.
- Interrupt driven or Polled mode operation.

Additional Protocol Support

- FEC Frame Synchronous scrambling.
- Programmable sequence detection.

Pin Compatibility to NIAGARA device**Low Power .13 u CMOS Technology**

- 1.2 Volt core operation.
- 2.5 Volt I/O.

APPLICATIONS

- SONET/SDH OC48/STM-16 OC192/STM-64 DWDM transport systems and DWDM metro networks.
- Transparent Add-Drop Multiplexing Transponder applications.
- Protocol Transparent Transport.
- IaDI to IrDI FEC transponder chip (6.2dB gain network to >8dB gain network).

GENERAL DESCRIPTION

The AMCC Rubicon-LH device is a wide-area and metropolitan transport device aimed at next generation applications, required transparent mapping, and enhanced error correction capability. The device utilizes the ITU G.709 frame and overhead structures to enable deployment of full OTN compliant network elements. Rubicon-LH will support two gain rates, the standard G.975 based rate of 6.2dB (raw optical coding gain), and AMCC's proprietary EFEC code, rated at greater than 8dB (raw optical coding gain).

The Rubicon-LH device is capable of running both these gains simultaneously, providing a superb single chip transponder solution for standard gain to enhanced gain networks. Note that the Rubicon-LH will employ the same industry leading EFEC code that was used in the AMCC Niagara device, making these devices totally compatible.

DATA INTERFACES

Both the Client and Network interfaces are SFI-4 compliant. Data is transferred as 16-bit LVDS parallel data with a synchronous clock. For 10 Gbps applications, both the Client and Network interface rate can vary between 622 Mbps and 705 Mbps, for an aggregate bandwidth of 9.95 Gbps to 11.28 Gbps. The defined low end of the parallel LVDS interface is 31.25 Mbps (across 4 bits of the interface) for an aggregate bandwidth of 125 Mbps. The device supports OC192/STM-64, ITU G.709 OTU-2, ITU-G.709 ODU-2, or proprietary direct map (into ODU-2) data up to a client rate of 10.519 Gbps.

CLIENT PERFORMANCE MONITORING

A SONET/SDH performance monitor supporting OC192/48/12/3 and SDH64/16/4/1 rates is provided to perform optional-section and limited-line termination functions. TOH for the SONET signal is dropped and added. On chip processing of the critical TOH functions, such as B1, B2, J0, is provided to enable functioning as a SONET/SDH network element. The performance monitor may also be configured to provide non-intrusive monitoring while transparently passing through the received signal with no overwrite. The 10 Gbps signal and the 2.5 Gbps signal may be synchronously or asynchronously mapped into the ODU-2 and ODU-1 payloads, respectively. FEC parity check bytes are then optionally added to form the OTU-2 or OTU-1. The device can also output the OTU-2 or OTU-1 with no parity check bytes. In the receive direction, data is de-mapped from the OTU-2 or OTU-1 and control signals are provided to enable timing regeneration of the client 10 Gbps or 2.5 Gbps signal.

When operating in the ITU G.709 OTU-2/OTU-1 or ODU-2/ODU-1 mode, the SONET monitors can be bypassed. Unlike the Niagara device, the Rubicon-LH provides the capability for intrusive SONET/SDH performance monitoring inside the OTN frame. On-chip processing of the G.709 overhead is provided to enable single chip G.709 section termination. G.709 Overhead can be added or dropped as required. The remapping that is required for synchronization of asynchronous ODU-1 signals is supported.

Client-signal monitoring for 8B/10B encoded data is also provided, as well as 64B/66B monitoring for 10GE-LAN traffic. A full 10GE-LAN MAC is also included in the Rubicon-LH device to support extensive 10GE monitoring.

10GE-LAN MAPPING

The Rubicon-LH device supports 2 distinct methods to map 10GE-LAN into OTU-2 for transport. The first is the same manner as supported in the Niagara; that is, the line rate will run at 7% above the client rate with the full 10GE-LAN being mapped into an expanded OTU-2 frame. In this mode, the line rate of the Rubicon

will be 11.1GHz.

The second manner of 10GE-LAN mapping is supported in the Rubicon-LH and involves the direct mapping of the client signal into a 10.7GHz OTU-2 frame. There is no flow control to rate limit the client in this mode.

AIS SUPPORT

For applications in which the client signal is SONET or SDH, the Rubicon-LH can generate a SONET/SDH AIS on both the client ingress and the egress.

For applications in which the client signal is G.709 compliant or for OTN regenerator applications, Line Fail and un-equipped OTN AIS is supported. For OTN edge applications, the device can be provisioned to provide either a SONET/SDH AIS or a OTN Generic AIS to the client. This facilitates convergence of the SONET/SDH and OTN functions into a single network element.

ODU MAPPING

ITU compliant client mapping of SONET OC192 or SDH STM-64 into the ODU-2 signals (and the corresponding 2.5G signals into an ODU-1) is supported whereby a stuff column is added to every G.709 sub-frame resulting in an ODU rate expansion of (239/237). The chip can be configured to insert the G.709 compliant stuff - byte value or to insert user data into this column. The values assigned to the stuff bytes can be defined either from a register set on chip or from an external add-drop port. Coverage of these stuff columns in the BIP calculation or in the FEC is optional and can be enabled via software. When the no-coverage option is enabled, the BIP and parity check values are calculated as if the standard stuff values were present.

A direct map mode is supported for ODU-2 and ODU-1 with no stuff columns to enable mapping with a 239/238 rate expansion. Start-of-frame signals are provided at the input and output ports to enable synchronization to the ODU.

LOOPBACK FUNCTIONS

Near-end and far-end loopback is supported for each of the client interfaces and for the line interface. This enables line and device testing and fault isolation. Each functional block may be bypassed as required to support the application. When all blocks are bypassed, the device allows transparent pass-through of client data (assuming synchronous inputs).

Key status and alarm signals are provided to outside pins to enable rapid response to failure conditions. These include but are not limited to: LOS, OOF, LOF, B1 Errors, and FEC errors. Three interrupt pins, each with a mask register are provided to enable prioritization of interrupts and timely interaction with firmware.

In addition to the loopback capabilities of the device, the Rubicon-LH also employs a unique port swapping capability allowing the physical ports on the device to be interfaced to either side of the FEC encoders. With this capability a customer can use the EFEC core on either physical port of the device. This capability increases the flexibility of a single board design used in a variety

of modes.

FORWARD ERROR CORRECTION CAPABILITY

Two FEC options are supported on the 10 Gbps line side. The Rubicon-LH can support standard RS(255,239) FEC compliant with G.709, G.975, and compatible with the AMCC Hudson device. The device can also support an enhanced FEC algorithm that is applied using the same G.709 frame structure and data rate as used in the Hudson and Niagara devices, but providing more than 2 dB of additional coding gain (*measured at a BER of 10^{-15}). The Rubicon-LH device will operate in a mode where both encoders and decoders are working simultaneously, allowing for a single chip transponder to operate between two networks with different gain characteristics.

LEGACY COMPATIBILITY

As indicated above, the Rubicon-LH also supports operation in the G.975 mode. In this mode, the G.709 overhead processing can be inhibited and direct access to the non-framing bytes in the overhead column is provided through the pins on the device. The device can should be configured to operate in the 255,238 mapping mode with no stuff columns inserted in the FEC payload.

FOOTPRINT COMPATIBILITY

In addition to the significant reuse of the Niagara register map in the Rubicon, the Rubicon will also be pin compatible with the Niagara device. Although the core power balls will be driven to a lower voltage (1.2V versus 1.8V), with careful board design considerations, the customer will be able to realize the Rubicon-LH device in sockets designed for the Niagara chip. This capability will allow the customer to use a more feature rich and lower power dissipation device in the target socket.

CONTROL INTERFACE

A general purpose 16-bit microprocessor interface is provided for control and monitoring. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either interrupt driven or polled-mode configurations.

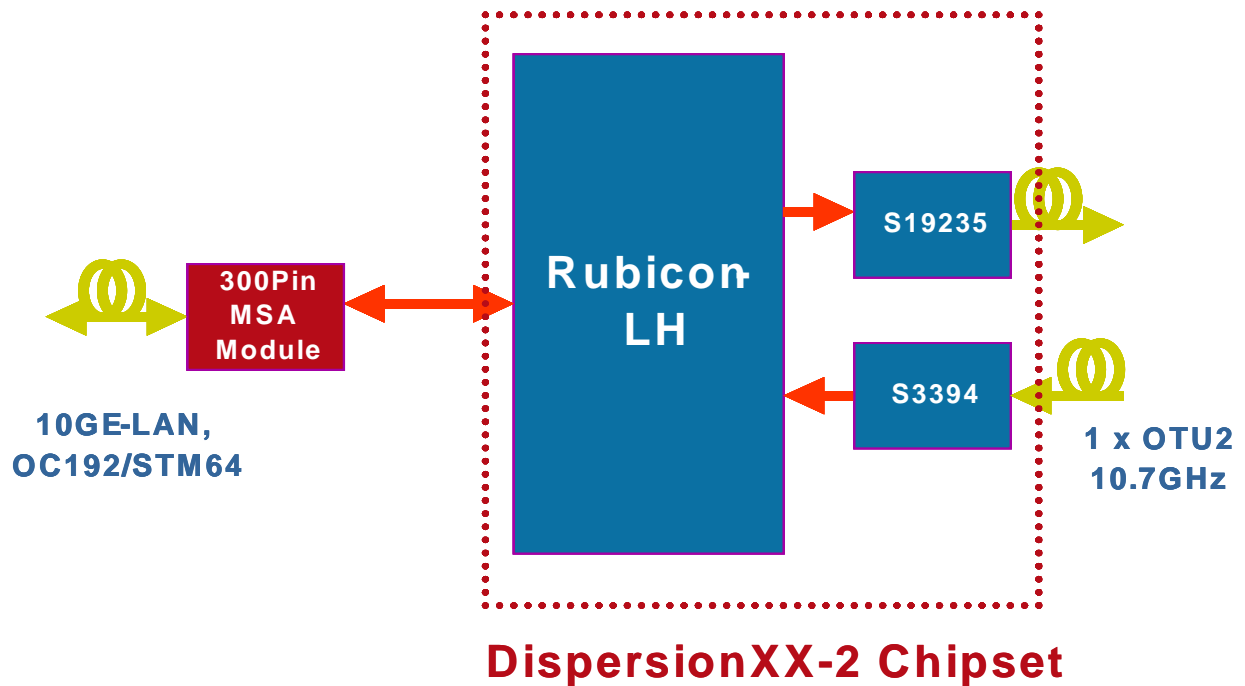
APPLICATION DIAGRAMS

Figure 2: OC192/STM64 to OTU-2 Edge Transponder

Figure 2 shows the Rubicon-LH in an edge transponder application. The client-side interface is achieved through the connection to a standard 300 Pin MSA SFI4P1 Transponder. On the network side, the AMCC S19235 and S3394 are used to provide a high-performance interface to the network side optics. This diagram is also the diagram for a mid-span transponder for either a standard FEC to standard FEC network or a standard FEC to enhanced

FEC network. In either of these mid-span transponder applications, the client rate would increase from the standard SONET rate to the 7% overhead rate.

Figure 2: OC192/STM64 to OTU-2 Edge Transponder



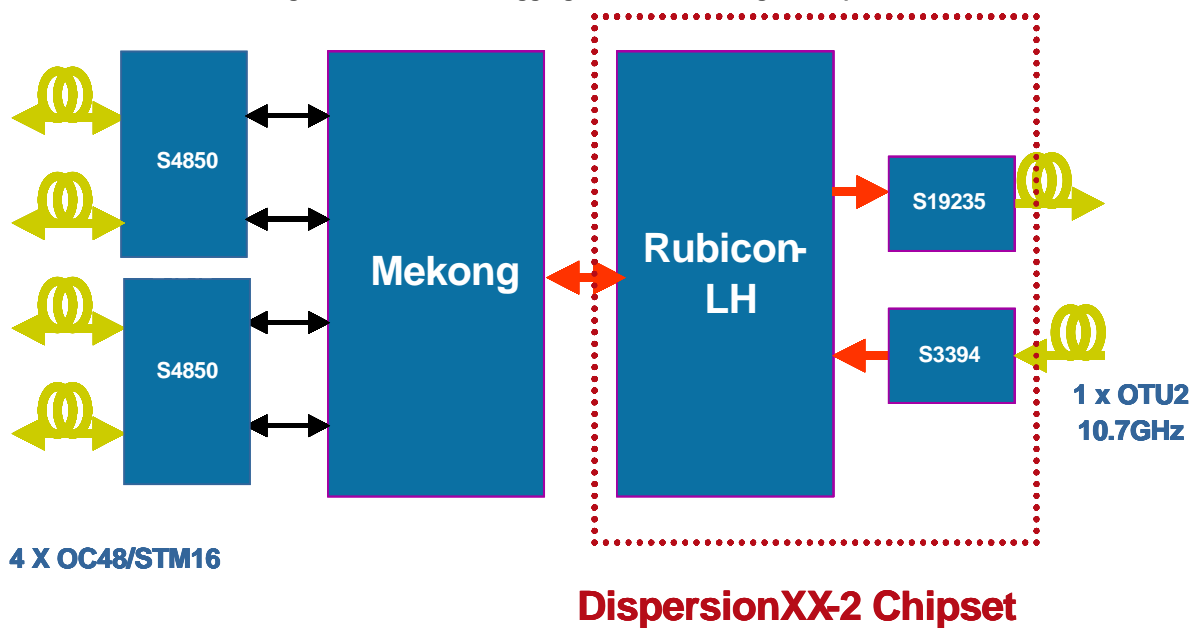
APPLICATION DIAGRAMS

Figure 3: OC48/STM16 Aggregation to OTU-2 Edge Transponder

Figure 3 shows the Rubicon-LH in an edge transponder application where the client signals are first aggregated in the AMCC Pointer Processor chip called Mekong. Once the Mekong aggregates the client 2.5G SONET/SDH signals into a OC192C/STM64 signal, this is then passed onto the Rubicon-LH which performs the OTN encapsulation and creates the FEC overhead. On the

network side, the AMCC S19235 and S3394 are used to provide a high-performance interface to the network side optics.

Figure 3: OC48/STM16 Aggregation to OTU-2 Edge Transponder



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215 Moffett Park Drive • Sunnyvale, CA 94089 • Tel: 408-542-8600 • Fax: 408-542-8601 • <http://www.amcc.com>; for technical support, please call 800 840-6055 or email support@amcc.com