SONY CXB1131Q/Q-Y

T-68-11-51

9, 8, Dual 4-bit Demultiplexer

Description

The CXB1131Q is an ultra high speed monolithic ECL Demultiplexer which functions as a 9-bit, 8-bit or dual 4-bit Serial to Parallel Converter. S1 and S2 select a bit length.

With Load Select (LS) input set to LOW, start Load pulse (ST) starts loading of the data. ST has to be maintaind High for at least (bit length −1) clock periods.

With LS set to HIGH, External Load (EL) pulse loads parallel data. The bit length is determined by a period of EL.

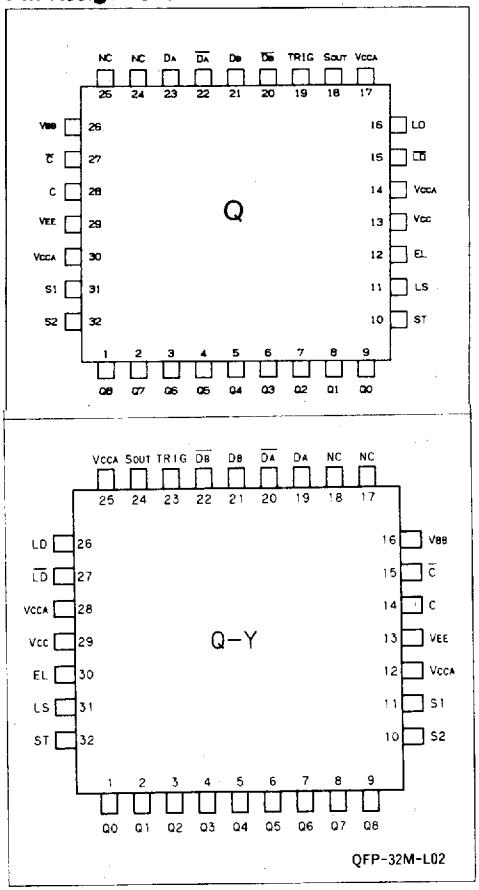
Features

- Typical clock rate up to 1.5 GHz
- Variable bit length: 9-bit,8-bit and Dual 4-bit
- Internal pull down resistors on input pins to maintain logic Low level with the pins left open
- ECL 100K compatible I/O levels
- Differential clock, data input and latch pulse output

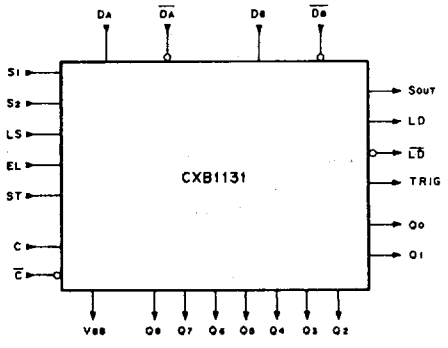
Pin Names

$D_A, \overline{D_A}$	Serial Data inputs (9, 8 and 4-bit operation)
$D_B, \overline{D_B}$	Serial Data inputs (4-bit operation)
Sn	Bit length Select inputs
LS	Load Select input
ST	Load Start input
EL	External Load pulse input
$C, \overline{C}$	Clock inputs (positive edge trigger)
Qn	Demultiplexed parallel data outputs (9, 8 and 4-bit)
S_{OUT}	Serial data output
TRIG	Trigger pulse output
$LD, \overline{LD}$	Load pulse outputs
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Neggative voltage supply

Pin Assignment



Logic Symbol



DC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−258	−190	−133	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

AC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item		Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time		T_{PLH}	C	Qn		1380	1840	2340	ps
		T_{PHL}				1350	1800	2290	
		T_{PLH}		S_{OUT}		890	1180	1500	
		T_{PHL}				870	1160	1470	
		T_{PLH}		TRIG	ST=L	1140	1520	1930	
		T_{PHL}				1130	1500	1900	
		T_{PLH}		LD	LS=L	1240	1650	2050	
		T_{PHL}				1030	1370	1740	
		T_{PLH}	EL		LS=H	750	970	1200	
		T_{PHL}				750	970	1200	
Set up time		T_S	D_A,C	Qn	LS=L	−110			
			D_B,C			260			
			C,EL		LS=H	50			
Hold time		T_h	C,D_A		LS=L	390			
			C,D_B			130			
			EL,C		LS=H	400			
Release time		T_R	ST,C			150			
Max. Clock frequency	9Bit	f_{MAX}	C			1.4	1.7		GHz
	8Bit					1.2	1.5		
	4Bit					1.3	1.6		
	External					1.4	1.7		
Rise time		T_{TLH}		Qn,LD S_{OUT},TRIG	20% to 80%		420	530	ps
Fall time		T_{THL}					360	460	

Note: AC test circuit; See pages 4-4 and 4-5.

T-68-11-51

Function Table

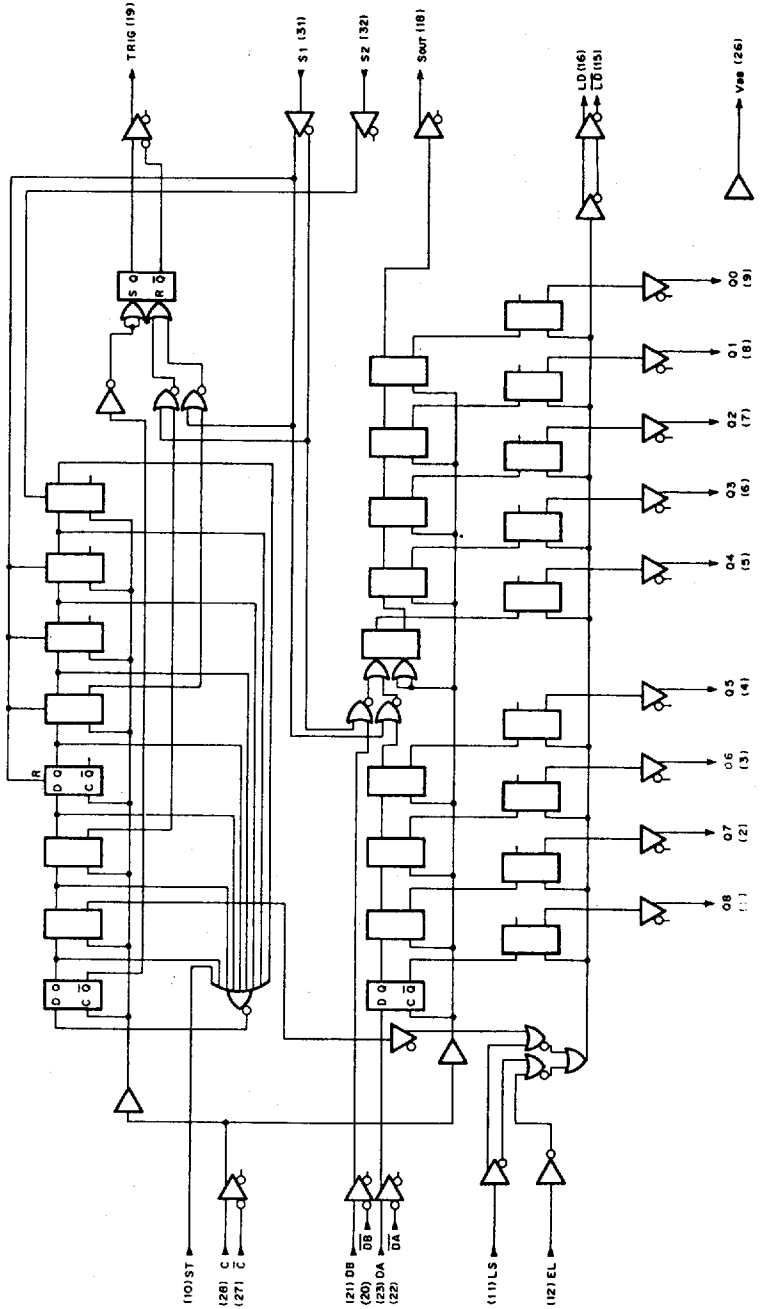
LS	S1	S2	ST	EL	C	Function			
L	L	L	L	×	∫	Internal Load	9bit	Load and output, DA → Q0-Q8	
L	L	L	H	×	∫			Initialize (8 clock period minimum)	
L	L	H	L	×	∫		8bit	Load and output, DA → Q1-Q8	
L	L	H	H	×	∫			Initialize (7 clock period minmum)	
L	H	×	L	×	∫		4bit ×2	Load and Shift	DA → Q5-Q8 DB → Q1-Q4
L	H	×	H	×	∫			Initialize (3 clock period minmum)	
H	L	×	×	×	∫	External Load	5 ≤ bit length ≤ 9		Serial Data Load
H	L	×	×	∫	×				Parallel Data Output
H	H	×	×	×	∫		bit length ≤ 4		Serial Data Load
H	H	×	×	∫	×				Parallel Data Output

H: HIGH voltage level, L: LOW voltage level, ∫: Positve transition edge, X: Don't care

In the External Load mode, serial input data is entered synchronusly with clock (C) and parallel output data is output to output pins synchronously with External Load (EL). The bit length can be datermined by the period of EL pulse. See Timing Diagram.

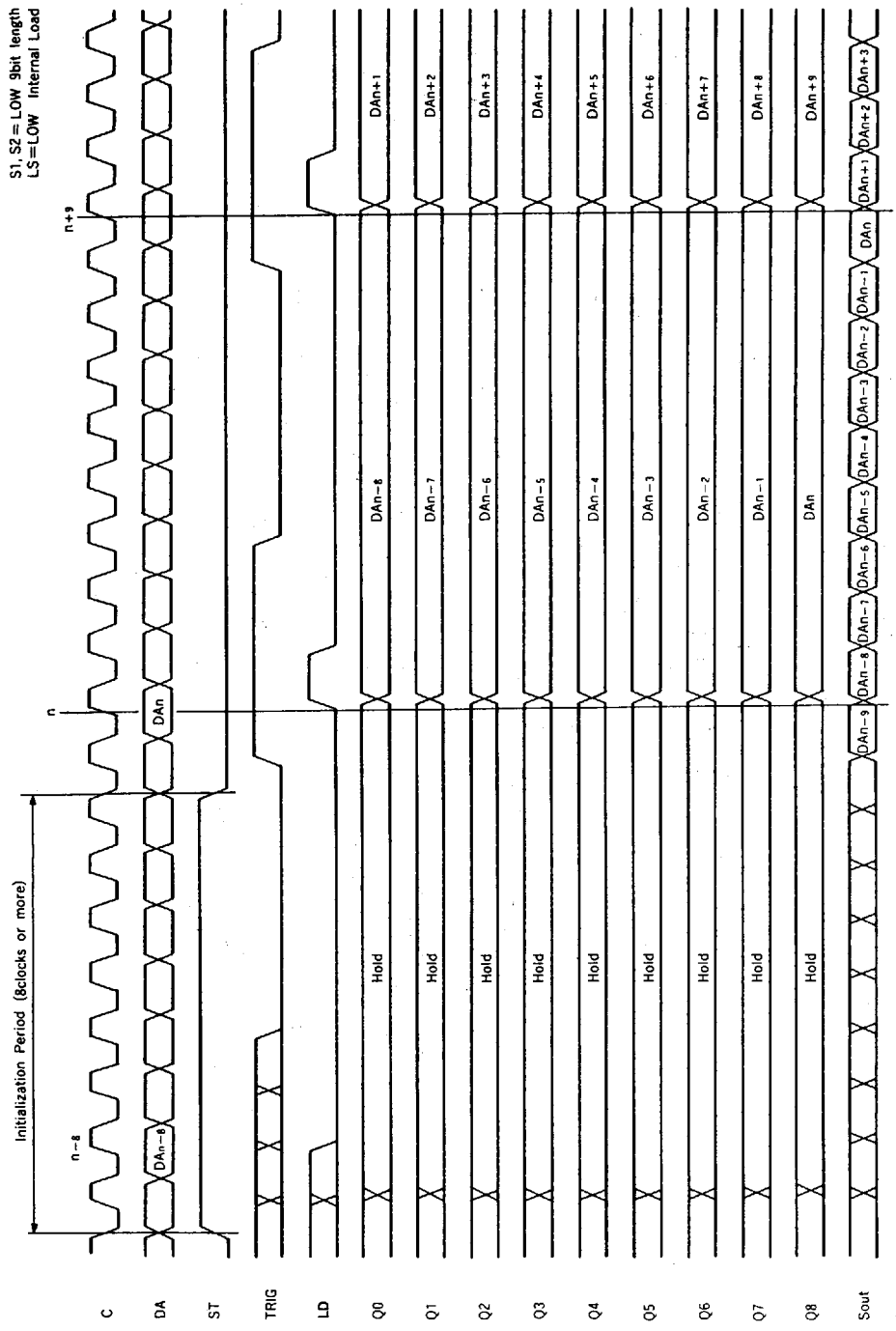
T-68-11-51

Block Diagram



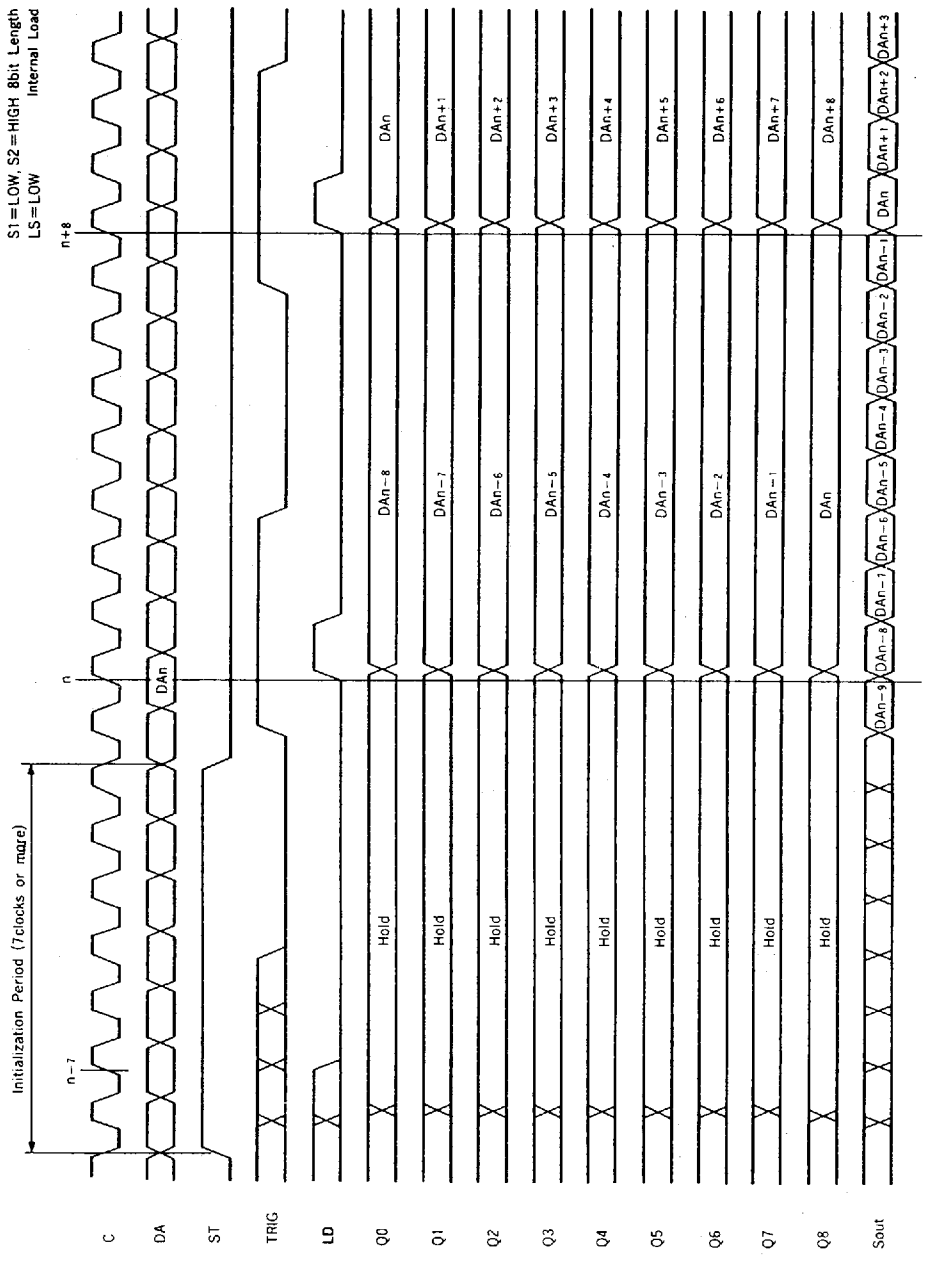
T-68-11-51

Timing Diagram — 9-bit



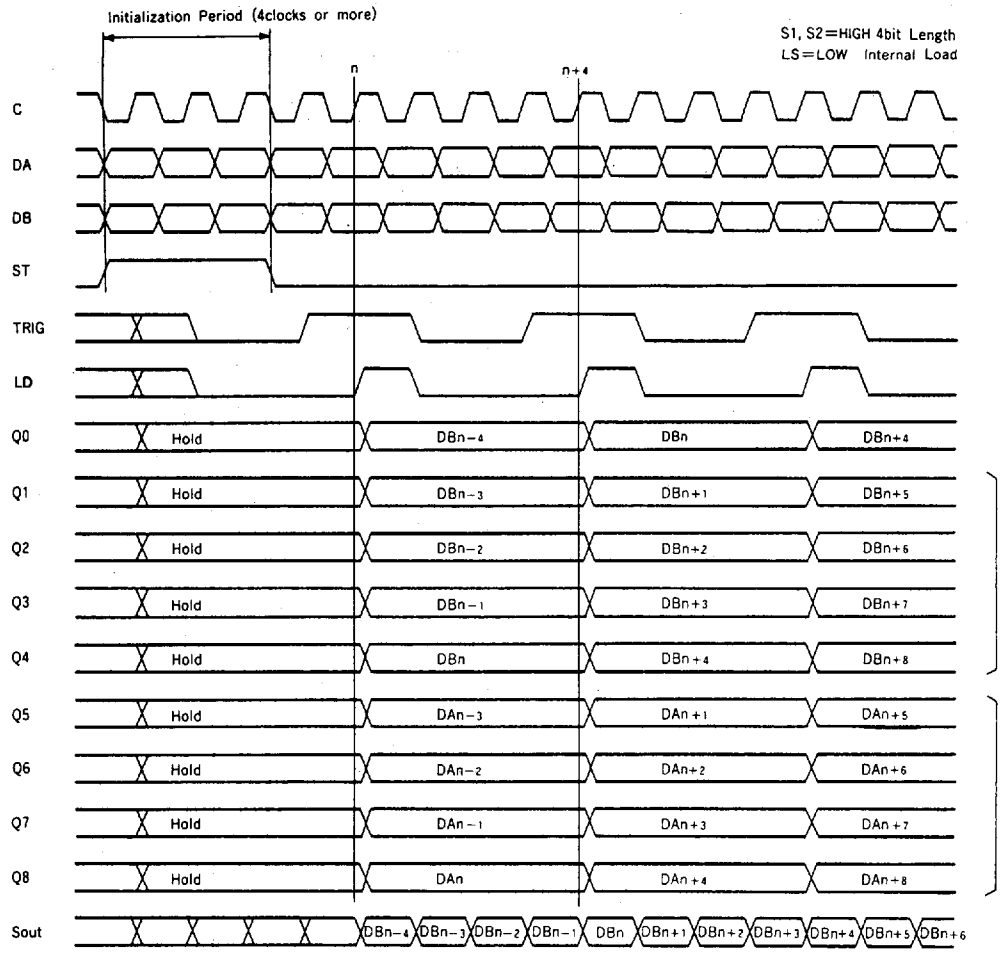
T-68-11-51

Timing Diagram — 8-bit



Timing Diagram — 4-bit×2

T-68-11-51



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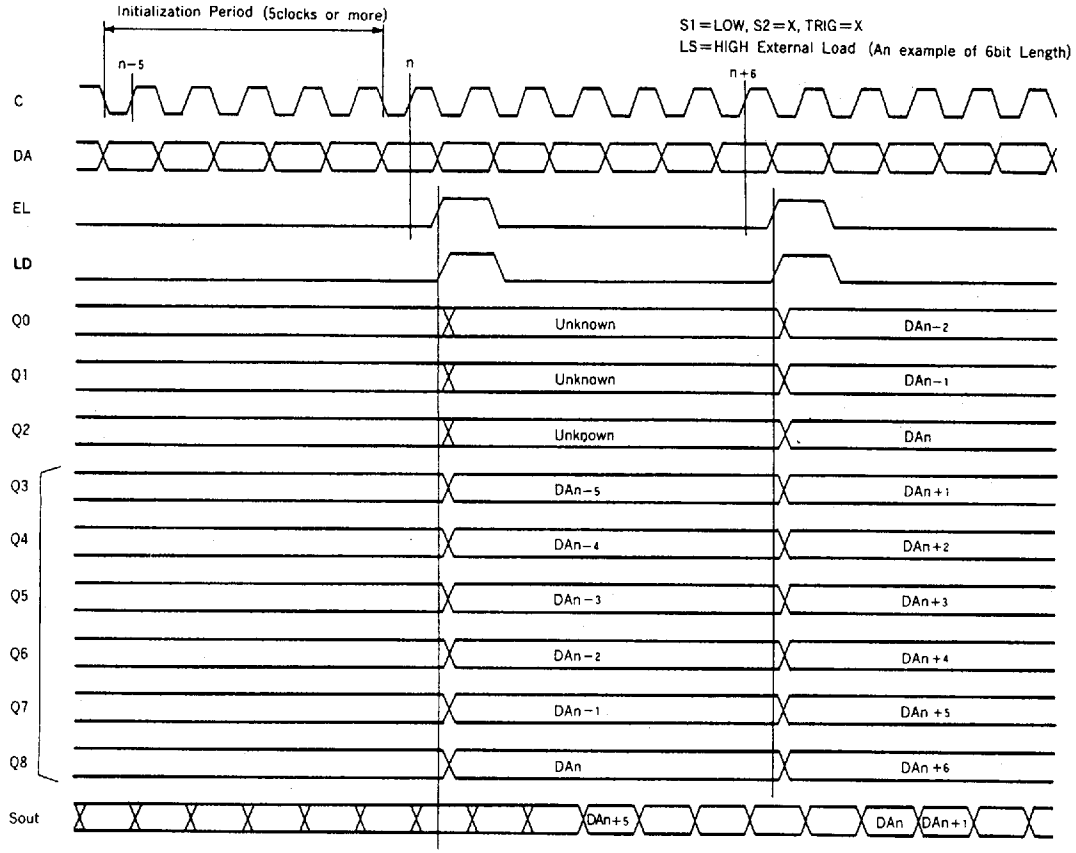
Timing Diagram — 6-bit External Load

T-68-11-51



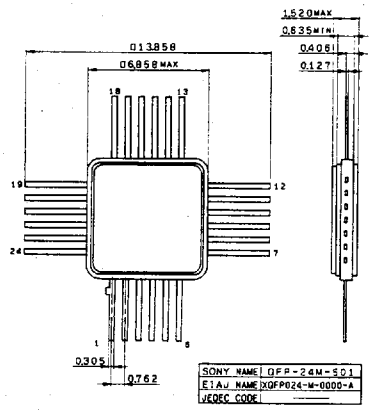
Package Data

T-90-20

Package Outline Uuit: mm

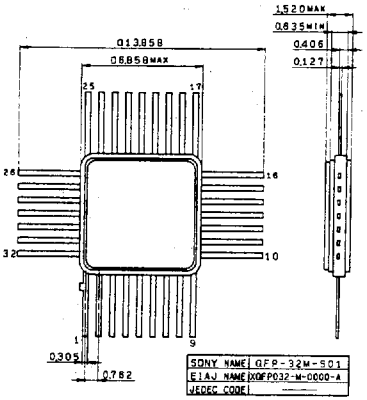
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



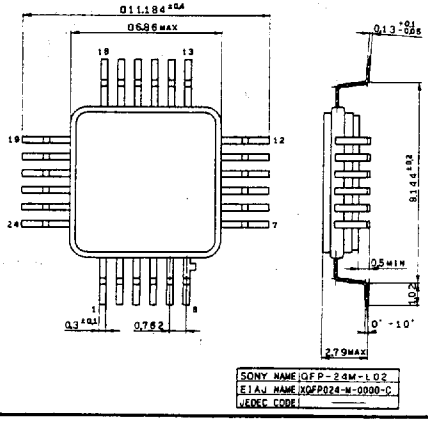
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



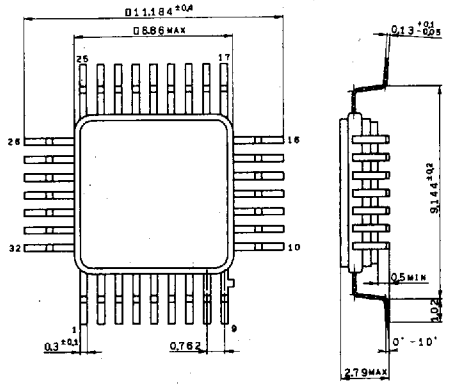
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

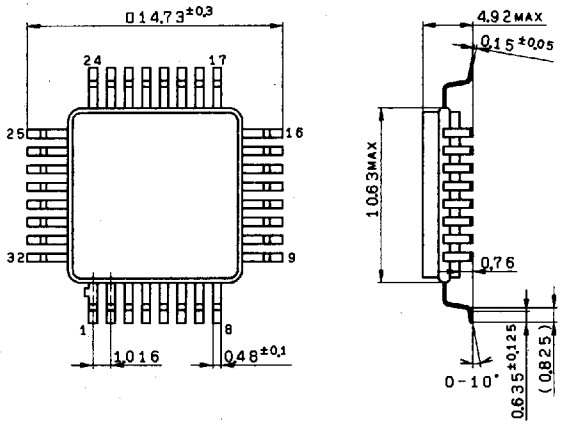
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

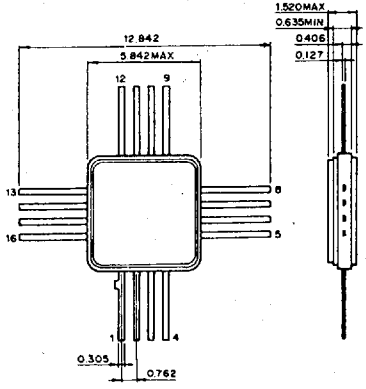
32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP



Package Data

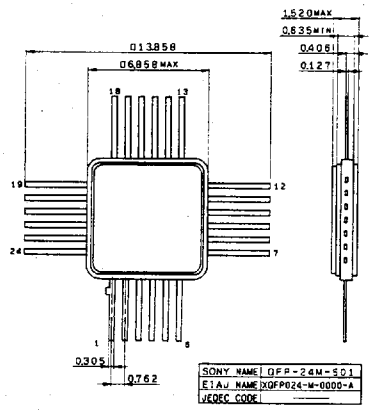
Package Data

T-90-20

Package Outline Uuit: mm

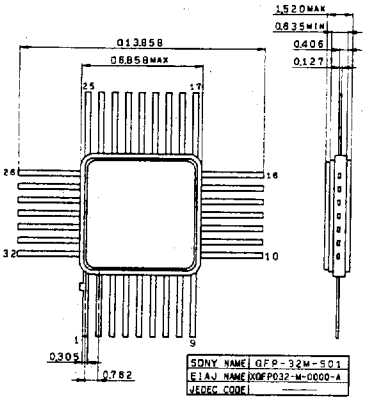
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



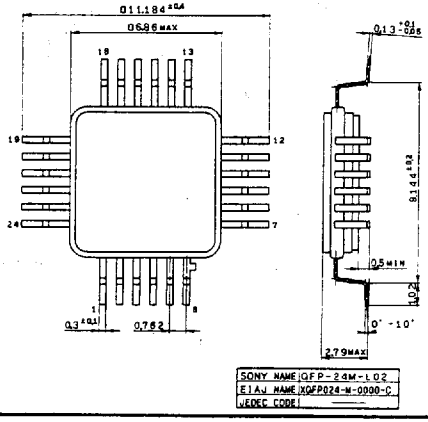
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



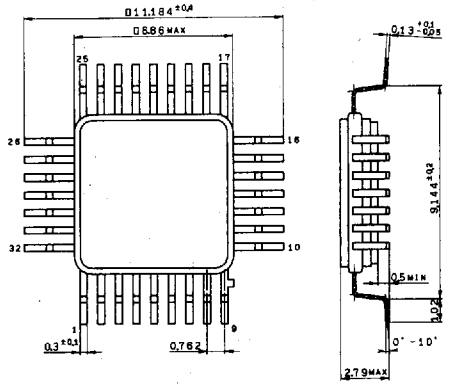
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

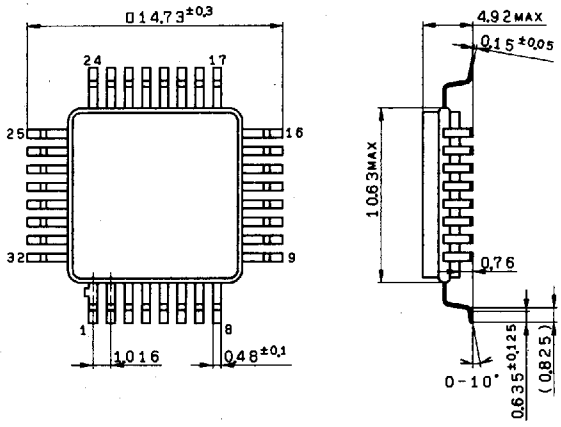
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP