

FDD2572 / FDU2572

N-Channel UltraFET® Trench MOSFET 150V, 29A, 54mΩ

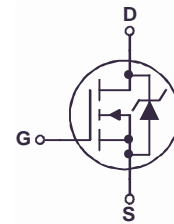
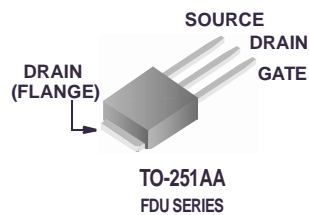
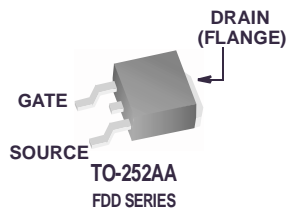
Features

- $r_{DS(ON)} = 45m\Omega$ (Typ.), $V_{GS} = 10V$, $I_D = 9A$
- $Q_g(tot) = 26nC$ (Typ.), $V_{GS} = 10V$
- Low Miller Charge
- Low Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101

Formerly developmental type 82860

Applications

- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- Direct Injection / Diesel Injection System
- 42V Automotive Load Control
- Electronic Valve Train System



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_C = 25^\circ C$, $V_{GS} = 10V$)	29	A
	Continuous ($T_C = 100^\circ C$, $V_{GS} = 10V$)	20	A
	Continuous ($T_{amb} = 25^\circ C$, $V_{GS} = 10V$, $R_{\theta JA} = 52^\circ C/W$)	4	
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	36	mJ
P_D	Power dissipation	135	W
	Derate above $25^\circ C$	0.9	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-251, TO-252	1.11	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-251, TO-252	100	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in ² copper pad area	52	$^\circ C/W$

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD2572	FDD2572	TO-252AA	330mm	16mm	2500 units
FDU2572	FDU2572	TO-251AA	Tube	N/A	75 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	150	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 9\text{A}, V_{GS} = 10\text{V}$	-	0.045	0.054	Ω
		$I_D = 4\text{A}, V_{GS} = 6\text{V}$	-	0.050	0.075	
		$I_D = 9\text{A}, V_{GS} = 10\text{V}, T_C = 175^\circ\text{C}$	-	0.126	0.146	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	1770	-	pF
C_{OSS}	Output Capacitance		-	183	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	40	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V to } 10\text{V}$	-	26	34	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V to } 2\text{V}$	-	3.3	4.3	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 75\text{V}$ $I_D = 9\text{A}$ $I_g = 1.0\text{mA}$	-	8	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	6	-	nC

Resistive Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 75\text{V}, I_D = 9\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 11.0\Omega$	-	-	36	ns
$t_{d(ON)}$	Turn-On Delay Time		-	11	-	ns
t_r	Rise Time		-	14	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	31	-	ns
t_f	Fall Time		-	14	-	ns
t_{OFF}	Turn-Off Time		-	-	66	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 9\text{A}$	-	-	1.25	V
		$I_{SD} = 4\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 9\text{A}, di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	74	ns
Q_{RR}	Reverse Recovery Charge	$I_{SD} = 9\text{A}, di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	169	nC

Notes:

1: Starting $T_J = 25^\circ\text{C}$, $L = 0.2\text{mH}$, $I_{AS} = 19\text{A}$.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted



Figure 1. Normalized Power Dissipation vs Ambient Temperature

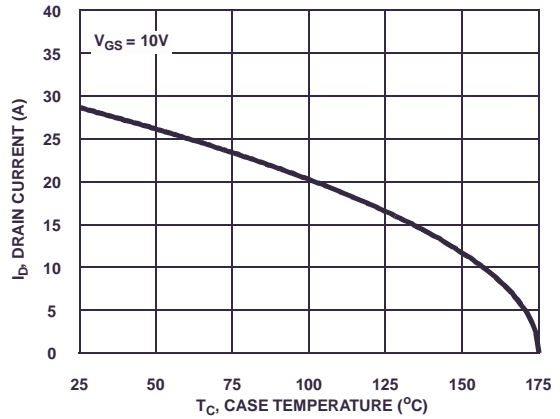


Figure 2. Maximum Continuous Drain Current vs Case Temperature

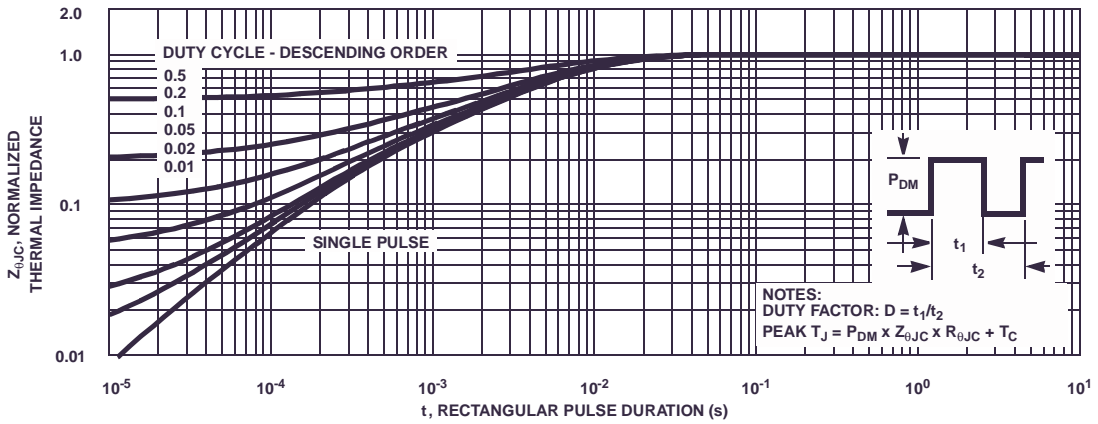


Figure 3. Normalized Maximum Transient Thermal Impedance

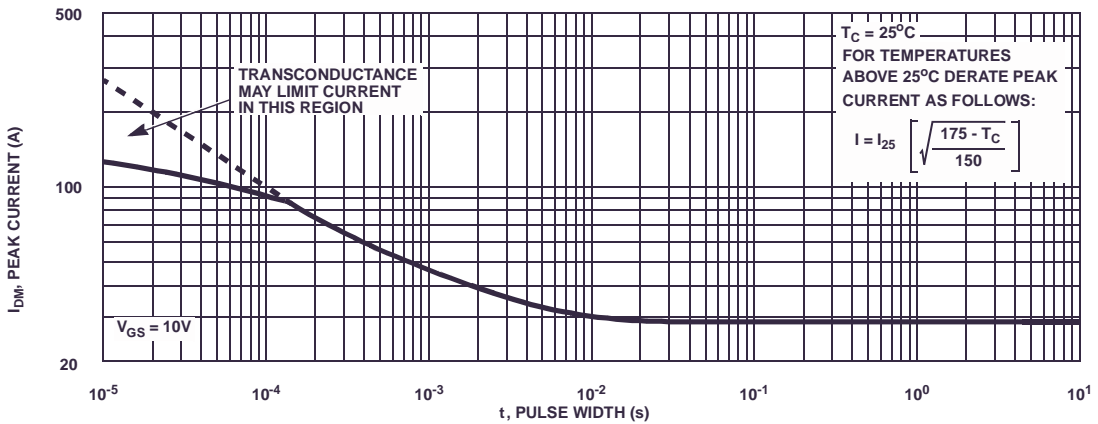
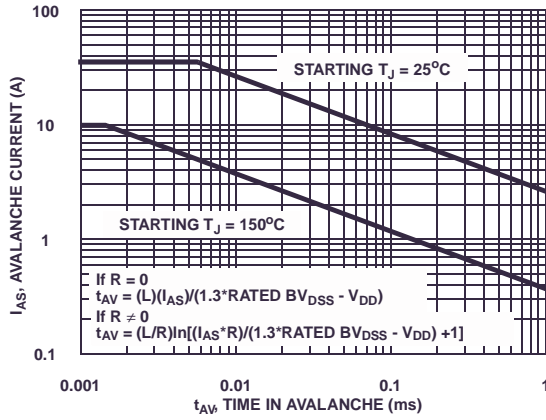


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
Figure 5. Unclamped Inductive Switching Capability

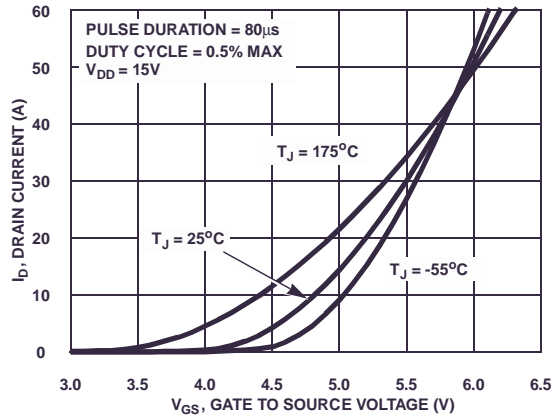


Figure 6. Transfer Characteristics

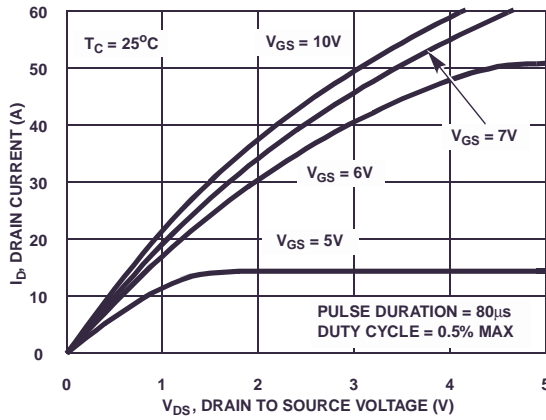


Figure 7. Saturation Characteristics

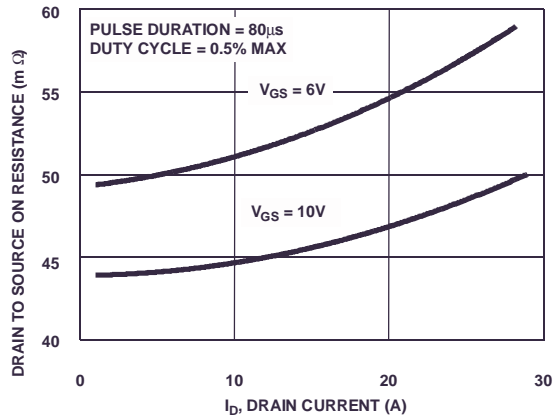


Figure 8. Drain to Source On Resistance vs Drain Current

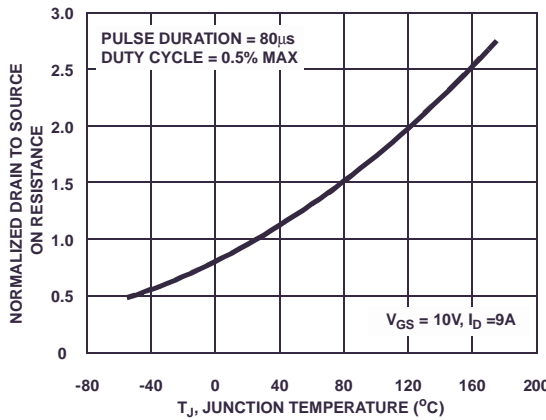


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

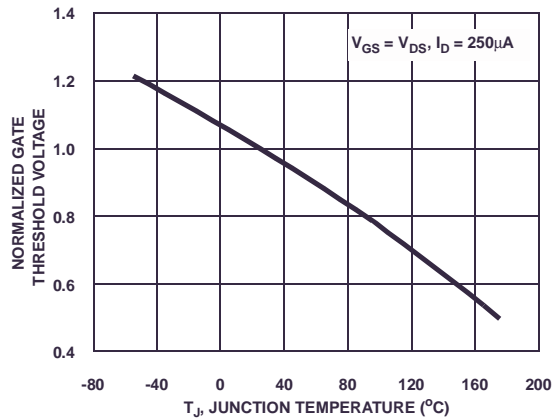


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

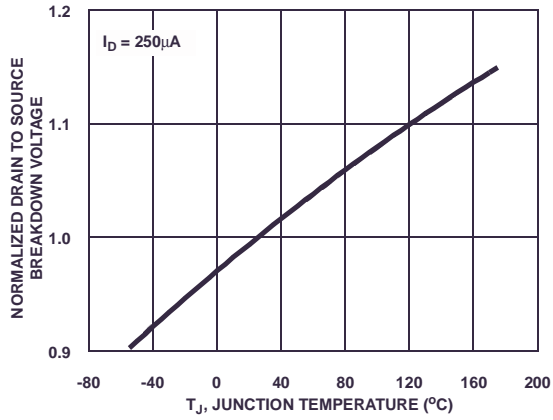


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

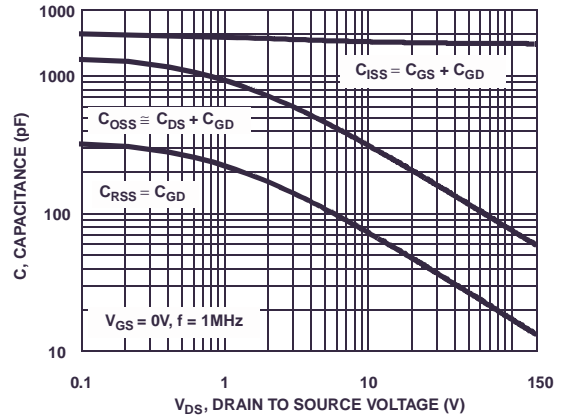


Figure 12. Capacitance vs Drain to Source Voltage

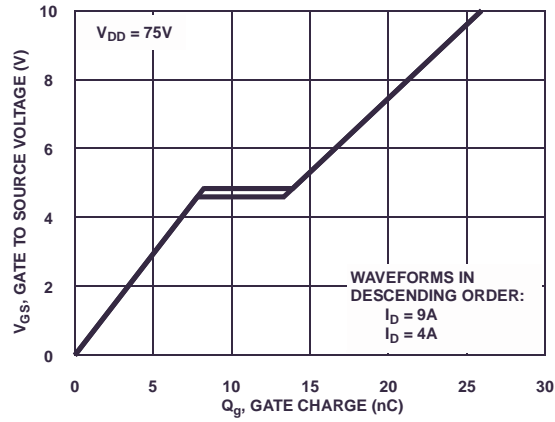


Figure 13. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms



Figure 14. Unclamped Energy Test Circuit



Figure 15. Unclamped Energy Waveforms



Figure 16. Gate Charge Test Circuit

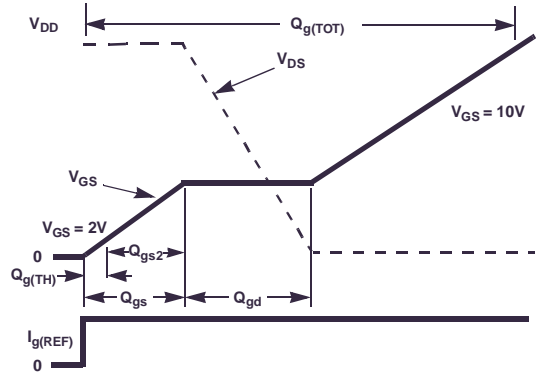


Figure 17. Gate Charge Waveforms



Figure 18. Switching Time Test Circuit



Figure 19. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}C$), and thermal resistance $R_{\theta JA}$ ($^{\circ}C/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 20 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 20 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeter square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \quad (\text{EQ. 2})$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)} \quad (\text{EQ. 3})$$

Area in Centimeters Squared

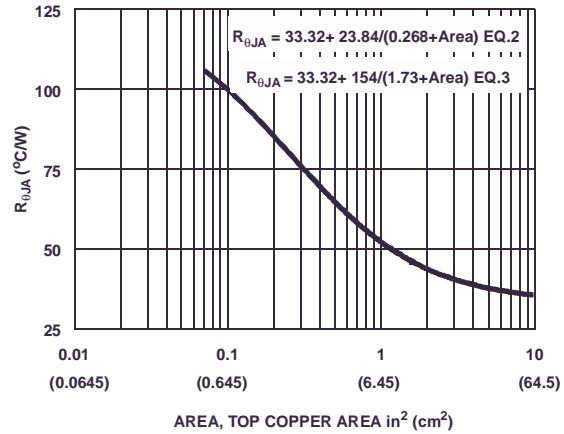


Figure 20. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model

.SUBCKT FDD2572 2 1 3 ; rev April 2002
 CA 12 8 5.5e-10
 Cb 15 14 7.4e-10
 Cin 6 8 1.7e-9

Dbody 7 5 DbodyMOD
 Dbreak 5 11 DbreakMOD
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 160
 Eds 14 8 5 8 1
 Egs 13 8 6 8 1
 Esg 6 10 6 8 1
 Evthres 6 21 19 8 1
 Evttemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 1.21e-9
 Ldrain 2 5 1.0e-9
 Lsource 3 7 4.45e-9

RLgate 1 9 12.1
 RLdrain 2 5 10
 RLsource 3 7 44.5

Mmed 16 6 8 8 MmedMOD
 Mstro 16 6 8 8 MstroMOD
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
 Rdrain 50 16 RdrainMOD 35e-3
 Rgate 9 20 1.6
 RSLC1 5 51 RSLCMOD 1.0e-6
 RSLC2 5 50 1.0e3
 Rsource 8 7 RsourceMOD 3.0e-3
 Rvthres 22 8 RvthresMOD 1
 Rvtemp 18 19 RvtempMOD 1
 S1a 6 12 13 8 S1AMOD
 S1b 13 12 13 8 S1BMOD
 S2a 6 15 14 13 S2AMOD
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*52),3))}}

.MODEL DbodyMOD D (IS=6.0E-11 N=1.14 RS=3.9e-3 TRS1=3.5e-3 TRS2=3.0e-6
 + CJO=1.1e-9 M=0.63 TT=6.2e-8 XTI=4.5)

.MODEL DbreakMOD D (RS=10 TRS1=5.0e-3 TRS2=-5.0e-6)

.MODEL DplcapMOD D (CJO=3.5e-10 IS=1.0e-30 N=10 M=0.65)

.MODEL MmedMOD NMOS (VTO=3.55 KP=3 IS=1e-40 N=10 TOX=1 L=1u W=1u RG=1.6)

.MODEL MstroMOD NMOS (VTO=4.0 KP=25 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL MweakMOD NMOS (VTO=2.95 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=16 RS=0.1)

.MODEL RbreakMOD RES (TC1=1.15e-3 TC2=-9.5e-7)

.MODEL RdrainMOD RES (TC1=9.0e-3 TC2=2.5e-5)

.MODEL RSLCMOD RES (TC1=3.0e-3 TC2=2.5e-6)

.MODEL RsourceMOD RES (TC1=4.0e-3 TC2=1.0e-6)

.MODEL RvthresMOD RES (TC1=-4.1e-3 TC2=-1.0e-5)

.MODEL RvtempMOD RES (TC1=-4.0e-3 TC2=1.0e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.0 VOFF=-3.5)

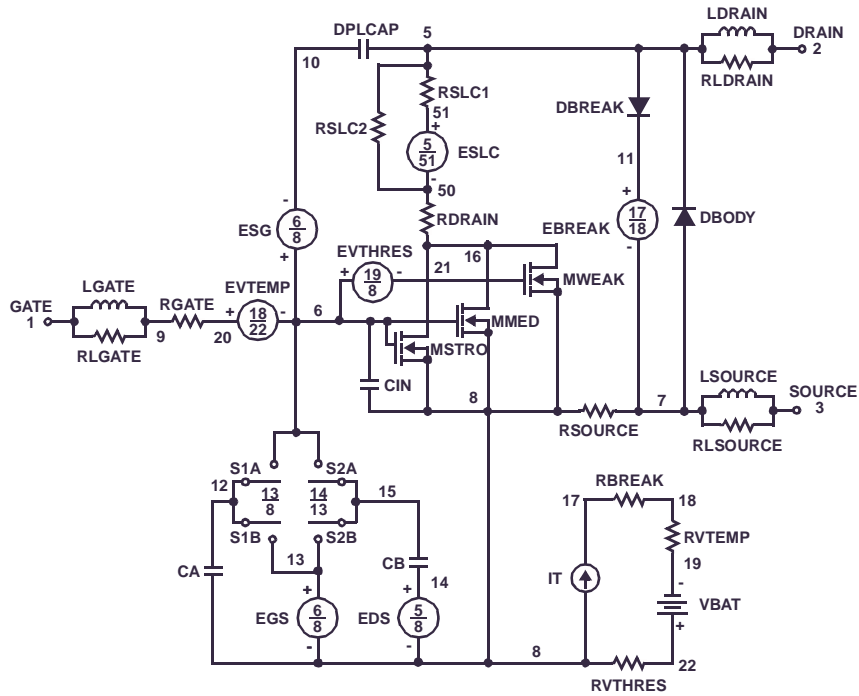
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-5.0)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.3)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.5)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

REV April 2002

ttemplate FDD2572 n2,n1,n3

electrical n2,n1,n3

{

var i iscl

dp..model dbodymod = (isl=6.0e-11,nl=1.14,rs=3.9e-3,trs1=3.5e-3,trs2=3.0e-6,cjo=1.1e-9,m=0.63,tt=6.2e-8,xti=4.5)

dp..model dbreakmod = (rs=10,trs1=5.0e-3,trs2=-5.0e-6)

dp..model dplcapmod = (cjo=3.5e-10,isl=10.0e-30,nl=10,m=0.65)

m..model mmedmod = (type=_n,vto=3.55,kp=3,is=1e-40,tox=1)

m..model mstrongmod = (type=_n,vto=4.0,kp=25,is=1e-30,tox=1)

m..model mweakmod = (type=_n,vto=2.95,kp=0.05,is=1e-30,tox=1,rs=0.1)

sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-5.0,voff=-3.5)

sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3.5,voff=-5.0)

sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=0.3,voff=0.3)

sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.3,voff=-0.5)

c.ca n12 n8 = 5.5e-10

c.cb n15 n14 = 7.4e-10

c.cin n6 n8 = 1.7e-9

dp.dbody n7 n5 = model=dbodymod

dp.dbreak n5 n11 = model=dbreakmod

dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 160

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evthres n6 n21 n19 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 1.21e-9

l.ldrain n2 n5 = 1.0e-9

l.lsource n3 n7 = 4.45e-9

res.rlgate n1 n9 = 12.1

res.rldrain n2 n5 = 10

res.rlsource n3 n7 = 44.5

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u

m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=1.15e-3,tc2=-9.5e-7

res.rdrain n50 n16 = 35e-3, tc1=9.0e-3,tc2=2.5e-5

res.rgate n9 n20 = 1.6

res.rslc1 n5 n51 = 1.0e-6, tc1=3.0e-3,tc2=2.5e-6

res.rslc2 n5 n50 = 1.0e3

res.rsource n8 n7 = 3.0e-3, tc1=4.0e-3,tc2=1.0e-6

res.rvthres n22 n8 = 1, tc1=-4.1e-3,tc2=-1.0e-5

res.rvtemp n18 n19 = 1, tc1=-4.0e-3,tc2=1.0e-6

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

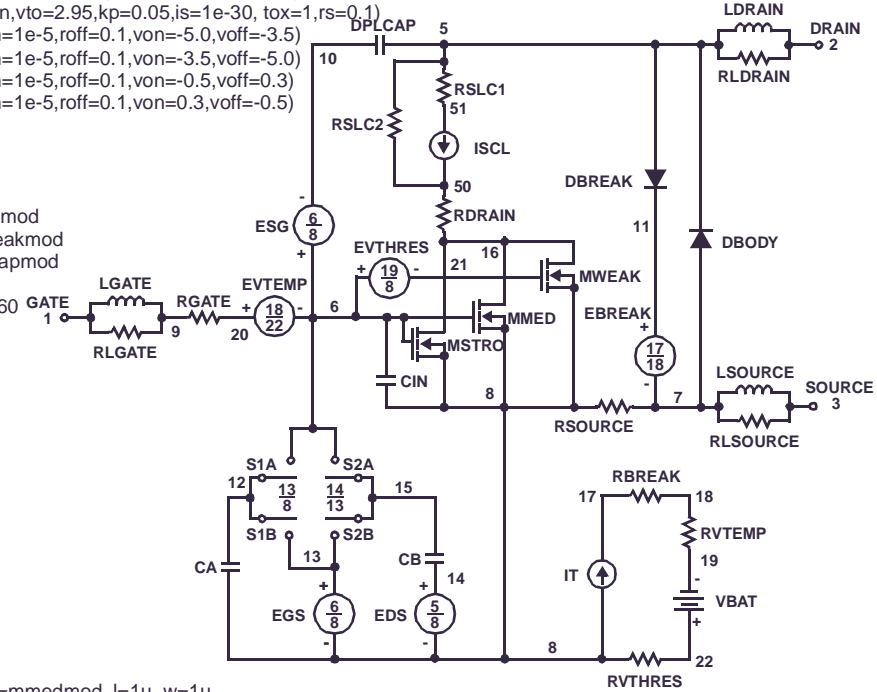
v.vbat n22 n19 = dc=1

equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = (((n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/52)** 3))

}



SPICE Thermal Model

REV 26 April 2002

FDD2572

CTHERM1 TH 6 3.8e-3
 CTHERM2 6 5 4.0e-3
 CTHERM3 5 4 4.2e-3
 CTHERM4 4 3 4.3e-3
 CTHERM5 3 2 8.5e-3
 CTHERM6 2 TL 3.0e-2

RTHERM1 TH 6 5.5e-4
 RTHERM2 6 5 5.0e-3
 RTHERM3 5 4 4.5e-2
 RTHERM4 4 3 10.5e-2
 RTHERM5 3 2 3.7e-1
 RTHERM6 2 TL 3.8e-1

SABER Thermal Model

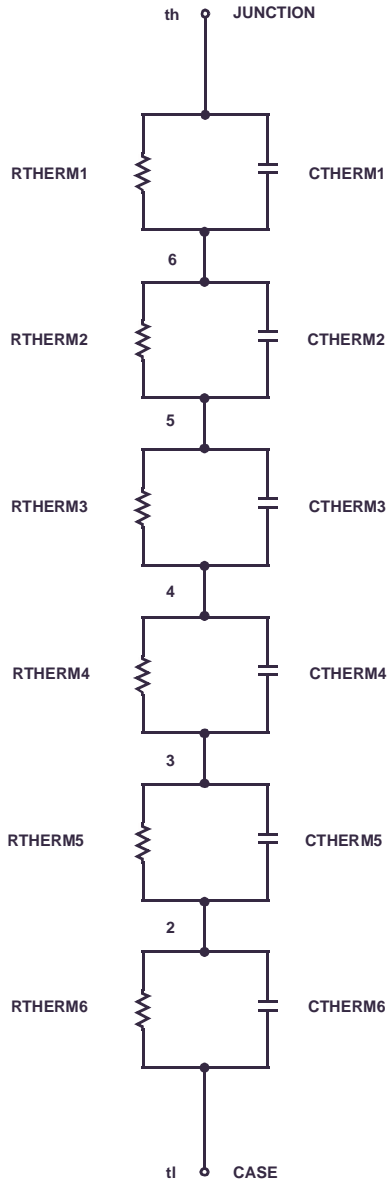
SABER thermal model FDD2572

template thermal_model th tl

thermal_c th, tl

```
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ctherm.ctherm2 6 5 =4.0e-3
ctherm.ctherm3 5 4 =4.2e-3
ctherm.ctherm4 4 3 =4.3e-3
ctherm.ctherm5 3 2 =8.5e-3
ctherm.ctherm6 2 tl =3.0e-2
```

```
rtherm.rtherm1 th 6 =5.5e-4
rtherm.rtherm2 6 5 =5.0e-3
rtherm.rtherm3 5 4 =4.5e-2
rtherm.rtherm4 4 3 =10.5e-2
rtherm.rtherm5 3 2 =3.7e-1
rtherm.rtherm6 2 tl =3.8e-1
}
```



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CROSSVOLT™	HiSeC™	PowerTrench®	SyncFET™
DOME™	I ² C™	QFET™	TinyLogic™
EcoSPARK™	ISOPLANAR™	QS™	TruTranslation™
E ² CMOS™	LittleFET™	QT Optoelectronics™	UHC™
EnSigna™	MicroFET™	Quiet Series™	UltraFET®
FACT™	MicroPak™	SILENT SWITCHER®	VCX™
FACT Quiet Series™	MICROWIRE™	SMART START™	
FAST®	OPTOLOGIC®	SPM™	
FASTr™	OPTOPLANAR™	Stealth™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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