Master I/O

DATA SHEET

32-bit SBus Master I/O Controller

DESCRIPTION

The STP2000 Master I/O Controller is an integrated SBus master device with built-in standard I/O capabilities for general purpose computing or embedded applications. The STP2000 directly interfaces the CPU through the system bus, SBus, to three major I/O channels for peripherals. The I/O channels include SCSI-II, ethernet and a parallel port. Together, with the STP2001 Slave I/O Controller, it provides a complete I/O subsystem.

The STP2000 SBus interface is a 32-bit interface that supports both DMA and slave modes. There is data buffering and flow control on each of the I/O channels. Each channel has access to the SBus through the controller which is capable of DMA transfers of up to 32-byte bursts. The SBus slave port is used mostly for status and control.

The STP2000 incorporates an ethernet controller, a Fast 8-bit SCSI-II controller, and a Centronics parallel port controller in a single package. The SCSI-II channel directly drives external peripherals. The ethernet channel can be connected to an external transceiver chip that supports twisted pair ethernet or AUI ethernet. The parallel port channel can be routed to external transceivers.

Features	*Benefits*
• Single-chip solution to standard SPARC DVMA devices	• Saves cost, power, board space, and weight
• Compatible with microSPARC, SuperSPARC and any SBus based system	• Standard low-cost solution
• Supports concurrent 10 MByte/sec SCSI transfers, 1.25 MByte/sec Ethernet transfers, and 4 MByte/sec Parallel Port transfers	• Improved system performance
• Direct master/slave SBus interface	• Improved system performance
• JTAG internal and boundary SCAN logic	• Improved chip and board level testability
• 160-pin PQFP packaging	• Cost effective packaging
• IC is also available from NCR Corp. (PN - NCR89C100)	• Second source

BLOCK, APPLICATION, AND LOGIC DIAGRAMS

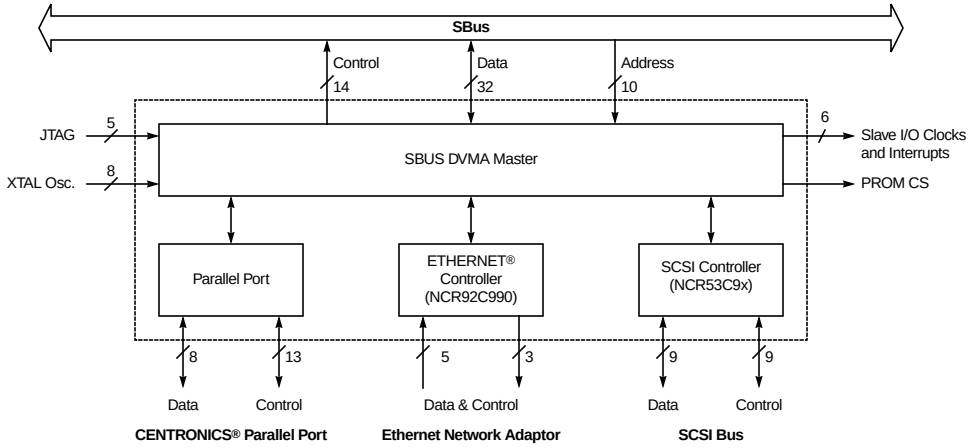


Figure 1. STP2000 Block Diagram

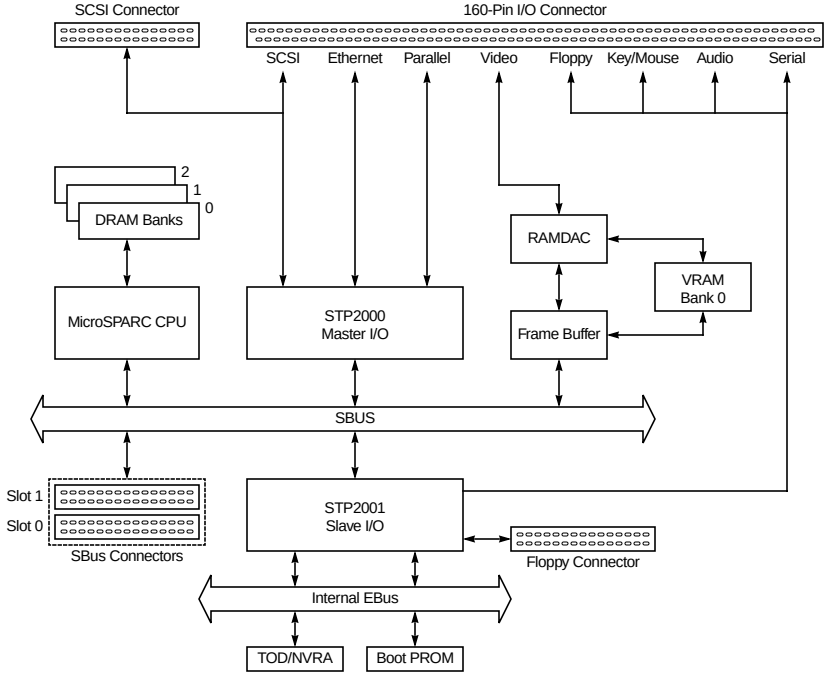


Figure 2. STP2000 Typical Application

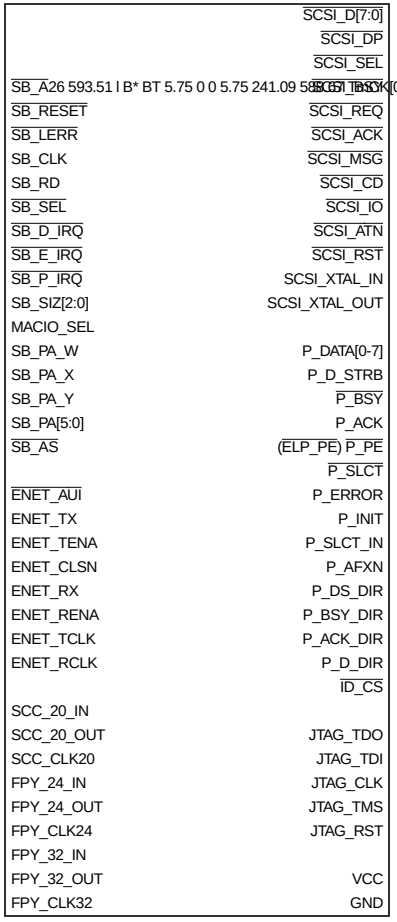


Figure 3. STP2000 Logical Connections

SIGNAL DESCRIPTIONS

SBus Interface

Name	Type	Description
SB_D[31:0]	I/O	SBus Data Bus (MSB)
$\overline{\text{SB\_BR}}$	I/O	SBus Bus Request
$\overline{\text{SB\_BG}}$	Input	SBus Bus Grant
$\overline{\text{SB\_ACK}}$[2:0]	I/O	SBus Acknowledge
$\overline{\text{SB\_RESET}}$	Input	SBus Reset
$\overline{\text{SB\_LERR}}$	Input	SBus Late Error (INT15)
SB_CLK	Input	SBus Clock Input
SB_RD	I/O	SBus Read/Write
$\overline{\text{SB\_SEL}}$	Input	SBus Select
$\overline{\text{SB\_D\_IRQ}}$	Output	SBus Interrupt for SCSI transfers (open-drain)
$\overline{\text{SB\_E\_IRQ}}$	Output	SBus Interrupt for ETHERNET transfers (open-drain)
$\overline{\text{SB\_P\_IRQ}}$	Output	SBus Interrupt for Parallel Port Transfers (open-drain)
SB_SIZ[2:0]	I/O	SBus Transfer Size
$\overline{\text{SB\_AS}}$	Input	SBus Address Strobe (address is valid)
CHIP_SEL [1]	Input	High order physical address bit
SB_PA[W]	Input	High order physical address bit
SB_PA[X]	Input	High order physical address bit
SB_PA[Y]	Input	High order physical address bit
SB_PA[5:0]	Input	Low order physical address bits

1. The CHIP_SEL pin is an additional qualifier (active high) to the $\overline{\text{SB\_SEL}}$ line. In some system configurations where the STP2000 (Master I/O Controller) and the STP2001 (Slave I/O Controller) share a single SBus select line, PA[27] can be used to select between the two.

Ethernet Interface

Name	Type	Description
$\overline{\text{ENET\_AUI}}$ [1]	Output	Ethernet TP/AUI select
ENET_TX	Output	Ethernet Transmit data
ENET_TENA	Output	Ethernet Transmit enable
ENET_CLSN	Input	Ethernet Collision detect
ENET_RX	Input	Ethernet Receive data
ENET_RENA	Input	Ethernet Receiver enable (carrier sense)
ENET_TCLK	Input	Ethernet Transmit clock
ENET_RCLK	Input	Ethernet Receive clock

1. Drives MIS input of the AT&T T7213 chip to select between twisted pair and AUI-type Ethernet interfaces, with $\overline{\text{ENET\_AUI}}$ = 0 selecting AUI.

SCSI Interface [1]

Name	Type	Description
SCSI_D[7:0]	I/O	SCSI Data
$\overline{\text{SCSI\_DP}}$	I/O	SCSI Data Parity
$\overline{\text{SCSI\_SEL}}$	I/O	SCSI Select
$\overline{\text{SCSI\_BSY}}$	I/O	SCSI Busy
$\overline{\text{SCSI\_REQ}}$	I/O	SCSI Request
$\overline{\text{SCSI\_ACK}}$	I/O	SCSI Acknowledge
$\overline{\text{SCSI\_MSG}}$	I/O	SCSI Message
$\overline{\text{SCSI\_CD}}$	I/O	SCSI Command/Data
$\overline{\text{SCSI\_IO}}$	I/O	SCSI Input/Output
$\overline{\text{SCSI\_ATN}}$	I/O	SCSI Attention
$\overline{\text{SCSI\_RST}}$	I/O	SCSI Reset
SCSI_XTAL_IN	Input	SCSI Clock Crystal In (can drive with external CMOS clock)
SCSI_XTAL_OUT	Output	SCSI Clock Crystal Out (must not connect to any external load)

1. All of the SCSI pads (except the crystal oscillator pads) are custom NCR 48 mA bidirectional open-drain pads with hysteresis on inputs.

Parallel Port Interface

Name	Type	Description
P_DATA[7:0]	3-State	Parallel Port Data Bus
P_D_STRB	I/O	Parallel Port Data Strobe (25 µA pull-down)
$\overline{\text{P\_BSY}}$	I/O	Parallel Port Busy (25 µA pull-up)

Parallel Port Interface

Name	Type	Description
P_ACK	I/O	Parallel Port Acknowledge (25 µA pull-down)
(ELP_PE) P_PE	I/O	Parallel Port Paper Error
P_SLCT	I/O	Parallel Port Select
P_ERROR	Input	Parallel Port Error
P_INIT	Output	Parallel Port Initialize
P_SLCT_IN	Output	Parallel Port Select In
P_AFXN	Output	Parallel Port Auto Feed
P_DS_DIR [1]	Output	Parallel Port Data Strobe Direction
P_BSY_DIR [1]	Output	Parallel Port Busy Direction
P_ACK_DIR [1]	Output	Parallel Port Acknowledge Direction
P_D_DIR [1]	Output	Parallel Port Data Direction
ID_CS	Output	Secondary Device Select (boot prom) output; pull low to specify absence of external PROM

1. The Parallel Port control and data line direction bits, (for example, P_*_DIR), are gang programmed by the DIR bit of the Transfer Control Register.
DIR=0 sets transfer direction away from the STP2000 (P_D_DIR=P_DS_DIR=1; P_BSY_DIR=P_ACK_DIR=0); DIR=1 sets transfer direction towards the STP2000 (P_D_DIR=P_DS_DIR=0; P_BSY_DIR=P_ACK_DIR=1).

JTAG Interface

Name	Type	Description
JTAG_TDO	Output	JTAG Test Data Output
JTAG_TDI	Input	JTAG Test Data Input (100 µA pull-up)
JTAG_CLK	Input	JTAG Clock
JTAG_TMS	Input	JTAG Test Mode Select (100 µA pull-up)
JTAG_RST	Input	JTAG Reset (100 µA pull-up)

Clock/Oscillator Interface [1]

Name	Type	Description
SCC_20_IN	Input	SCC Clock Crystal In (19.66 MHz) (can drive with external CMOS clock)
SCC_20_OUT	Output	SCC Clock Crystal Out (19.66 MHz) (must not connect to any external load)
SCC_CLK20	Output	SCC Clock Out (19.66 MHz)
FPY_24_IN	Input	Floppy Clock Crystal In (24 MHz) (can drive with external CMOS clock)
FPY_24_OUT	Output	Floppy Clock Crystal Out (24 MHz) (must not connect to any external load)
FPY_CLK24	Output	Floppy Clock Out (24 MHz)

Clock/Oscillator Interface [1] (Continued)

Name	Type	Description
FPY_32_IN	Input	Floppy Clock Crystal In (32 MHz) (can drive with external CMOS clock)
FPY_32_OUT	Output	Floppy Clock Crystal Out (32 MHz) (must not connect to any external load)
FPY_CLK32	Output	Floppy Clock Out (32 MHz)

1. In some system configurations, the STP2000 provides these three clocks to the STP2001 (Slave I/O Controller) (which is pin limited). These are really general-purpose 20-50 MHz crystal oscillator pads that can operate in both fundamental and overtone mode.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage	7.0	V
V_{IN}	Input voltage	V_{CC} + 0.5	V
I_I	Current Drain V_{CC} and GND	100	mA
T_L	Lead temperature (less than 10 second soldering)	250	°C
T_J	Operating temperature	0 to +70	°C
T_S	Storage temperature	-55 to +150	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply voltage	4.75	5.0	5.25	V
T_A	Operating Temperature	0	25	70	°C
P_D	Power consumption (@ 25 MHz SBus)	–	750	1400	mW

Capacitance

Symbol	Parameter	Typ	Max	Units
C_{IN}	Input capacitance	6	–	pF
C_{OUT}	Output capacitance	6	–	pF
C_{BI}	Bidirectional pin capacitance	6	–	pF
C_{SCSI}	SCSI pin capacitance	–	10	pF

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units
V_{IH}	Input high voltage		2.0	–	–	V
V_{IL}	Input Low voltage		–	–	0.8	V
V_{OH}	High level output voltage		4.4	4.5	–	V
V_{OL}	Low level output voltage		–	0	0.1	V
I_{IN}	Input leakage current		-10	–	10	µA
I_{OH}	High level source current (V_{OH} = 2.4 V)	I_{OH} = 2.0 mA	2	–	–	mA
		I_{OH} = 4.0 mA	4	–	–	mA
		I_{OH} = 8.0 mA	8	–	–	mA
		I_{OH} = 16.0 mA	16	–	–	mA
		I_{OH} = 24.0 mA	24	–	–	mA
I_{OL}	Low level sink current (V_{OL} = 0.4 V)	I_{OL} = -2.0 mA	2	–	–	mA
		I_{OL} = -4.0 mA	4	–	–	mA
		I_{OL} = -8.0 mA	8	–	–	mA
		I_{OL} = -16.0 mA	16	–	–	mA
		I_{OL} = -24.0 mA	24	–	–	mA
		I_{OL} = -48.0 mA	48	–	–	mA
		SCSIPAD (V_{OL} = 0.5 V)	48	–	–	mA
		SCSIPADF (V_{OL} = 0.5 V)	48	–	–	mA

AC Characteristics: SBus Timing

Signal #	Parameter	Conditions	Min	Max	Units
1	Clock Period		40.0	60.0	ns
2	Clock High		17.0	–	ns
3	Clock Low		17.0	–	ns
4	Hold wrt CLK Rising		0.0	–	ns
5	Setup to CLK Rising		15.0	–	ns
6	Hold wrt CLK Rising [1]		1.0	–	ns
7	Hold wrt CLK Rising		0.0	–	ns
8	CLK Rising to Output Valid	160 pF load	2.5	22.5	ns
9	CLK Rising to Output Invalid	160 pF load	2.5	20.0	ns

1. This is the only violation of SBus Specification B.0. No known implementation to date provides less than 1.0 ns hold time on these signals.

AC Characteristics: Parallel Port Timing

Signal #	Parameter	Conditions	Min	Max	Units
10	CLK to P_D_STRB	75 pF	–	35	ns
11	P_D_STRB nominal width	DSW=0,1,2,3	3	–	SB_CLK periods
12	P_DATA valid to P_D_STRB assert	75 pF	5	–	ns
13	P_DATA valid (nominal)	DSS=0, DSN=3	6	–	SB_CLK periods
14	P_ACK, $\overline{\text{P\_BSY}}$ setup to CLK		5	–	ns
15	P_ACK, $\overline{\text{P\_BSY}}$ input pulse width		3	–	SB_CLK periods
16	P_D_STRB setup to CLK		5	–	ns
17	P_D_STRB input pulse width		3	–	SB_CLK periods
18	P_DATA setup to P_D_STRB		36	–	ns
19	P_DATA input hold from P_D_STRB		4	–	SB_CLK periods
20	P_D_STRB to $\overline{\text{P\_BSY}}$ valid	75 pF	2	3 + 26 ns	SB_CLK periods
21	CLK to P_ACK, $\overline{\text{P\_BSY}}$	75 pF	–	40	ns
22	P_ACK, $\overline{\text{P\_BSY}}$ nominal pulse width	75 pF	3	–	SB_CLK periods
23	CLK to output	75 pF	–	35	ns

AC Characteristics: SCSI TIming

Signal #	Parameter	Conditions	Min	Max	Units
24	Clock period (t_{CP})		25	83.3	ns
25	Synchronization latency		t_{CL}	$t_{CL} + t_{CP}$	ns
	With FASTCLK bit reset				
26	Clock frequency, asynchronous [1]		12	25	MHz
27	Clock frequency, synchronous [1]		20	25	MHz
28	Clock high		14.58	0.65 x t_{CP}	ns
29	Clock low (t_{CL})		14.58	0.65 x t_{CP}	ns
	With FASTCLK bit set				
26	Clock frequency, asynchronous [1]		20	40	MHz
27	Clock frequency, synchronous [1]		38	40	MHz
28	Clock high		0.40 x t_{CP}	0.60 x t_{CP}	ns
29	Clock low (t_{CL})		0.40 x t_{CP}	0.60 x t_{CP}	ns
	Asynchronous SCSI				
30	Data setup to $\overline{\text{SCSI\_ACK}}$/$\overline{\text{SCSI\_REQ}}$ low		60	–	ns
31	Data hold from $\overline{\text{SCSI\_REQ}}$ high/$\overline{\text{SCSI\_ACK}}$ low	FIFO is not empty	5	–	ns
32	$\overline{\text{SCSI\_ACK}}$ low to $\overline{\text{SCSI\_REQ}}$ high		–	50	ns
33	SCSI_ACK high to $\overline{\text{SCSI\_REQ}}$ low (data already setup)	FIFO is not full.	–	45	ns
34	$\overline{\text{SCSI\_REQ}}$ high to SCSI_ACK high		–	50	ns
35	$\overline{\text{SCSI\_REQ}}$ low to SCSI_ACK low (data already setup)	FIFO is not full.	–	50	ns
36	Data setup to $\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ low		0	–	ns
37	Data hold from $\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ low		–	18	ns
	Synchronous SCSI - Normal SCSI				
38	Data setup to $\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ low		55	–	ns
39	Data hold from $\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ low		100	–	ns
40	$\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ assertion period		90	–	ns
41	$\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ negation period		90	–	ns
	Synchronous SCSI - Fast SCSI				
38	Data setup to $\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ low		25	–	ns
39	Data hold from $\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ low		35	–	ns
40	$\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ assertion period		30	–	ns
41	$\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ negation period		30	–	ns

AC Characteristics: SCSI TIming (Continued)

Signal #	Parameter	Conditions	Min	Max	Units
	Synchronous SCSI Input Cycle				
42	Data setup to $\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ low		5	–	ns
43	Data hold from $\overline{\text{SCSI\_REQ}}$/$\overline{\text{SCSI\_ACK}}$ low		15	–	ns
44	$\overline{\text{SCSI\_REQ}}$ assertion period		27	–	ns
45	$\overline{\text{SCSI\_REQ}}$ negation period		20	–	ns
46	$\overline{\text{SCSI\_ACK}}$ assertion period		20	–	ns
47	$\overline{\text{SCSI\_ACK}}$ negation period		20	–	ns

1. These minimum numbers are required to comply with ANSI SCSI spec. For Synchronous SCSI data transfers and FASTCLK enabled, the clock inputs must also meet the following requirements: $2t_{CP} + t_{CL} > 97.92$ ns and $2t_{CP} + t_{CH} > 97.92$ ns.

AC Characteristics: Ethernet Timing

Signal #	Parameter	Min	Max	Units
48	ENET_TCLK period	99	101	ns
49	ENET_TCLK high pulse duration	45	–	ns
50	ENET_TCLK low pulse duration	45	–	ns
51	ENET_TCLK rise time	–	8	ns
52	ENET_TCLK fall time	–	8	ns
53	ENET_TENA propagation delay after rising edge of ENET_TCLK	–	25	ns
54	ENET_TENA hold time after ENET_TCLK rising	7	–	ns
55	ENET_TX propagation delay after ENET_TCLK rising	–	32	ns
56	ENET_TX hold time after ENET_TCLK rising	7	–	ns
57	ENET_RCLK period	85	118	ns
58	ENET_RCLK high pulse duration	38	–	ns
59	ENET_RCLK low pulse duration	38	–	ns
60	ENET_RCLK rise time	–	8	ns
61	ENET_RCLK fall time	–	8	ns
62	ENET_RX data rise time	–	8	ns
63	ENET_RX data fall time	–	8	ns
64	ENET_RX data hold time from ENET_RCLK rising	5	–	ns
65	ENET_RX data setup time to ENET_RCLK rising	40	–	ns
66	ENET_RENA low duration	120	–	ns
67	ENET_CLSN high duration	110	–	ns
68	ENET_RENA hold time after the rising edge of ENET_RCLK	1	–	ns
69	ENET_RENA defer before ENET_TENA	356	–	ns
70	ENET_RENA extended after ENET_RCLK last falling	–	275	ns

TIMING DIAGRAMS

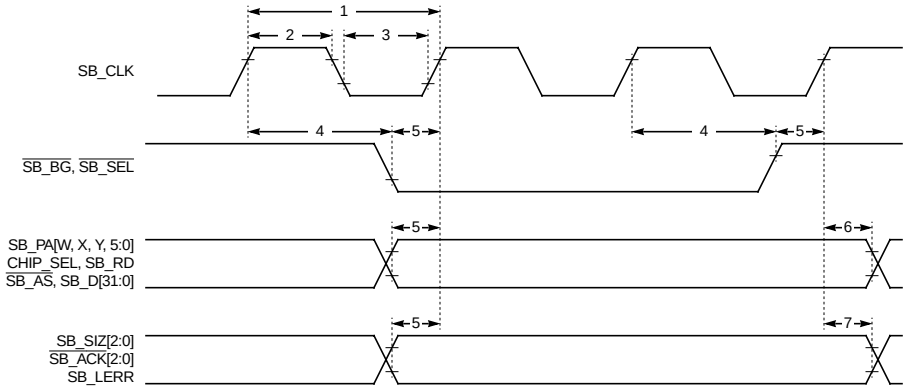


Figure 4. SBus Input Timing

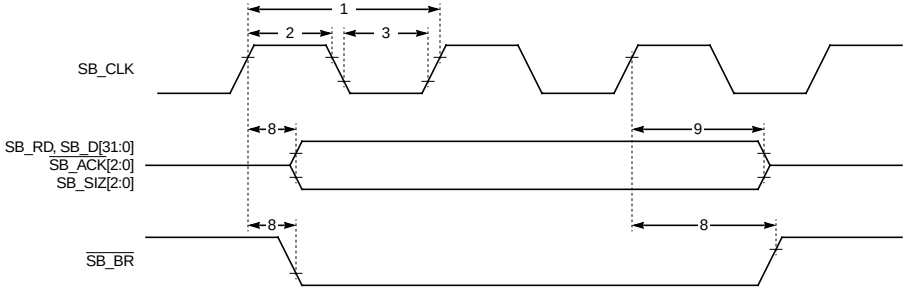


Figure 5. SBus Output Timing

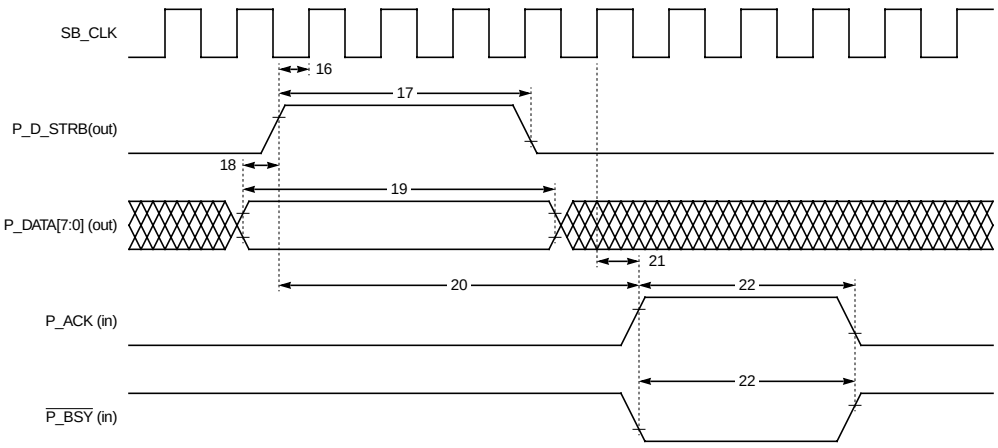


Figure 6. Parallel Port Input Timing

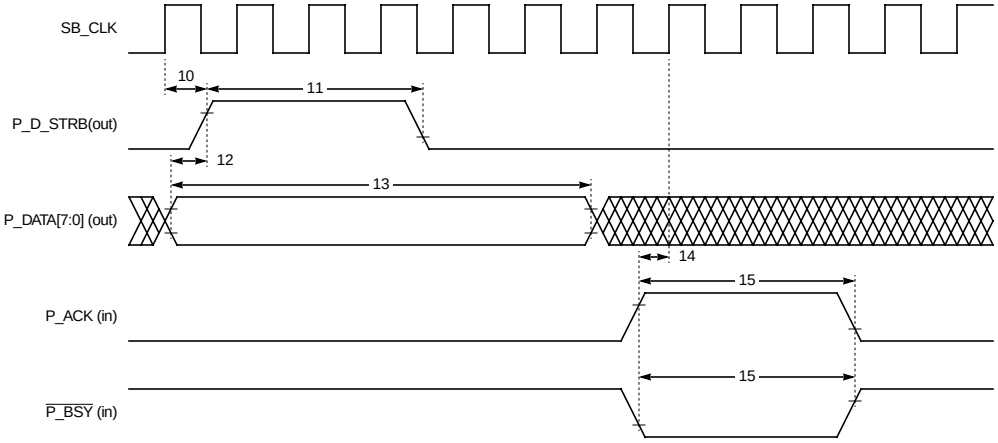


Figure 7. Parallel Port Output Timing

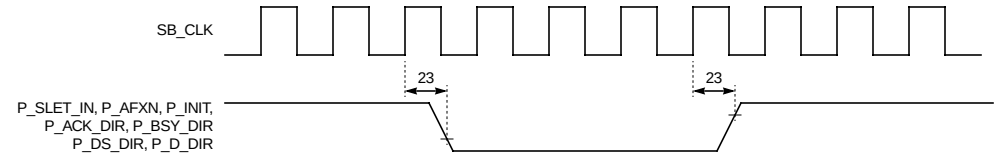


Figure 8. Parallel Port Other Timing

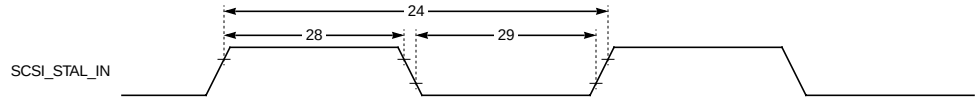


Figure 9. SCSI Clock Timing

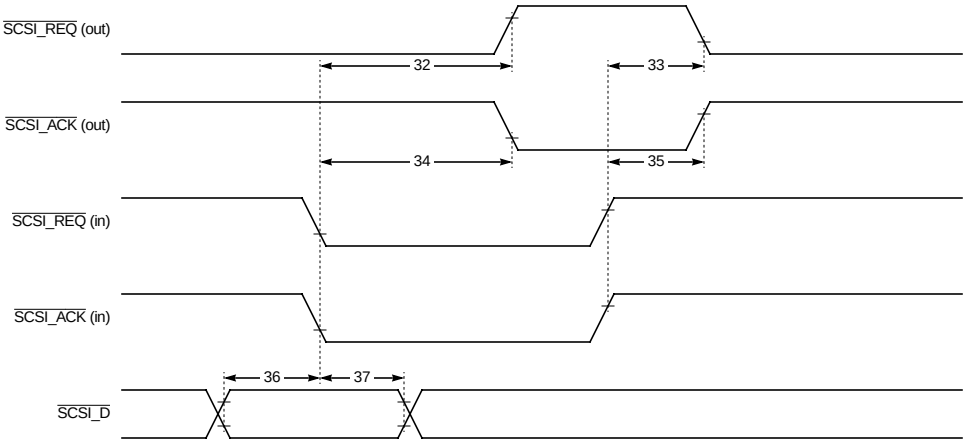


Figure 10. SCSI Asynchronous Input Timing

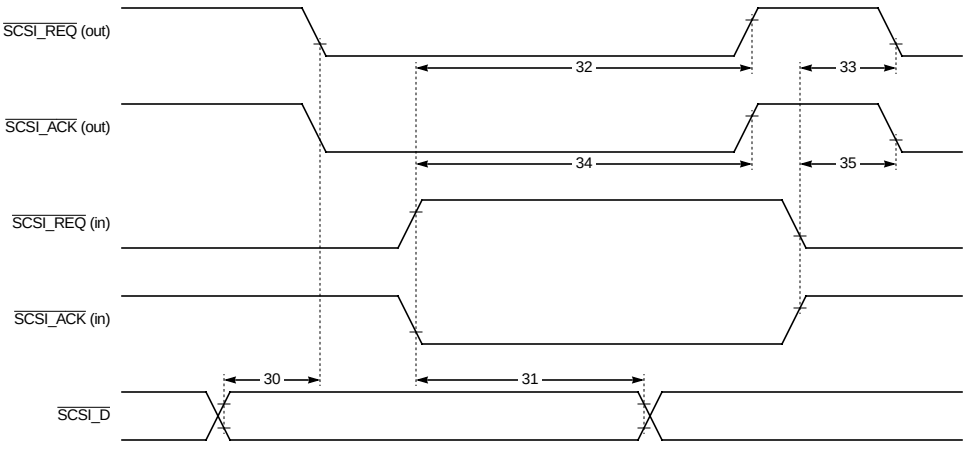


Figure 11. SCSI Asynchronous Output Timing

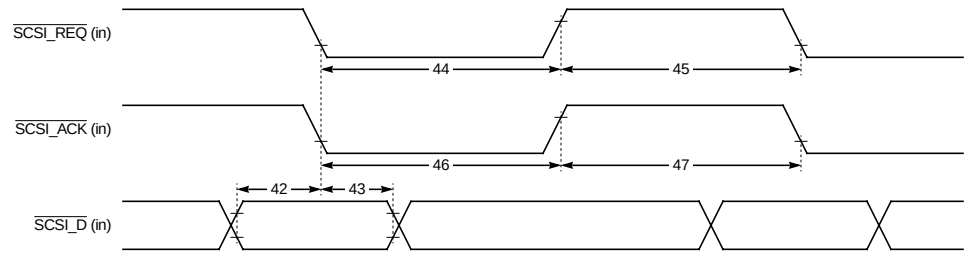


Figure 12. SCSI Synchronous Input Timing

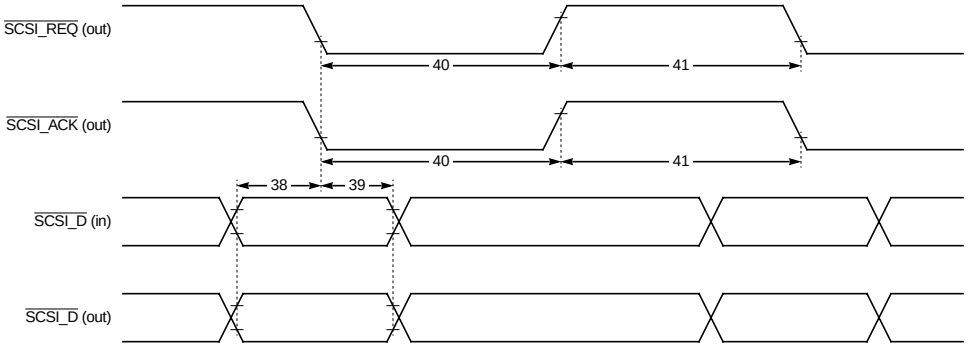


Figure 13. SCSI Synchronous Output Timing

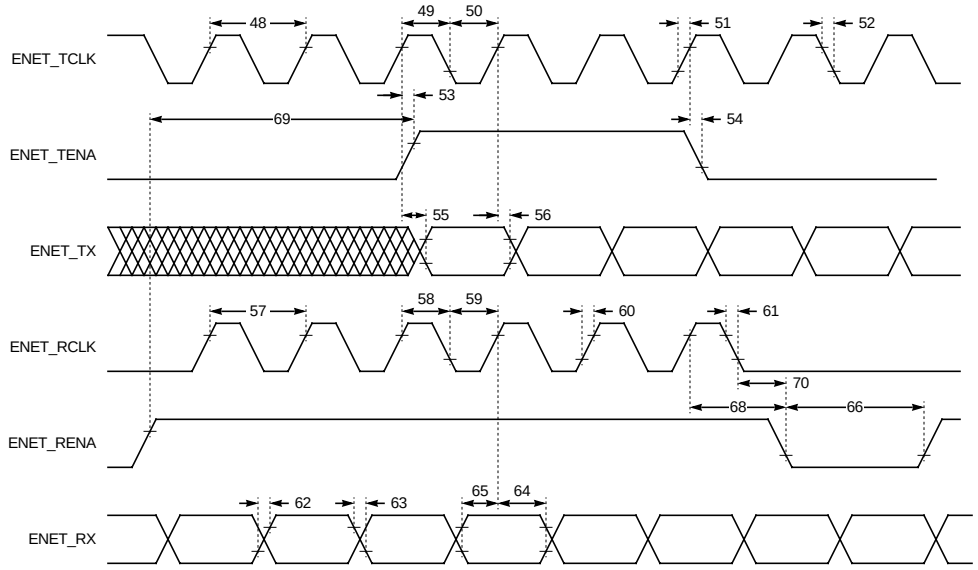


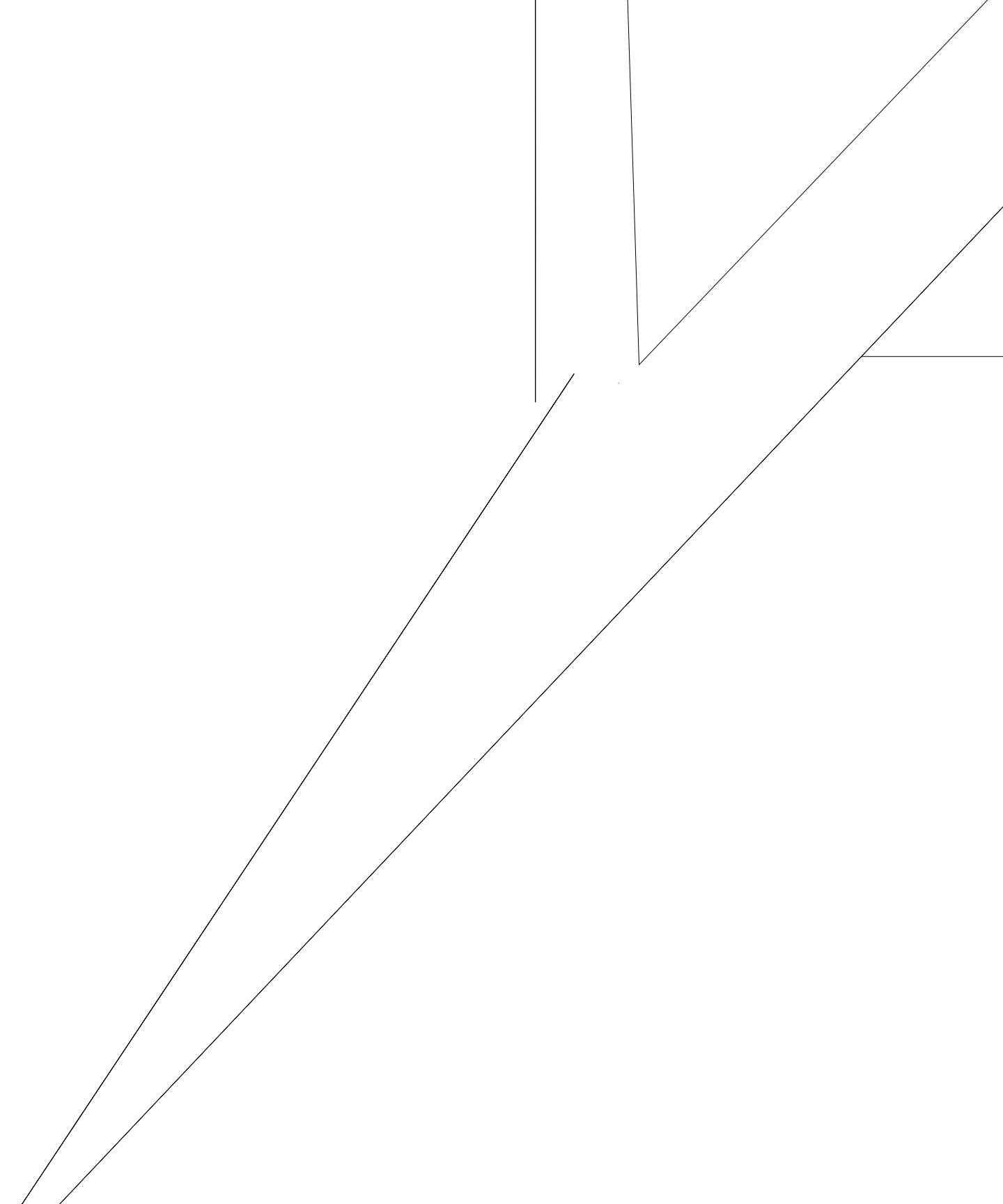
Figure 14. Ethernet Transmit/Receive Timing

Figure 15. Ethernet Collision Timing

PACKAGE INFORMATION

160-Pin PQFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	SB_D[22]	28	P_DATA[5]	55	GND	82	SCSI_SEL	109	SB_D[1]	136	SB_AS
2	SB_D[23]	29	P_DATA[4]	56	ENET_AUI	83	SCSI_BSY	110	SB_D[2]	137	SB_ACK[0]
3	GND	30	GND	57	ENET_TX	84	SCSI_REQ	111	SB_D[3]	138	SB_SIZ[2]
4	SB_D[24]	31	P_DATA[3]	58	ENET_TENA	85	SCSI_ACK	112	GND	139	SB_SIZ[1]
5	SB_D[25]	32	P_DATA[2]	59	ENET_CLSN	86	GND	113	SB_D[4]	140	SB_SIZ[0]
6	SB_D[26]	33	VCC	60	ENET_RX	87	SCSI_MSG	114	VCC	141	VCC
7	VCC	34	P_DATA[1]	61	ENET_RENA	88	SCSI_CD	115	SB_D[5]	142	SB_CLK
8	SB_D[27]	35	P_DATA[0]	62	ENET_TCLK	89	SCSI_IO	116	SB_D[6]	143	GND
9	SB_D[28]	36	GND	63	ENET_RCLK	90	SCSI_ATN	117	GND	144	SB_PA_W
10	SB_D[29]	37	P_ERROR	64	JTAG_TDO	91	SCSI_RST	118	SB_D[7]	145	SB_PA_X
11	SB_D[30]	38	P_SLCT	65	JTAG_CLK	92	GND	119	SB_D[8]	146	SB_P_Y
12	SB_D[31]	39	P_PE	66	JTAG_TDI	93	GND	120	SB_D[9]	147	SB_PA[4]
13	GND	40	P_SLCT_IN	67	JTAG_TMS	94	GND	121	SB_D[10]	148	SB_PA[3]
14	ID_CS	41	P_AFXN	68	JTAG_RST	95	SCSI_XTAL_OUT	122	SB_D[11]	149	SB_PA[2]
15	GND	42	P_INIT	69	GND	96	SCSI_XTAL_IN	123	SB_D[12]	150	SB_PA[1]
16	SB_RESET	43	P_ACK_DIR	70	GND	97	VCC	124	VCC	151	SB_PA[0]
17	VCC	44	P_BSY_DIR	71	SCSI_D[0]	98	VCC	125	SB_D[13]	152	SB_PA[5]
18	SB_P_IRQ	45	P_DS_DIR	72	SCSI_D[1]	99	SCC_20_IN	126	SB_D[14]	153	SB_D[16]
19	SB_E_IRQ	46	P_D_DIR	73	SCSI_D[2]	100	SCC_20_OUT	127	GND	154	SB_D[17]
20	GND	47	GND	74	SCSI_D[3]	101	SCC_CLK20	128	SB_D[15]	155	SB_D[18]
21	P_ACK	48	FPY_CLK24	75	GND	102	GND	129	SB_ACK[2]	156	VCC
22	P_BSY	49	FPY_24_OUT	76	SCSI_D[4]	103	GND	130	SB_ACK[1]	157	SB_D[19]
23	P_D_STRB	50	FPY_24_IN	77	SCSI_D[5]	104	SB_D_IRQ	131	SB_BR	158	GND
24	VCC	51	VCC	78	SCSI_D[6]	105	VCC	132	SB_BG	159	SB_D[20]
25	P_DATA[7]	52	FPY_32_IN	79	SCSI_D[7]	106	SB_RD	133	SB_LERR	160	SB_D[21]
26	P_DATA[6]	53	FPY_32_OUT	80	SCSI_DP	107	GND	134	CHIP_SEL		
27	VCC	54	FPY_CLK32	81	GND	108	SB_D[0]	135	SB_SEL		



ORDERING INFORMATION

Part Number	Description
STP2000QFP	160-Pin Plastic Quad Flat Package (PQFP)

Document Part Number: STP2000