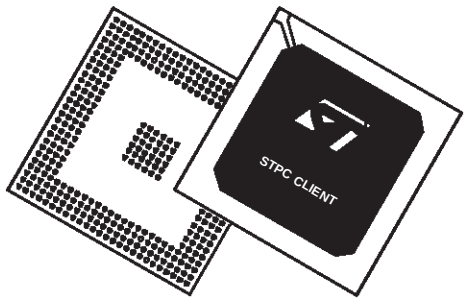
STPC CLIENT

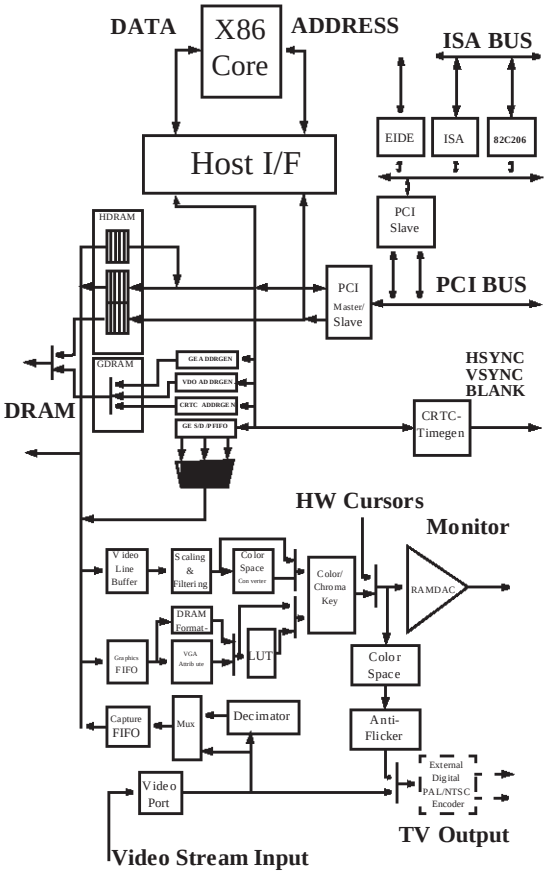
Multimedia PC on a Chip

- POWERFUL X86 PROCESSOR
- 64-BIT 66MHz BUS INTERFACE
- 64-BIT DRAM CONTROLLER
- SVGA GRAPHICS CONTROLLER
- UMA ARCHITECTURE
- VIDEO SCALER
- VIDEO OUTPUT PORT
- VIDEO INPUT PORT
- CRT CONTROLLER
- 135MHz RAMDAC
- 2 OR 3 LINE FLICKER FILTER
- SCAN CONVERTER
- PCI MASTER / SLAVE / ARBITER
- ISA MASTER/SLAVE
- IDE CONTROLLER
- DMA CONTROLLER
- INTERRUPT CONTROLLER
- TIMER / COUNTERS
- POWER MANAGEMENT



PBGA388

Figure 1. Logic Diagram



DESCRIPTION

The STPC Client integrates a fully static x86 processor, fully compatible with standard x86 processors, and combines it with powerful chipset, graphics and video pipelines to provide a single Consumer orientated PC compatible subsystem on a single device. The device is packaged in a 388 Ball Grid Array (PBGA).

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8Kbyte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.

- Clock core speeds up to of 133 MHz.
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 3.3V operation.

- **DRAM Controller**
- Integrated system memory and graphic frame memory.
- Supports up to 128 MBytes system memory in 4 banks and as little as 2Mbytes.
- Supports 4MB, 8MB, 16MB, 32MB single-sided and double-sided DRAM SIMMs.
- Four quad-word write buffers for CPU to DRAM and PCI to DRAM cycles.
- Four 4-word read buffers for PCI masters.
- Supports Fast Page Mode & EDO DRAMs.
- Programmable timing for DRAM parameters including CAS pulse width, CAS pre-charge time, and RAS to CAS delay.
- 60, 70, 80 & 100ns DRAM speeds.
- Memory hole between 1 MByte & 8 MByte supported for PCI/ISA busses.
- Hidden refresh.

- **Graphics Controller**
- 64-bit windows accelerator.
- Backward compatibility to SVGA standards.
- Hardware acceleration for text, bitblts, transparent blts and fills.
- Up to 64 x 64 bit graphics hardware cursor.
- Up to 4MB long linear frame buffer.
- 8-, 16-, and 24-bit pixels.
- Drivers for Windows and other operating systems.

- **CRT Controller**
- Integrated 135MHz triple RAMDAC allowing for 1024 x 768 x 75Hz display.
- Requires external frequency synthesizer and reference sources.
- 8-, 16-, 24-bit pixels.
- Interlaced or non-interlaced output.

- **Video Pipeline**
- Two-tap interpolative horizontal filter.
- Two-tap interpolative vertical filter.
- Color space conversion (RGB to YUV and YUV to RGB).
- Programmable window size.
- Chroma and color keying for integrated video overlay.
- Programmable two tap filter with gamma correction or three tap flicker filter.
- Progressive to interlaced scan converter.

- **Video Input port**
- Accepts video inputs in CCIR 601/656 or ITU-R 601/656, and decodes the stream.
- Optional 2:1 decimator
- Stores captured video in off setting area of the onboard frame buffer.
- Video pass through to the onboard PAL/ NTSC encoder for full screen video images.
- HSYNC and B/T generation or lock onto external video timing source.

- **PCI Controller**
- Fully compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External PAL allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- 0.33X and 0.5X CPU clock PCI clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/ O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus. NSP compliant.

- **IDE Interface**
- Supports PIO and Bus Master IDE
- Supports up to Mode 5 Timings
- Transfer Rates to 22 MBytes/sec
- Supports up to 4 IDE devices
- Concurrent channel operation (PIO & DMA modes) - 4 x 32-Bit Buffer FIFO per channel
- Support for PIO mode 3 & 4.
- Support for DMA mode 1 & 2.
- Support for 11.1/16.6 MB/s, I/O Channel Ready PIO data transfers.
- Supports 13.3/16.6 MB/s DMA data transfers
- Bus Master with scatter/gather capability
- Multi-word DMA support for fast IDE drives
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Supports hard drives larger than 528MB
- Support for CD-ROM and tape peripherals
- Backward compatibility with IDE (ATA-1).
- Drivers for Windows and other OSes

- **Integrated peripheral controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports SMM and APM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel ports.
- Slow system clock down to 8MHz
- Slow Host clock down to 8Hz
- Slow graphic clock down to 8Hz
- Supports RTC, interrupts and DMAs wake-up

1 GENERAL DESCRIPTION

At the heart of the STPC Client is an advanced processor block, dubbed the 5ST86. The 5ST86 includes a powerful x86 processor core along with a 64-bit DRAM controller, advanced 64bit accelerated graphics and video controller, a high speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA bus) and EIDE controller.

The STPC Client has in addition to the 5ST86 a Video subsystem and high quality digital Television output.

The STMicroelectronics x86 processor core is embedded with standard and application specific peripheral modules on the same silicon die. The core has all the functionality of the SGS-THOMSON standard x86 processor products, including the low power System Management Mode (SMM).

System Management Mode (SMM) provides an additional interrupt and address space that can be used for system power management or software transparent emulation of peripherals. While running in isolated SMM address space, the SMM interrupt routine can execute without interfering with the operating system or application programs.

Further power management facilities include a suspend mode that can be initiated from either hardware or software. Because of the static nature of the core, no internal data is lost.

The STPC Client makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This significantly reduces total system memory with system performances equal to that of a comparable solution with separate frame buffer and system memory. In addition, memory bandwidth is improved by attaching the graphics engine directly to the 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus.

The 64-bit wide memory array provides the system with 320MB/s peak bandwidth, double that of an equivalent system using 32 bits. This allows for higher screen resolutions and greater color depth. The processor bus runs at the speed of the processor (DX devices) or half the speed (DX2 devices).

The ‘standard’ PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated with the x86 processor core.

The PCI bus is the main data communication link to the STPC Client chip. The STPC Client translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports generation of Configuration cycles on the PCI bus. The STPC Client, as a PCI bus agent (host bridge class), fully complies with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

The STPC Client integrates an ISA bus controller. Peripheral modules such as parallel and serial communications ports, keyboard controllers and additional ISA devices can be accessed by the STPC Client chip set through this bus.

An industry standard EIDE (ATA 2) controller is built in to the STPC Client and connected internally via the PCI bus.

Graphics functions are controlled by the on-chip SVGA controller and the monitor display is managed bythe 2D graphics display engine.

This Graphics Engine is tuned to work with the host CPU to provide a balanced graphics system with a low silicon area cost. It performs limited graphics drawing operations, which include hardware acceleration of text, bitblts, transparent blts and fills. These operations can operate on off-screen or on-screen areas. The frame buffer size is up to 4 Mbytes anywhere in the physical main memory.

The graphics resolution supported is a maximum of 1280x1024 in 65536 colours at 75Hz refresh rate and is VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to accommodate above display resolution.

STPC Client provides several additional functions to handle MPEG or similar video streams. The Video Input Port accepts an encoded digital video stream in one of a number of industry standard formats, decodes it, optionally decimates it by a factor of 2:1, and deposits it into an off screen area of the frame buffer. An interrupt request can be generated when an entire field or frame has been captured.

The video output pipeline incorporates a video-scaler and color space converter function and provisions in the CRT controller to display a video window. While repainting the screen the CRT controller fetches both the video as well as the normal non-video frame buffer in two separate internal FIFOs (256-bytes each). The video stream can be color-space converted (optionally) and smooth scaled. Smooth interpolative scaling in both horizontal and vertical direction are implemented. Color and Chroma key functions are also implemented to allow mixing video stream with non-video frame buffer.

The video output passes directly to the RAMDAC for monitor output or through another optional color space converter (RGB to 4:2:2 YCrCb) to the programmable anti-flicker filter. The flicker filter is configured as either a two line filter with gamma correction (primarily designed for DOS type text) or a 3 line flicker filter (primarily designed for Windows type displays). The flicker filter is optional and can be software disabled for use with large screen area's of video.

The Video output pipeline of the STPC Client interfaces directly to the external digital TV encoder (STV0119). It takes a 24 bit RGB non-interlaced pixel stream and converts to a multiplexed 4:2:2 YCrCb 8 bit output stream, the logic includes a progressive to interlaced scan converter and logic to insert appropriate CCIR656 timing reference codes into the output stream. It facilitates the high quality display of VGA or full screen video streams received via the Video input port to standard NTSC or PAL televisions.

The STPC Client core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit module (PMU) controls the power consumption by providing a comprehensive set of features that control the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides following hardware structures to assist the software in managing the power consumption by the system.

- System Activity Detection.

- 3 power-down timers detecting system inactivity:

  - Doze timer (short durations).
  - Stand-by timer (medium durations).
  - Suspend timer (long durations).

- House-keeping activity detection.

- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.

- Peripheral activity detection.

- Peripheral timer detecting peripheral inactivity

- SUSP# modulation to adjust the system performance in various power down states of the system including full power on state.

- Power control outputs to disable power from different planes of the board.

Lack of system activity for progressively longer period of times is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate SMI interrupt to allow the software to bring the system back up to full power on state. The chip-set supports up to three power down states: Doze state, Stand-by state and Suspend mode. These correspond to decreasing levels of power savings.

Power down puts the STPC Client into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. removing power down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped.

A reference design for the STPC Client is available including the schematics and layout files, the design is a PC ATX motherboard design. The design is available as a demonstration board for application and system development.

The STPC Client is supported by several BIOS vendors, including the super I/O device used in the reference design. Drivers for 2D accelerator, video features and EIDE are availaible on various operating systems.

The STPC Client has been designed using modern reusable modular design techniques, it is possible to add to or remove the standard features of the STPC Client or other variants of the 5ST86 family. Contact your local STMicroelectonics sales office for further information.

Figure 2. Interfaces

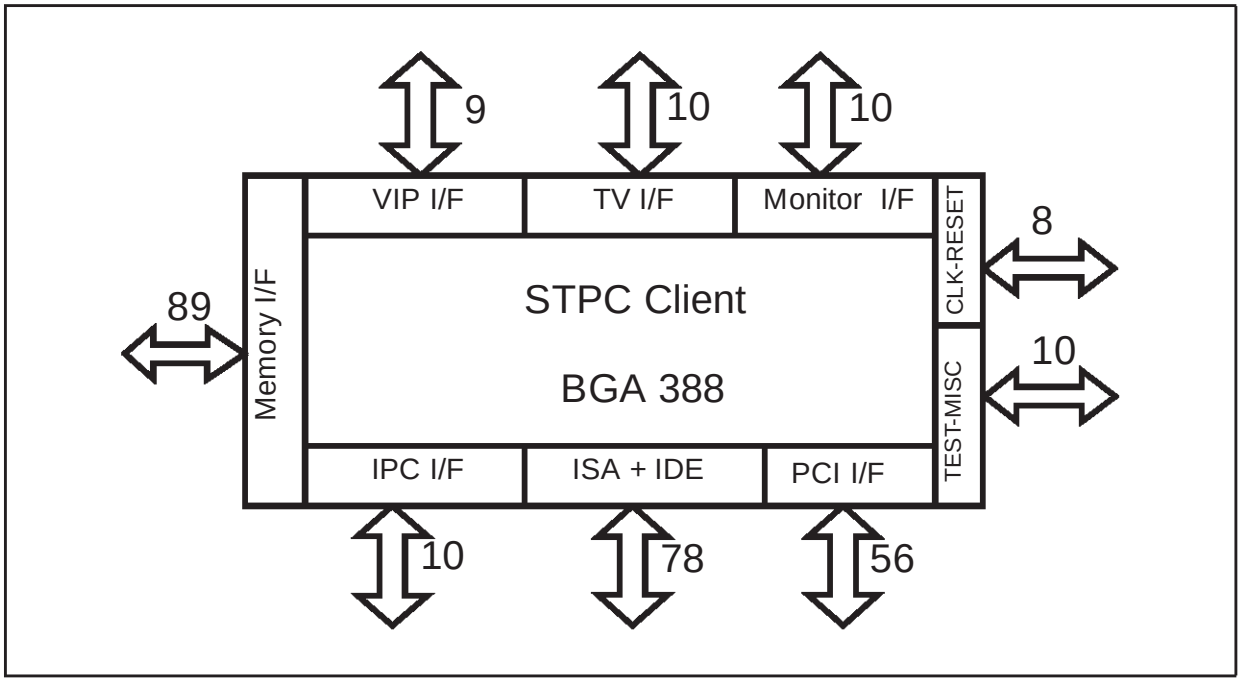


Figure 3. Die Highlight

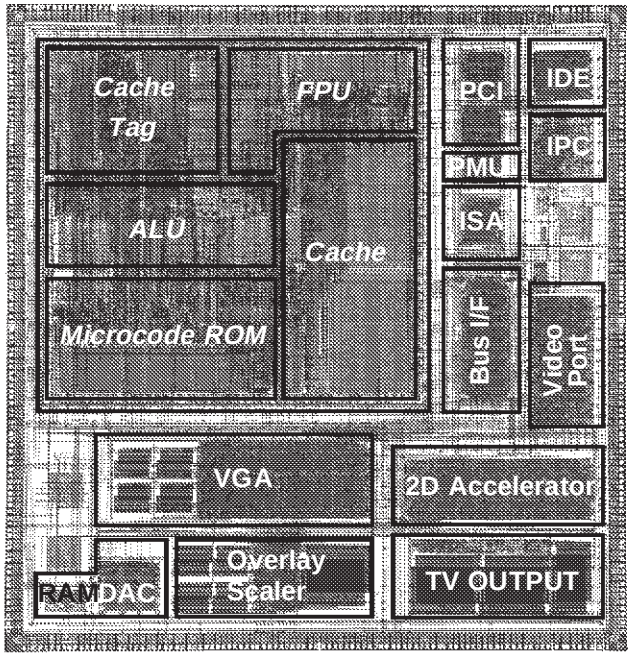


Figure 4. Functionnal description.

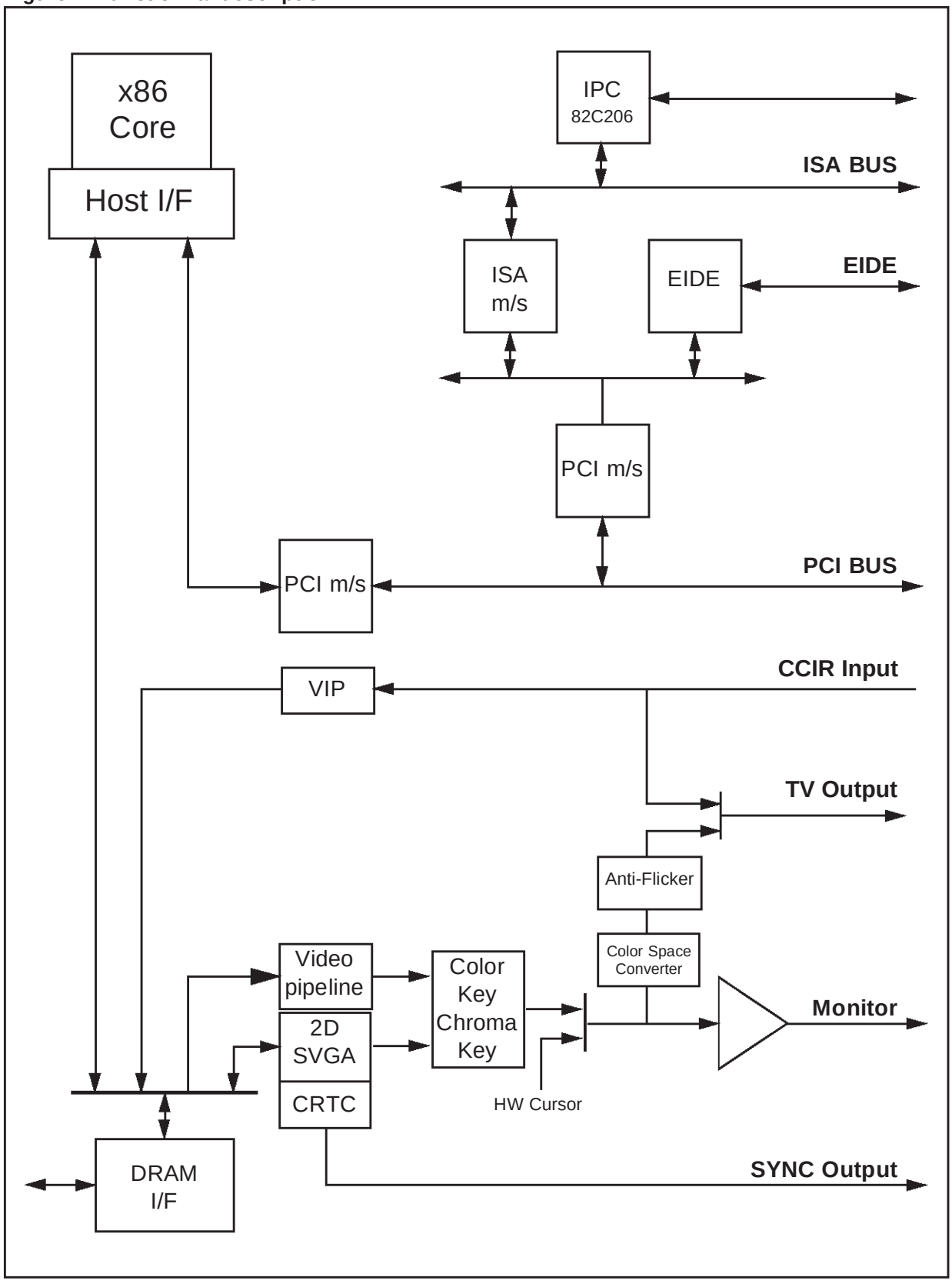


Figure 5. Pictorial Block Diagram

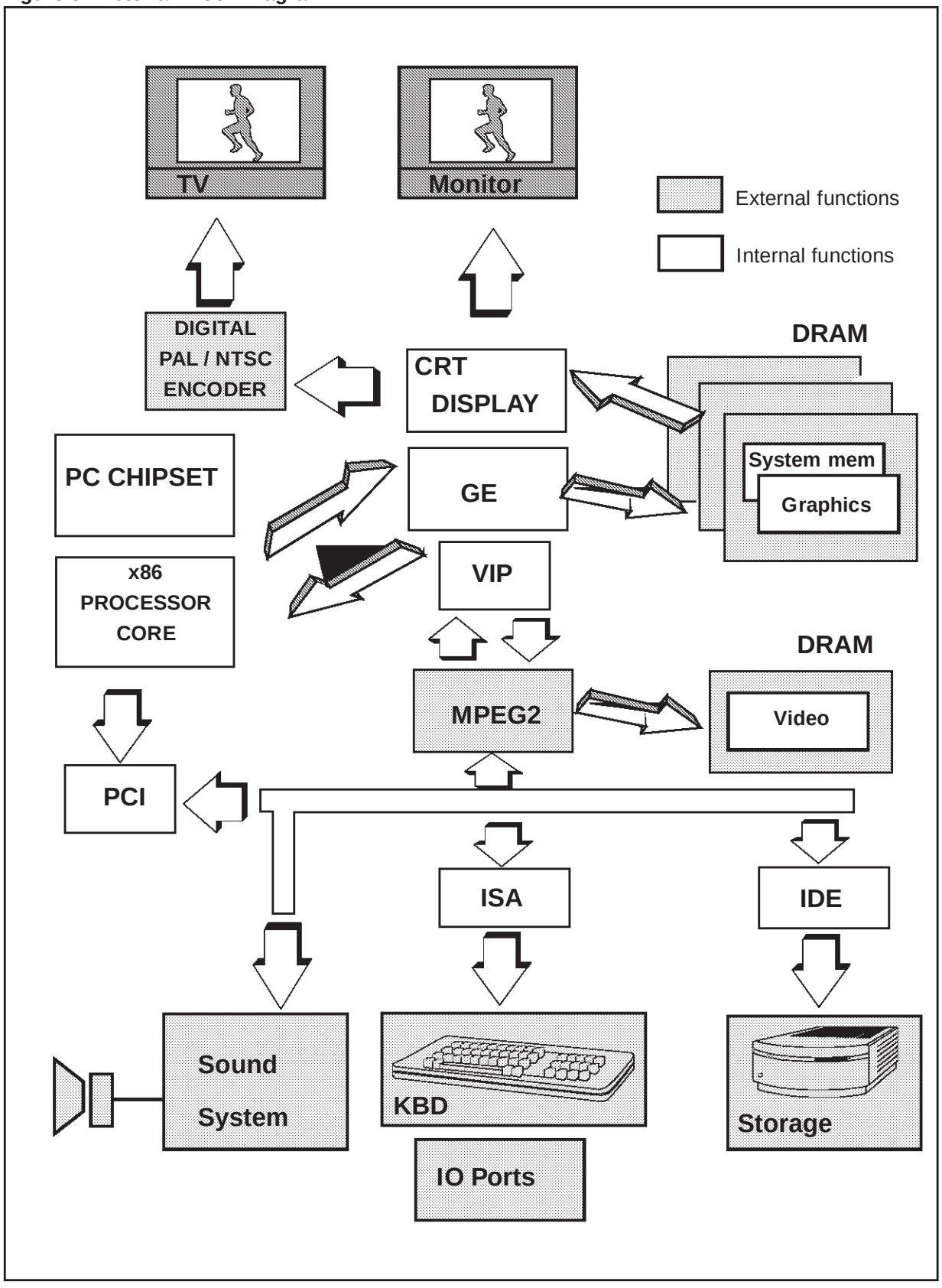
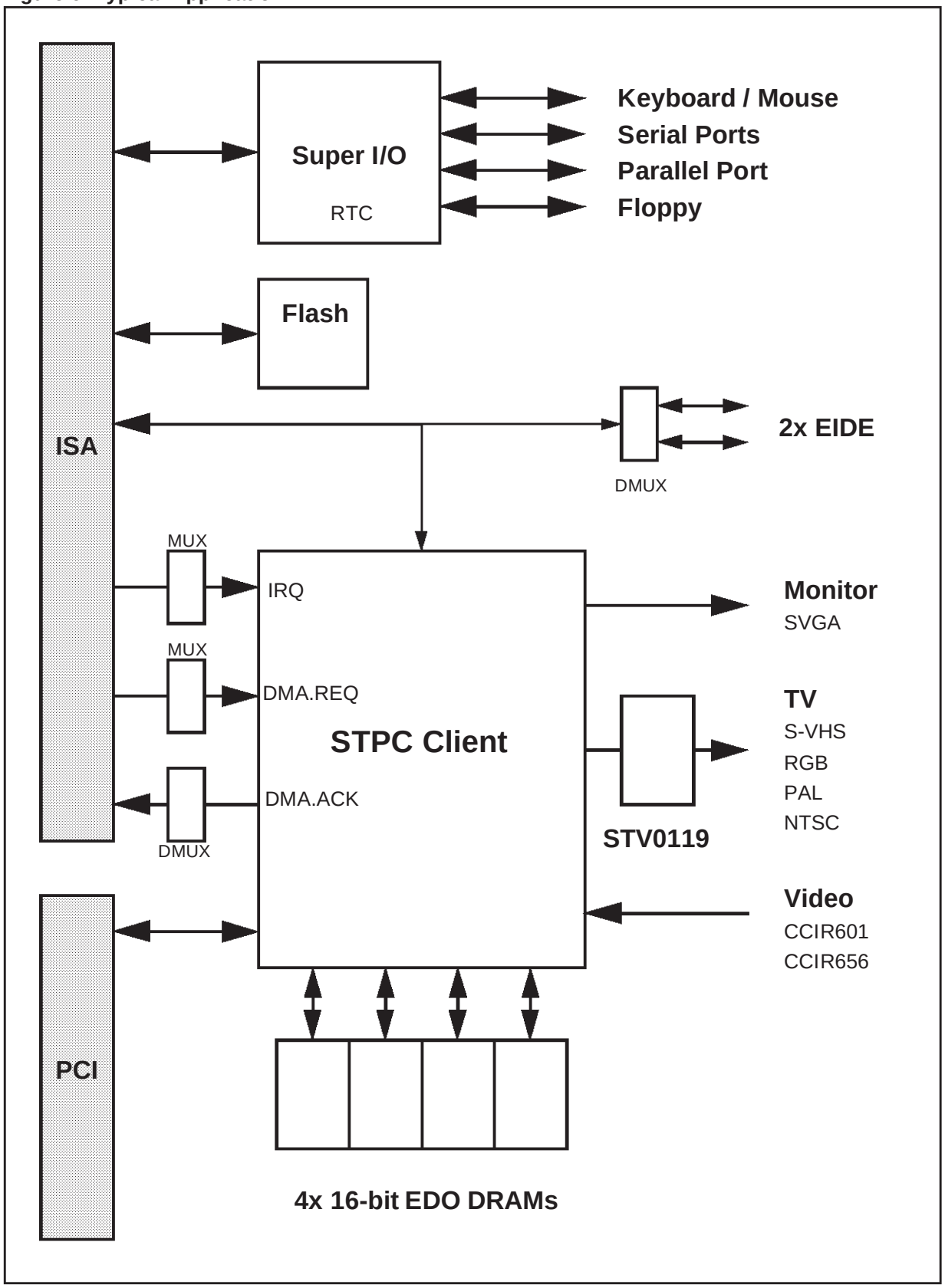


Figure 6. Typical Application



2 PIN DESCRIPTION

2.1 INTRODUCTION

The STPC Client integrates most of the functionalities of the PC architecture. As a result, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the STPC Client. This offers improved performance due to the tight coupling of the processor core and these peripherals. As a result many of the external pin connections are made directly to the on-chip peripheralfunctions.

Figure 7 shows the STPC Client's external interfaces. It defines the main busses and their function. Table 1 describes the physical implementation listing signals type and their functionality. Table 2 provides a full pin listing and description of pins. Table 3 provides a full listing of pin locations of the STPC Client package by physical connection. Please refer to the pin allocation drawing for reference.

Table 1. Signal Description

Group name	Qty
Basic Clocks reset & Xtal	7
Memory Interface	89
PCI interface	56
ISA / IDE / IPC combined interface	88
Video Input	9
Video Output	10
VGA Monitor interface	10
Grounds	69
V_{DD}	24
Analog specific V_{CC}/V_{DD}	16
Reserved	10
Total Pin Count	388

Note: Several interface pins are multiplexed with other functions, refer to the Pin Description section for further details

Figure 7. PC Client External Interfaces

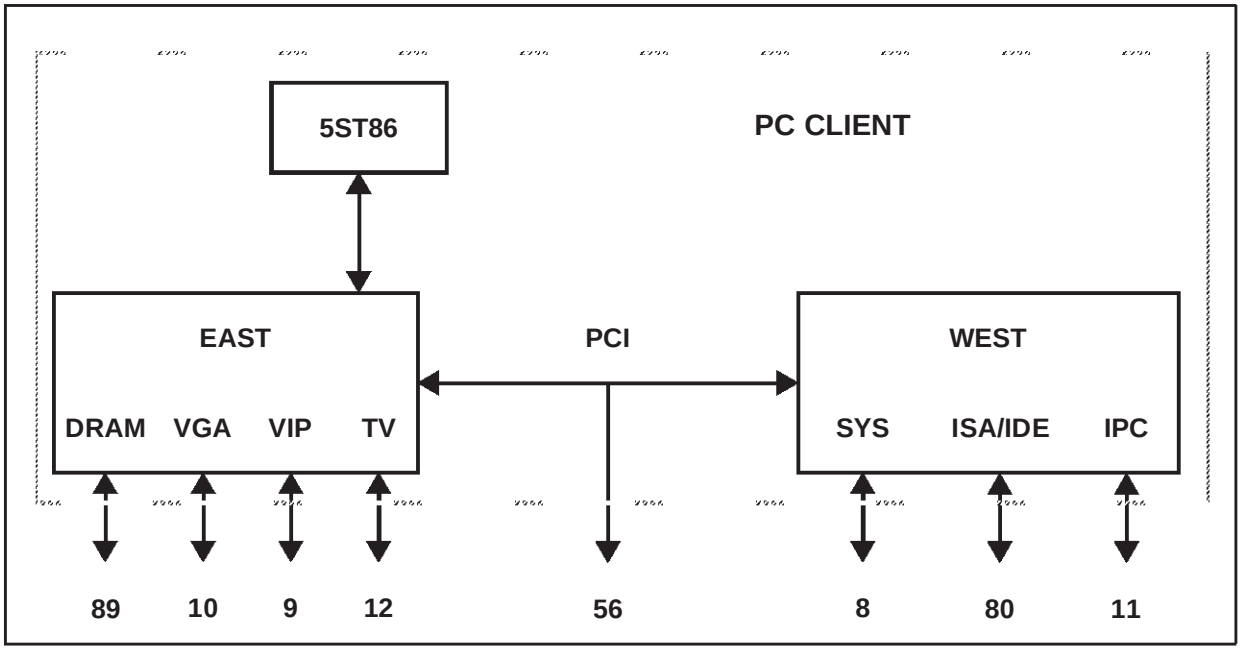


Table 2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
BASIC CLOCKS AND RESETS			
PWERGD	I	System Reset / Power good	1
XTALI	I	14.3MHz Crystal Input	1
XTALO	I/O	14.3MHz Crystal Output - External Oscillator Input	1
HCLK	O	Host Clock (Test)	1
DEV_CLK	O	24MHz Peripheral Clock (floppy drive)	1
GCLK2X	I/O	80MHz Graphics Clock	1
DCLK	I/O	135MHz Dot Clock	1
DCLK _DIR	I	Dot Clock Direction	1
MEMORY INTERFACE			
MA[11:0]	I/O	Memory Address	12
RAS#[3:0]	O	Row Address Strobe	4
CAS#[7:0]	O	Column Address Strobe	8
MWE#	O	Write Enable	1
MD[63:0]	I/O	Memory Data	64
PCI INTERFACE			
PCI_CLKI	I	33MHz PCI Input Clock	1
PCI_CLKO	O	33MHz PCI Output Clock (from internal PLL)	1
AD[31:0]	I/O	PCI Address / Data	32
CBE[3:0]	I/O	Bus Commands / Byte Enables	4
FRAME#	I/O	Cycle Frame	1
TRDY#	I/O	Target Ready	1
IRDY#	I/O	Initiator Ready	1
STOP#	I/O	Stop Transaction	1
DEVSEL#	I/O	Device Select	1
PAR	I/O	Parity Signal Transactions	1
SERR#	O	System Error	1
LOCK#	I	PCI Lock	1
PCIREQ#[2:0]	I	PCI Request	3
PCIGNT#[2:0]	O	PCI Grant	3
PCI_INT[3:0]	I	PCI Interrupt Request	4
ISA AND IDE COMBINED ADDRESS/DATA			
LA[23:22] / SCS3#,SCS1#	I/O	Unlatched Address (ISA) / Secondary Chip Select (IDE)	2
LA[21:20] / PCS3#,PCS1#	I/O	Unlatched Address (ISA) / Primary Chip Select (IDE)	2
LA[19:17] / DA[2:0]	O	Unlatched Address (ISA) / Address (IDE)	3
RMRTCCS# / DD[15]	I/O	ROM/RTC Chip Select / Data Bus bit 15 (IDE)	1
KBCS# / DD[14]	I/O	Keyboard Chip Select / Data Bus bit 14 (IDE)	1
RTCRW# / DD[13]	I/O	RTC Read/Write / Data Bus bit 13 (IDE)	1
RTCDS# / DD[12]	I/O	RTC Data Strobe / Data Bus bit 12 (IDE)	1
SA[19:8] / DD[11:0]	I/O	Latched Address (ISA) / Data Bus (IDE)	16
SA[7:0]	I/O	Latched Address (IDE)	4
SD[15:0]	I/O	Data Bus (ISA)	16
ISA/IDE COMBINED CONTROL			
IOCHRDY / DIORDY	I/O	I/O Channel Ready (ISA) - Busy/Ready (IDE)	1

PIN DESCRIPTION

Table 2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
ISA CONTROL			
SYSRSTO#	O	Reset Output to System	1
ISA_CLK	O	ISA Clock Output - Multiplexer Select Line For IPC	1
ISA_CLK2X	O	ISA Clock x 2 Output - Multiplexer Select Line For IPC	1
OSC14M	O	ISA bus synchronisation clock	1
ALE	O	Address Latch Enable	1
BHE#	I/O	System Bus High Enable	1
MEMR#, MEMW#	I/O	Memory Read and Memory Write	2
SMEMR#, SMEMW#	O	System Memory Read and Memory Write	2
IOR#, IOW#	I/O	I/O Read and Write	2
MASTER#	I	Add On Card Owns Bus	1
MCS16#, IOCS16#	I	Memory/IO Chip Select16	2
REF#	O	Refresh Cycle.	1
AEN	O	Address Enable	1
IOCHCK#	I	I/O Channel Check.	1
ISAOE#	O	Bidirectional OE Control	1
GPIOCS#	I/O	General Purpose Chip Select	1
IDE CONTROL			
PIRQ	I	Primary Interrupt Request	1
SIRQ	I	Secondary Interrupt Request	1
PDRQ	I	Primary DMA Request	1
SDRQ	I	Secondary DMA Request	1
PDACK#	O	Primary DMA Acknowledge	1
SDACK#	O	Secondary DMA Acknowledge	1
PIOR#	I/O	Primary I/O Read	1
PIOW#	O	Primary I/O Write	1
SIOR#	I/O	Secondary I/O Read	1
SIOW#	O	Secondary I/O Write	1
IPC			
IRQ_MUX[3:0]	I	Multiplexed Interrupt Request	4
DREQ_MUX[1:0]	I	Multiplexed DMA Request	2
DACK_ENC[2:0]	O	DMA Acknowledge	3
TC	O	ISA Terminal Count	1
MONITOR INTERFACE			
RED, GREEN, BLUE	O	Red, Green, Blue	3
VSYNC	O	Vertical Sync	1
HSYNC	O	Horizontal Sync	1
VREF_DAC	I	DAC Voltage reference	1
RSET	I	Resistor Set	1
COMP	I	Compensation	1
DDC[1:0]	I/O	Display Data Channel Serial Link	2
VIDEO INPUT			
VCLK	I	Pixel Clock	1
VIN	I	YUV Video Data Input CCIR 601 or 656	8

Table 2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
DIGITAL TV OUTPUT			
TV_YUV[7:0]	O	Digital Video Outputs	8
VTV_BT#	O	Frame Synchronisation	1
VTV_HSYNC	O	Horizontal Line Synchronisation	1
MISCELLANEOUS			
ST[6:0]	I/O	Reserved (Test/Misc pins)	7
CLKDEL[2:0]	I/O	Reserved (Test/Misc pins)	3

2.2 SIGNAL DESCRIPTIONS

2.2.1 BASIC CLOCKS AND RESETS

PWGD *System Reset/Power good.* This input is low when the the reset switch is depressed. Otherwise, it reflects the power supply's power good signal. PWGD is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of PWGD.

SYSRSTO# *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output.

XTALI *14.3MHz Crystal Input*
XTALO *14.3MHz Crystal Output.* These pins are the 14.318 MHz crystal input; This clock is used as the reference clock for the internal frequency synthesizer to generate the HCLK, CLK24M, GCLK2X and DCLK clocks.
A 14.318 MHz Series Cut Quartz Crystal should be connected between these two pins. Balance capacitors of 15 pF should also be added. In the event of an external oscillator providing the master clock signal to the STPC Client device, the TTL signal should be provided on XTALO.

HCLK *Host Clock.* This is the host 1X clock. Its frequency can vary from 25 to 75 MHz. All host transactions and PCI transactions are synchronized to this clock. The DRAM controller to execute the host transactions is also driven by this clock. In normal mode, this output clock is generated by the internal pll.

PCI_CLKI *33MHz PCI Input Clock*

This signal is the PCI bus clock input and should be driven from the PCI_CLKO pin.

PCI_CLKO *33MHz PCI Output Clock.* This is the master PCI bus clock output.

GCLK2X *80MHz Graphics Clock.* This is the Graphics 2X clock, which drives the graphics engine and the the DRAM controller to execute the graphics and display cycles.
Normally GCLK2X is generated by the internal frequency synthesizer, and this pin is an output. By setting a bit in Strap Register 2, this pin can be made an input so that an external clock can replace the internal frequency synthesizer.

DCLK *135MHz Dot Clock.* This is the dot clock, which drives graphics display cycles. Its frequency can be as high as 135 MHz, and it is required to have a worst case duty cycle of 60-40.
This signal is either driven by the internal pll (VGA) either by an external 27MHz oscillator (TV). The direction can be controlled by a strap option or an internal register bit.

DCLK_DIR *Dot Clock Direction.* Specify if DCLK is an input (0) or an output (1).

ISA_CLK *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces the Clock signal for the ISA bus. It is also used with ISA_CLK2X as the multiplexor control lines for the Interrupt Controller Interrupt input lines. This is divided down version of either the PCICLK or OSC14M.

ISA_CLKX2 *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces a signal at twice the frequency of the Clock signal for the ISA bus. It is also used with ISA_CLK as the multiplexor control lines for the Interrupt Controller Interrupt input lines.

DEV_CLK *24MHz Peripheral Clock Output.* This 24MHZ signal is provided as a convenience for the system integration of a Floppy Disk driver function in an external chip.

OSC14M *ISA bus synchronisation clock Output.* This is the buffered 14.318 Mhz clock to the ISA bus.

2.2.2 MEMORY INTERFACE

MA[11:0] *Memory Address Output.* These 12 multiplexed memory address pins support external DRAM with up to 4K refresh. These include all 16M x N and some 4M x N DRAM modules. The address signals must be externally buffered to support more than 16 DRAM chips. The timing of these signals can be adjusted by software to match the timings of most DRAM modules.

MD[63:0] *Memory Data I/O.* This is the 64-bit memory data bus. If only half of a bank is populated, MD63-32 is pulled high, data is on MD31-0.
MD[40-0] are read by the device strap option registers during rising edge of PWGD.

RAS#[3:0] *Row Address Strobe Output.* There are 4 active low row address strobe outputs, one each for each bank of the memory. Each bank contains 4 or 8-bytes of data. The memory controller allows half of a bank (4-bytes) to be populated to enable memory upgrade at finer granularity.
The RAS# signals drive the SIMMs directly without any external buffering. These pins are always outputs, but they can also simultaneously be inputs, to allow the memory controller to monitor the value of the RAS# signals at the pins.

CAS#[7:0] *Column Address Strobe Output.*There are 8 active low column address strobe outputs, one each for each byte of the memory.
The CAS# signals drive the SIMMs either directly or through external buffers.
These pins are always outputs, but they can also simultaneously be inputs, to allow the memory controller to monitor the value of the CAS# signals at the pins.

MWE# *Write Enable Output.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L). This single write enable controls all DRAMs. It can be externally buffered to boost the maximum number of loads (DRAM chips) supported.
The MWE# signals drive the SIMMs directly without any external buffering.

2.2.3 VIDEO INTERFACE

VIDEO_CLK *Pixel Clock Input.*

VIDEO_D[7:0] *YUV Video Data Input CCIR 601 or 656.* Time multiplexed 4:2:2 luminance and chrominance data as defined in ITU-R Rec601-2 and Rec656 (except for TTL input levels). This bus interfaces with an MPEG video decoder output port and typically carries a stream of Cb,Y,Cr,Y digital video at VCLK frequency, clocked on the rising edge (by default) of VCLK. A 54-Mbit/s 'double' Cb, Y, Cr, Y input multiplex is supported for double encoding application (rising and falling edge of CKREF are operating).

2.2.4 TV OUTPUT

TV_YUV[7:0] *Digital video outputs.*

VTV_BT# *Frame Synchronisation.*

VTV_HSYNC *Horizontal Line Synchronisation.*

2.2.5 PCI INTERFACE

AD[31:0] *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions.

CBE#[3:0] *Bus Commands/Byte Enables.* These are the multiplexed command and byte enable signals of the PCI bus. During the address phase they define the command and during the data phase they carry the byte enable information. These pins are inputs when a PCI master other than the STPC Client owns the bus and outputs when the STPC Client owns the bus.

FRAME# *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when STPC Client owns the PCI bus.

TRDY# *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the STPC Client is the target of the current bus transaction. It is used as an input when STPC Client initiates a cycle on the PCI bus.

IRDY# *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the STPC Client initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the STPC Client to determine when the current PCI master is ready to complete the current transaction.

STOP# *Stop Transaction.* Stop is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for the bus cycles initiated by the STPC Client and is used as an output when a PCI master cycle is targeted to the STPC Client.

DEVSEL# *I/O Device Select.* This signal is used as an input when the STPC Client initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output either when the STPC Client is the target of the current PCI transaction or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

PAR *Parity Signal Transactions.* This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE#[3:0], and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions. (Its assertion is identical to that of the AD bus delayed by one PCI clock cycle)

SERR# *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a STPC Client initiated PCI transaction. Its assertion by either the STPC Client or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

LOCK# *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

PCIREQ#[2:0] *PCI Request.* This pin are the three external PCI master request pins. They indicates to the PCI arbiter that the external agents desire use of the bus.

PCIGNT#[2:0] *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it on its PCIREQ#.

2.2.6 ISA/IDE COMBINED ADDRESS/DATA

LA[23]/SCS3# *Unlatched Address (ISA)/Secondary Chip Select (IDE).* This pin has two functions, depending on whether the ISA bus is active or the IDE bus is active.
When the ISA bus is active, this pins is ISA Bus unlatched address bit 23 for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, this pin is in output mode. When an ISA bus master owns the bus, this pins is in input mode.
When the IDE bus is active, this signals is used as the active high secondary slave IDE chip select signal. This signal is to be externally NANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

LA[22]/SCS1# *Unlatched Address (ISA)/Secondary Chip Select (IDE)*

This pin has two functions, depending on whether the ISA bus is active or the IDE bus is active.
When the ISA bus is active, this pins is ISA Bus unlatched address bit 22 for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, this pin is in output mode. When an ISA bus master owns the bus, this pins is in input mode.
When the IDE bus is active, this signals is used as the active high secondary slave IDE chip select signal. This signal is to be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

LA[21]/PCS3# *Unlatched Address (ISA)/Primary Chip Select (IDE).* This pin has two functions, depending on whether the ISA bus is active or the IDE bus is active.
When the ISA bus is active, this pins is ISA Bus unlatched address bit 21 for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, this pin is in output mode. When an ISA-bus master owns the bus, this pins is in input mode.
When the IDE bus is active, this signals is used as the active high primary slave IDE chip select signal. This signal is to be externally NANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

LA[20]/PCS1# *Unlatched Address (ISA)/Primary Chip Select (IDE).* This pin has two functions, depending on whether the ISA bus is active or the IDE bus is active.
When the ISA bus is active, this pins is ISA Bus unlatched address bit 20 for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, this pin is in output mode. When an ISA bus master owns the bus, this pins is in input mode.
When the IDE bus is active, this signals is used as the active high primary slave IDE chip select signal. This signal is to be externally NANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

LA[19:17]/DA[2:0] *Unlatched Address (ISA)/Address (IDE).* These pins are multi-function pins. They are used as the ISA bus unlatched address bits [19:17] for ISA bus or the three address bits for the IDE bus devices.
When used by the ISA bus, these pins are ISA Bus unlatched address bits 19-17 on 16-bit devices. When ISA bus is accessed by any cycle initiated from the PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are tristated.

For IDE devices, these signals are used as the DA[2:0] and are connected to DA[2:0] of IDE devices directly or through a buffer. If the toggling of signals are to be masked during ISA bus cycles, they can be externally ORed before being connected to the IDE devices.

SA[19:8]/DD[11:0] *Unlatched Address (ISA)/Data Bus (IDE).* These are multifunction pins. When the ISA bus is active, they are used as the ISA bus system address bits 19-8. When the IDE bus is active, they serve as IDE signals DD[11:0].
These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.
IDE devices are connected to SA[19:8] directlyand ISA bus is connected to these pins through two LS245 transceivers. The $\overline{OE}$ of the transceivers are connected to ISAOE# and DIR is connected to MASTER#. A bus signals of the transceivers are connected to CPC and IDE DD bus and B bus signals are connected to ISA SA bus.

DD[15:12] *Databus (IDE).* The high 4 bits of the IDE databus are combined with several of the X-bus lines. Refer to the following section for X-bus pins for further information.

SA[7:0] *ISA Bus address bits [7:0].* These are the 8 low bits of the system address bus of ISA on 8-bit slot. These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.

SD[15:0] *I/O Data Bus (ISA).* These pins are the external databus to the ISA bus.

2.2.7 ISA/IDE COMBINED CONTROL

IOCHRDY/DIORDY *Channel Ready (ISA)/Busy/Ready (IDE).* This is a multi-function pin. When the ISA bus is active, this pin is IOCHRDY. When the IDE bus is active, this serves as IDE signal DIORDY.
IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Client. The STPC Client monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh.
ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Client since the access to the system memory can be considerably delayed due to CRT refresh or a write back cycle.

2.2.8 ISA CONTROL

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the STPC Client to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the STPC Client.
ALE is driven low after reset.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Client generates SMEMR# signal of the ISA bus only when the address is below one megabyte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Client generates SMEMW# signal of the ISA bus only when the address is below one megabyte.

IOR# *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

MCS16# *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The STPC Client ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The STPC Client does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Client is executed as an extended 8-bit IO cycle.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Client performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Client performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that can not be corrected. NMI signal becomes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

ISAOE# *Bidirectional OE Control.* This signal controls the OE signal of the external transceiver that connects the IDE DD bus and ISA SA bus.

GPIOCS# *I/O General Purpose Chip Select 1.* This output signal is used by the external latch on ISA bus to latch the data on the SD[7:0] bus. The latch can be use by PMU unit to control the external peripheral devices to power down or any other desired function.
This pin is also serves as a strap input during reset.

2.2.9 IDE CONTROL

PIRQ *Primary Interrupt Request.* Interrupt request from primary IDE channel.

SIRQ *Secondary Interrupt Request.* Interrupt request from secondary IDE channel.

PDRQ *Primary DMA Request.* DMA request from primary IDE channel.

SDRQ *Secondary DMA Request.* DMA request from secondary IDE channel.

PDACK# *Primary DMA Acknowledge.* DMA acknoledge to primary IDE channel.

SDACK# *Secondary DMA Acknowledge.* DMA acknoledge to secondary IDE channel.

PIOR# *Primary I/O Read.* Primary channel read. Active low output.

PIOW# *Primary I/O Write.* Primary channel write. Active low output.

SIOR# *Secondary I/O Read* Secondary channel read. Active low output.

SIOW# *Secondary I/O Write* Secondary channel write. Active low output.

2.2.10 X-Bus Interface pins / IDE Data

RMRTCCS# / DD[15] *ROM/Real Time clock chip select.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as RMRTCCS#. This signal is asserted if a ROM access is decoded during a memory cycle. It should be combined with MEMR# or MEMW# signals to properly access the ROM. During a IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR or IOW# signals to properly access the real time clock.
When ISAOE# is inactive, this signal is used as IDE DD[15] signal.
This signal must be ORed externally with ISAOE# and is then connected to ROM and RTC. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor.

KBCS# / DD[14] *Keyboard Chip Select.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as KBCS#. This signal is asserted if a keyboard access is decoded during a I/O cycle.
When ISAOE# is inactive, this signal is used as IDE DD[14] signal.
This signal must be ORed externally with ISAOE# and is then connected to keyboard. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor.

RTCRW# / DD[13] *Real Time Clock R$\overline{W}$.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as RTCRW#. This signal is asserted for any I/O write to port 71H.
When ISAOE# is inactive, this signal is used as IDE DD[13] signal.
This signal must be ORed externally with ISAOE# and then connected to the RTC. An LS244 or equivalent function can be used if OE is connected to ISAOE# and the output is provided with a weak pull-up resistor.

RTCDS# / DD[12] *Real Time Clock DS.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as RTCDS. This signal is asserted for any I/O read to port 71H.
When ISAOE# is inactive, this signal is used as IDE DD[12] signal.
This signal must be ORed externally with ISAOE# and is then connected to RTC. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor.

2.2.11 IPC

IRQ_MUX[3:0] *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They are to be encoded before connection to the STPC Client using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the $\overline{IRQ}$ pin of the RTC.

PCI_INT[3:0] *PCI Interrupt Request.* These are the PCI bus interrupt signals. They are to be encoded before connection to the STPC Client using ISACLK and ISACLKX2 as the input selection strobes.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Client using ISACLK and ISACLKX2 as the input selection strobes.

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Client before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the byte count expires.

2.2.12 Monitor Interface

RED, GREEN, BLUE *RGB Video Outputs.* These are the 3 analog color outputs from the RAMDACs

VSYNC *Vertical Synchronisation Pulse.* This is the vertical synchronization signal from the VGA controller.

HSYNC *Horizontal Synchronisation Pulse.* This is the horizontal synchronization signal from the VGA controller.

VREF_DAC *DAC Voltage reference.* An external voltage reference is connected to this pin to bias the DAC.

RSET *Resistor Current Set.* This is reference current input to the RAMDAC is used to set the full-scale output of the RAMDAC.

COMP *Compensation.* This is the RAMDAC compensation pin. Normally, an external capacitor (typically 10nF) is connected between this pin and V_{DD} to damp oscillations.

DDC[1:0] *Direct Data Channel Serial Link.* These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to I^2C electrical specifications, they have open-collector output drivers which are internally connected to V_{DD} through pull-up resistors.

2.2.13 MISCELLANEOUS

ST[6:0] *Reserved.* The pins are reserved for Test and Miscellaneous functions)

CLKDEL[2:0] *Reserved.* The pins are reserved for Test and Miscellaneous functions)

Table 3. Pinout.

Pin #	Pin name
AF3	PWERGD
AF15	XTALI
AE16	XTALO
G23	HCLK
F25	DEV_CLK
AC5	GCLK2X
AD5	DCLK
AF5	DCLK_DIR
AD15	MA[0]
AF16	MA[1]
AC15	MA[2]
AE17	MA[3]
AD16	MA[4]
AF17	MA[5]
AC17	MA[6]
AE18	MA[7]
AD17	MA[8]
AF18	MA[9]
AE19	MA[10]
AF19	MA[11]
AD18	RAS#[0]
AE20	RAS#[1]
AC19	RAS#[2]
AF20	RAS#[3]
AE21	CAS#[0]
AC20	CAS#[1]
AF21	CAS#[2]
AD20	CAS#[3]
AE22	CAS#[4]
AF22	CAS#[5]
AD21	CAS#[6]
AE23	CAS#[7]
AC22	MWE#
AF23	MD[0]
AE24	MD[1]
AF24	MD[2]
AD25	MD[3]
AC25	MD[4]
AC26	MD[5]
AB24	MD[6]
AA25	MD[7]
AA24	MD[8]
Y25	MD[9]
Y24	MD[10]
V23	MD[11]
W24	MD[12]
V26	MD[13]
V24	MD[14]
U23	MD[15]
U24	MD[16]
R26	MD[17]
P25	MD[18]
P26	MD[19]
N25	MD[20]
N26	MD[21]
M25	MD[22]
M26	MD[23]
M24	MD[24]
M23	MD[25]
L24	MD[26]
J25	MD[27]
J26	MD[28]
H26	MD[29]
G25	MD[30]
G26	MD[31]
AD22	MD[32]
AD23	MD[33]
AE26	MD[34]
AD26	MD[35]
AC24	MD[36]
AB25	MD[37]
AB26	MD[38]
Y23	MD[39]
AA26	MD[40]
Y26	MD[41]
W25	MD[42]
W26	MD[43]
V25	MD[44]
U25	MD[45]
U26	MD[46]
T25	MD[47]
R25	MD[48]
T24	MD[49]
R23	MD[50]
R24	MD[51]
N23	MD[52]
P24	MD[53]
N24	MD[54]
L25	MD[55]
L26	MD[56]
K25	MD[57]
K26	MD[58]
K24	MD[59]
H25	MD[60]
J24	MD[61]
H23	MD[62]
H24	MD[63]
F24	PCI_CLKI
D25	PCI_CLKO
A20	AD[0]
C20	AD[1]
B19	AD[2]
A19	AD[3]
C19	AD[4]
B18	AD[5]
A18	AD[6]
B17	AD[7]
C18	AD[8]
A17	AD[9]
D17	AD[10]
B16	AD[11]
C17	AD[12]
B15	AD[13]
A15	AD[14]
C16	AD[15]
D15	AD[16]
A14	AD[17]
C15	AD[18]
B13	AD[19]
D13	AD[20]
A13	AD[21]
C14	AD[22]
C13	AD[23]
A12	AD[24]
B11	AD[25]
C12	AD[26]
A11	AD[27]
D12	AD[28]
B10	AD[29]
C11	AD[30]
A10	AD[31]
D10	CBE[0]
C10	CBE[1]
A9	CBE[2]
B8	CBE[3]
A8	FRAME#
B7	TRDY#
D8	IRDY#
A7	STOP#
C8	DEVSEL#
B6	PAR
D7	SERR#
A6	LOCK#
C21	PCI_REQ#[0]
A21	PCI_REQ#[1]
B20	PCI_REQ#[2]

PIN DESCRIPTION

Pin #	Pin name
C22	PCI_GNT#[0]
B21	PCI_GNT#[1]
D20	PCI_GNT#[2]
D24	PCI_INT[0]
C26	PCI_INT[1]
A25	PCI_INT[2]
B24	PCI_INT[3]
F2	LA[17]/DA[0]
G4	LA[18]/DA[1]
F3	LA[19]/DA[2]
F1	LA[20]/PCS1#
G2	LA[21]/PCS3#
G3	LA[22]/SCS1#
H2	LA[23]/SCS3#
J4	SA[0]
H1	SA[1]
H3	SA[2]
J2	SA[3]
J1	SA[4]
K2	SA[5]
J3	SA[6]
K1	SA[7]
K4	SA[8]/DD[0]
L2	SA[9]/DD[1]
K3	SA[10]/DD[2]
L1	SA[11]/DD[3]
M2	SA[12] / DD[4]
M1	SA[13] / DD[5]
L3	SA[14] / DD[6]
N2	SA[15] / DD[7]
M4	SA[16] / DD[8]
N1	SA[17] / DD[9]
M3	SA[18] / DD[10]
P4	SA[19] / DD[11]
P3	RTCDS / DD[12]
R2	RTCRW# / DD[13]
N3	KBCS# / DD[14]
P1	RMRTCCS# / DD[15]
R1	SD[0]
T2	SD[1]
R3	SD[2]
T1	SD[3]
R4	SD[4]
U2	SD[5]
T3	SD[6]
U1	SD[7]
U4	SD[8]
V2	SD[9]

Pin #	Pin name
U3	SD[10]
V1	SD[11]
W2	SD[12]
W1	SD[13]
V3	SD[14]
Y2	SD[15]
AE4	SYSRSETOx
AD4	ISA_CLK
AE5	ISA_CLK2X
C6	OSC14M
W3	ALE
AA2	BHE#
Y4	MEMR#
AA1	MEMW#
Y3	SMEMR#
AB2	SMEMW#
AA3	IOR#
AC2	IOW#
AB4	MASTER#
AC1	MCS16#
AB3	IOCS16#
AD2	REF#
AC3	AEN
AD1	IOCHCK#
AF2	ISAOE#
AE3	GPIOCS#
Y1	IOCHRDY
B1	PIRQ
C2	SIRQ
C1	PDRQ
D2	SDRQ
D3	PDACK#
D1	SDACK#
E2	PIOR#
E4	PIOW#
E3	SIOR#
E1	SIOW#
E23	IRQ_MUX[0]
D26	IRQ_MUX[1]
E24	IRQ_MUX[2]
C25	IRQ_MUX[3]
A24	DREQ_MUX[0]
B23	DREQ_MUX[1]
C23	DACK_ENC[0]
A23	DACK_ENC[1]
B22	DACK_ENC[2]
D22	TC

Pin #	Pin name
AE6	RED
AD6	GREEN
AF6	BLUE
AE9	VSYNC
AF9	HSYNC
AD7	VREF
AE8	RSET
AC9	COMP
AF8	DDC[1]
AD8	DDC[0]
AD14	VIDEO_CLK
AE13	VIDEO_D[0]
AC12	VIDEO_D[1]
AD12	VIDEO_D[2]
AE14	VIDEO_D[3]
AC14	VIDEO_D[4]
AF14	VIDEO_D[5]
AD13	VIDEO_D[6]
AE15	VIDEO_D[7]
AF10	VTV_YUV[0]
AC10	VTV_YUV[1]
AE11	VTV_YUV[2]
AD10	VTV_YUV[3]
AF11	VTV_YUV[4]
AE12	VTV_YUV[5]
AF12	VTV_YUV[6]
AD11	VTV_YUV[7]
AE10	VTV_HSYNC
AD9	VTV_BT#
B4	ST[0]
D5	ST[1]
A4	ST[2]
C5	ST[3]
B3	ST[4]
C4	ST[5]
A3	ST[6]
C7	CLKDEL[0]
B5	CLKDEL[1]
A5	CLKDEL[2]
AC7	VDD_DAC1
AF4	VDD_DAC2
W4	VDD_GCLK_PLL
AB1	VDD_DCLK_PLL
F26	VDD_HCLK_PLL
G24	VDD_DEVCLK_PLL

Pin #	Pin name
AF13	VDDE
AD19	VDDE
A16	VDD5
B12	VDD5
B9	VDD5
D18	VDD5
A22	VDD
B14	VDD
C9	VDD
D6	VDD
D11	VDD
D16	VDD
D21	VDD
F4	VDD
F23	VDD
G1	VDD
K23	VDD
L4	VDD
L23	VDD
P2	VDD
T4	VDD
T23	VDD
T26	VDD
AA4	VDD
AA23	VDD
AB23	VDD
AC6	VDD
AC11	VDD
AC16	VDD
AC21	VDD
AE7	VSS_DAC1
AF7	VSS_DAC2
E25	VSS_DLL
E26	VSS_DLL
A1:2	VSS
A26	VSS
B2	VSS
B25:26	VSS
C3	VSS
C24	VSS
D4	VSS
D9	VSS
D14	VSS
D19	VSS
D23	VSS
H4	VSS
J23	VSS
L11:16	VSS

Pin #	Pin name
M11:16	VSS
N4	VSS
N11:16	VSS
P11:16	VSS
P23	VSS
R11:16	VSS
T11:16	VSS
V4	VSS
W23	VSS
AC4	VSS
AC8	VSS
AC13	VSS
AC18	VSS
AC23	VSS
AD3	VSS
AD24	VSS
AE1:2	VSS
AE25	VSS
AF1	VSS
AF25	VSS
AF26	VSS

3 ELECTRICAL SPECIFICATIONS

3.1 Introduction

The electrical specifications in this chapter are valid for the STPC Client.

3.2 Electrical Connections

3.2.1 Power/Ground Connections/Decoupling

Due to the high frequency of operation of the STPC Client, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the STPC Client and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VSS and VDD pins.

3.2.2 Unused Input Pins

All inputs not used by the designer and not listed in the table of pin connections in Chapter 3 should be connected either to VDD or to VSS. Connect active-high inputs to VDD through a 20 kΩW (±10%) pull-down resistor and active-low inputs to VSS and connect active-low inputs to VCC through a 20 kΩW (±10%) pull-up resistor to prevent spurious operation.

3.2.3 Reserved Designated Pins

Pins designated reserved should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

3.3 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the STPC Client device. Stresses beyond those listed under Table 4 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those specified in section ”Operating Conditions”.

Exposure to conditions beyond Table 4 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 4) may also result in reduced useful life and reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DDx}	DC Supply Voltage	-0.3, 4.0	V
V_I, V_O	Digital Input and Output Voltage	-0.3, VDD + 0.3	V
T_{STG}	Storage Temperature	-40, +150	°C
T_{OPER}	Operating Temperature	0, +70	°C
P_{TOT}	Total Power Dissipation	4.8	W

3.4 DC Characteristics

Table 5. DC Characteristics

Recommended Operating conditions : VDD = 3.3V±0.3V, Tcase = 0 to 100°C unless otherwise specified

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
P_{DD}	Supply Power	V_{DD} = 3.3V, H_{CLK} = 66Mhz		3.2	3.9	W
H_{CLK}	Internal Clock	(Note 1)			75	Mhz
V_{REF}	DAC Voltage Reference		1.215	1.235	1.255	V
V_{OL}	Output Low Voltage	I_{Load} =1.5 to 8mA depending of the pin			0.5	V
V_{OH}	Output High Voltage	I_{Load} =-0.5 to -8mA depending of the pin	2.4			V
V_{IL}	Input Low Voltage	Except XTALI	-0.3		0.8	V
		XTALI	-0.3		0.9	V
V_{IH}	Input High Voltage	Except XTALI	2.1		V_{DD}+0.3	V
		XTALI	2.35		V_{DD}+0.3	V
I_{LK}	Input Leakage Current	Input, I/O	-5		5	µA
C_{IN}	Input Capacitance	(Note 2)				pF
C_{OUT}	Output Capacitance	(Note 2)				pF
C_{CLK}	Clock Capacitance	(Note 2)				pF

Notes:

1. MHz ratings refer to CPU clock frequency.
2. Not 100% tested.

3.5 AC Characteristics

Table 7 through Table 12 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified inFigure 8 and Figure 9. The rising clock edge reference level VREF , and other reference levels are shown inTable 6 below for the STPC Client. Input or output signals must cross these levels during testing.

Figure 8 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 6. Drive Level and Measurement Points for Switching Characteristics

Symbol	Value	Units
V_{REF}	1.5	V
V_{IHD}	3.0	V
V_{ILD}	0.0	V

Note: Refer to Figure 8.

Figure 8. Drive Level and Measurement Points for Switching Characteristics

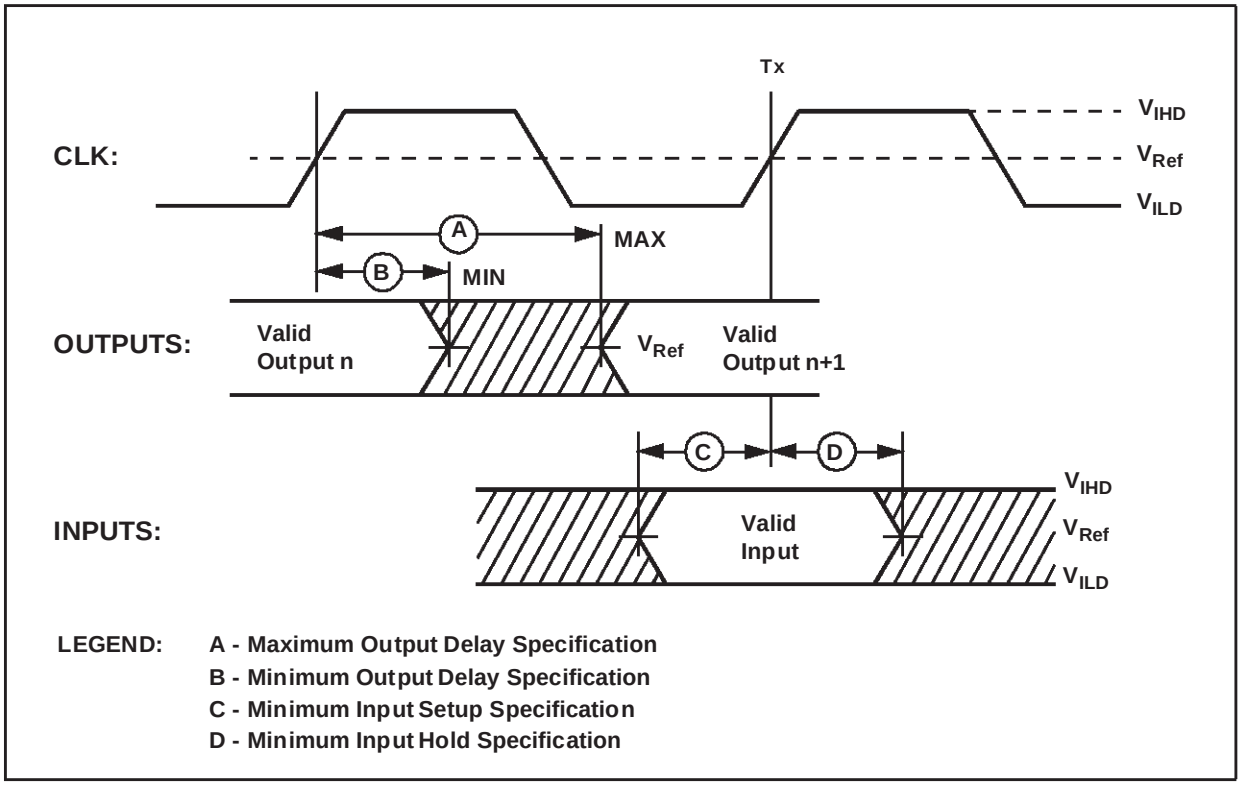


Figure 9. CLK Timing Measurement Points

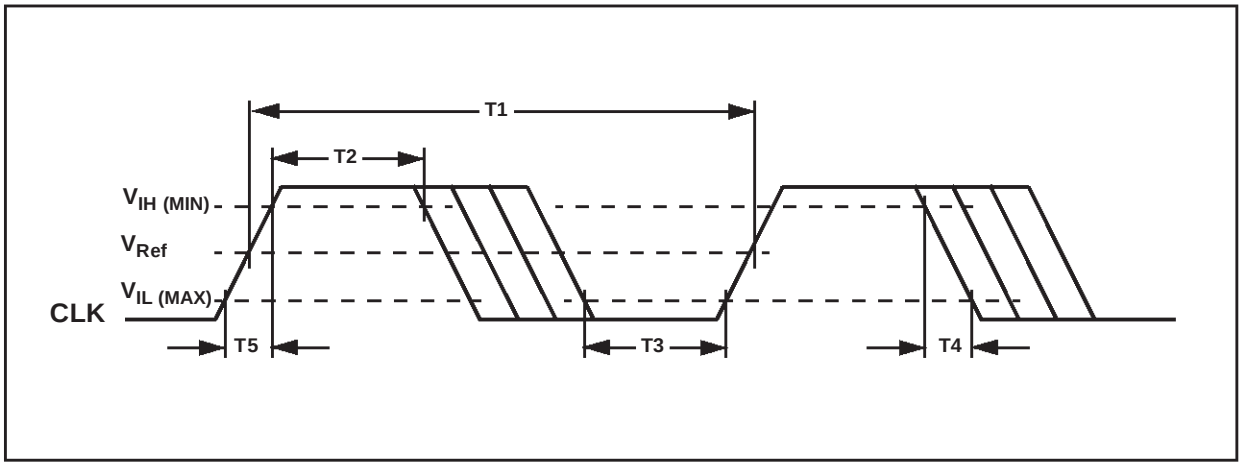


Table 7. PCI Bus AC Timing

Name	Parameter	Min	Max	Unit
t1	PCI_CLKI to AD[31:0] valid	2	11	ns
t2	PCI_CLKI to FRAME# valid	2	11	ns
t3	PCI_CLKI to CBE#[3:0] valid	2	11	ns
t4	PCI_CLKI to PAR valid	2	11	ns
t5	PCI_CLKI to TRDY# valid	2	11	ns
T6	PCI_CLKI to IRDY# valid	2	11	ns
T7	PCI_CLKI to STOP# valid	2	11	ns
T8	PCI_CLKI to DEVSEL# valid	2	11	ns
T9	PCI_CLKI to PCI_GNT# valid	2	12	ns
t10	AD[31:0] bus setup to PCI_CLKI	7		ns
t11	AD[31:0] bus hold from PCI_CLKI	0		ns
t12	PCI_REQ#[2:0] setup to PCI_CLKI	10		ns
t13	PCI_REQ#[2:0] hold from PCI_CLKI	0		ns
t14	CBE#[3:0] setup to PCI_CLKI	7		ns
t15	CBE#[3:0] hold to PCI_CLKI	0		ns
t16	IRDY# setup to PCI_CLKI	7		ns
t17	IRDY# hold to PCI_CLKI	0		ns
t18	FRAME# setup to PCI_CLKI	7		ns
t19	FRAME# hold from PCI_CLKI	0		ns

Table 8. IDE Bus AC Timing

Name	Parameter	Min	Max	Unit
t20	DD[15:0] setup to PIOR#/SIOR# falling	15		ns
t21	DD[15:0} hold to PIOR#/SIOR# falling	12		ns

Table 9. DRAM Bus AC Timing

Name	Parameter	Min	Max	Unit
t22	HCLK to RAS#[3:0] valid		15	ns
t23	HCLK to CAS#[7:0] bus valid		15	ns
t24	HCLK to MA[11:0] bus valid		15	ns
t25	HCLK to MWE# valid		15	ns
t26	HCLK to MD[63:0] bus valid		19	ns
t27	MD[63:0] Generic setup			ns
t28	GCLK2X to RAS#[3:0] valid		15	ns
t29	GCLK2X to CAS#[7:0] valid		15	ns
t30	GCLK2X to MA[11:0] bus valid		15	ns
t31	GCLK2X to MWE# valid		15	ns
t32	GCLK2X to MD[63:0] bus valid		18	ns
t33	MD[63:0] Generic hold			ns

Table 10. Video Input/TV Output AC Timing

Name	Parameter	Min	Max	Unit
t34	DCLK to TV_YUV[7:0] bus valid		18	ns
t35	VIDEO_D[7:0] setup to VCLK	5		ns
t36	VIDEO_D[7:0] hold from VCLK	2		ns
t37	VCLK to VTV_BT# valid		15	ns
t38	VCLK to VTV_HSYNC valid		15	ns
t39	VTV_BT# setup to VCLK	10		ns
t40	VTV_BT# hold from VCLK	5		ns
t41	VTV_HSYNC setup to VCLK	10		ns
t42	VTV_HSYNC hold from VCLK	5		ns

Table 11. Graphics Adapter (VGA) AC Timing

Name	Parameter	Min	Max	Unit
t43	DCLK to VSYNC valid		45	ns
t44	DCLK to HSYNC valid		45	ns

Table 12. ISA Bus AC Timing

Name	Parameter	Min	Max	Unit
t45	XTALO to LA[23:17] bus active		60	ns
t46	XTALO to SA[19:0] bus active		60	ns
t47	XTALO to BHE# valid		62	ns
t48	XTALO to SD[15:0] bus active		35	ns
t49	PCI_CLKI to ISAOE# valid		28	ns
t50	XTALO to GPIOCS# valid		60	ns
t51	XTALO to ALE valid		62	ns
t52	XTALO to MEMW# valid		50	ns
t53	XTALO to MEMR# valid		50	ns
t54	XTALO to SMEMW# valid		50	ns
t55	XTALO to SMEMR# valid		50	ns
t56	XTALO to IOR# valid		50	ns
t57	XTALO to IOW# valid		50	ns

4 MECHANICAL DATA

4.1 388-Pin Package

The pin numbering for the STPC 388-pin Plastic BGA package is shown in Figure 10.

Dimensions are shown in Figure 11, Table 13 and Figure 12, Table 14.

Figure 10. 388-Pin PBGA Package - Top View

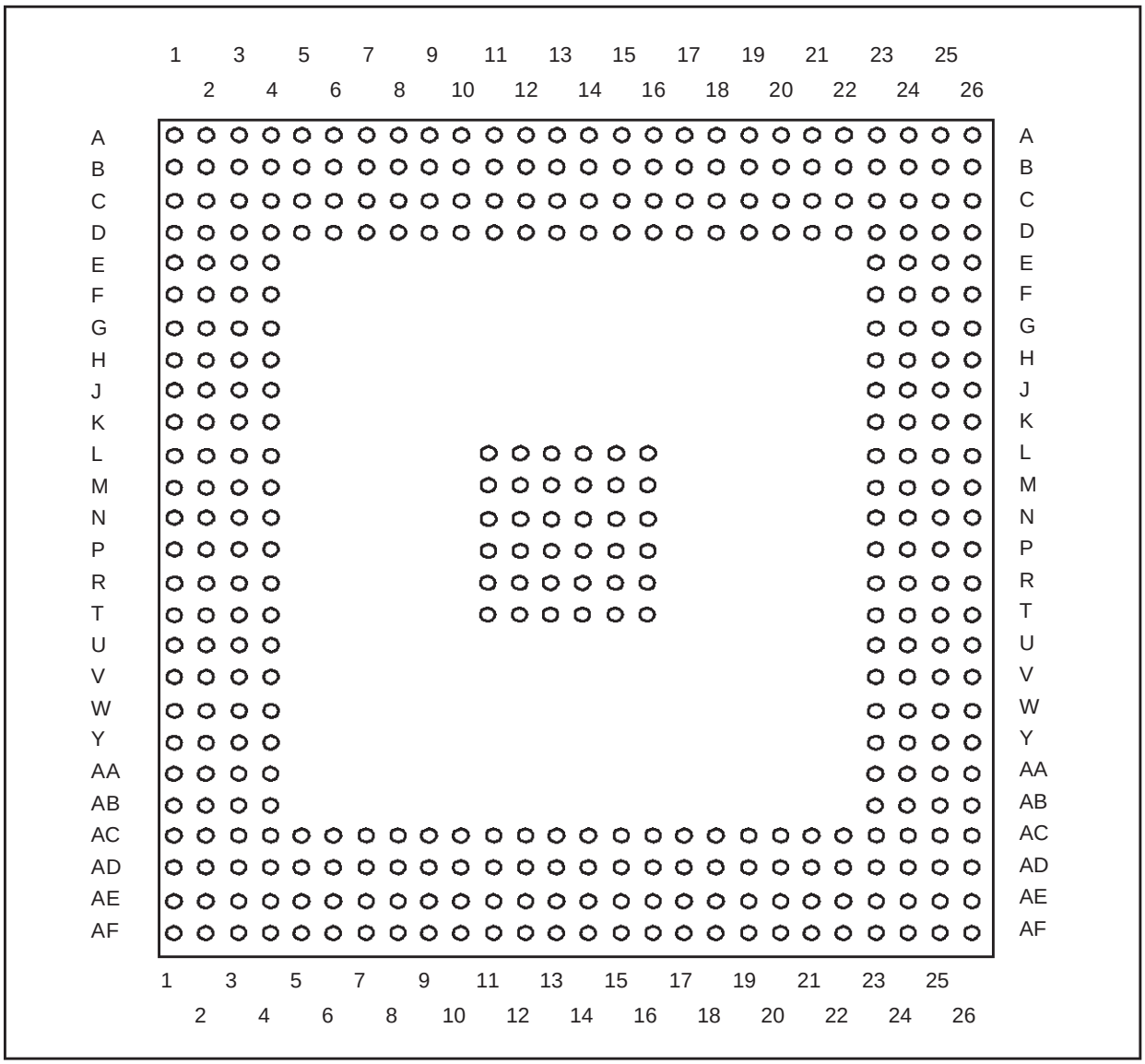


Figure 11. 388-Pin PBGA Package - Dimensions

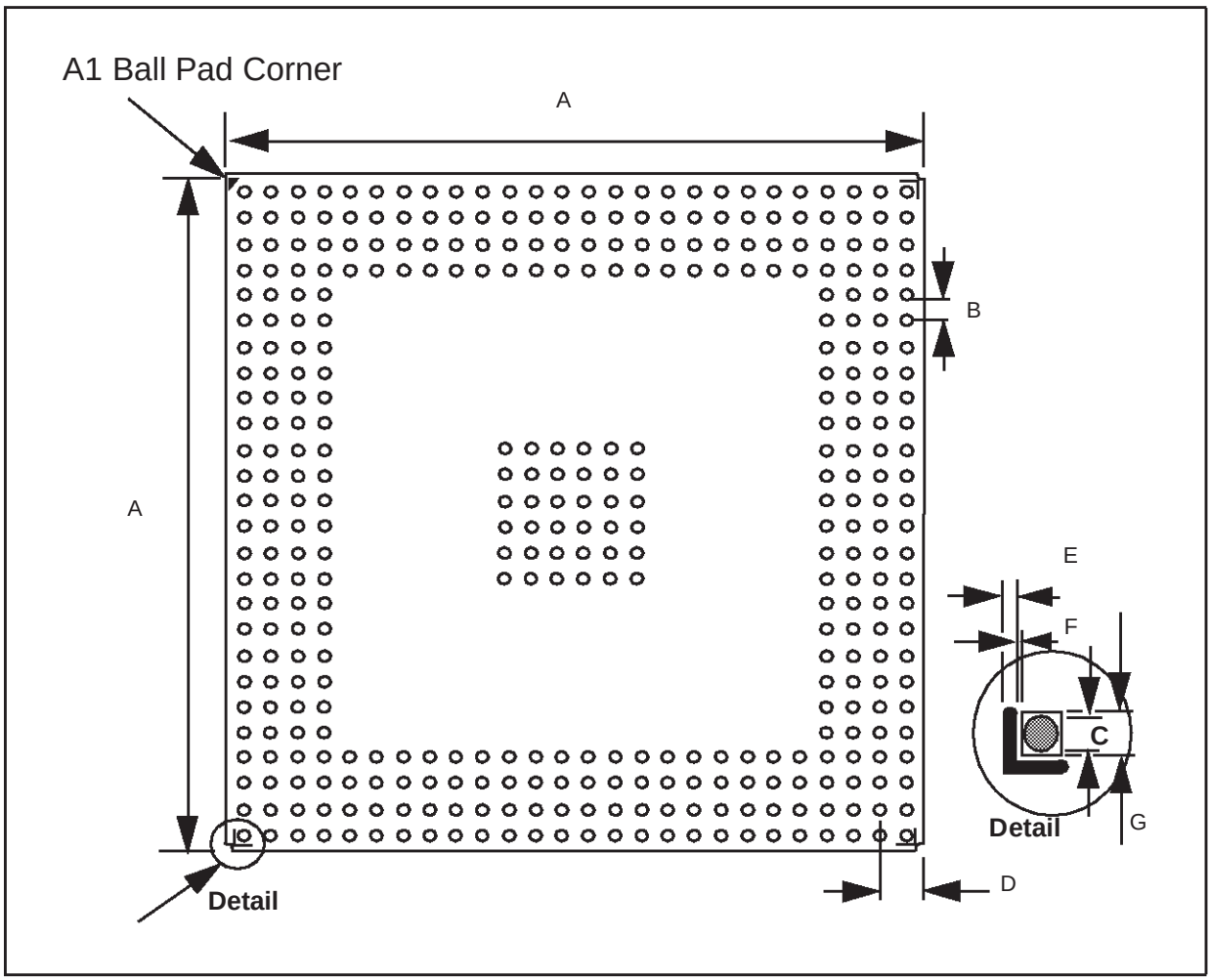


Table 13. PBGA388 - 388 Solder Ball Plastic 35mm x 35mm

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	34.95	35.00	35.05	1.375	1.378	1.380
B	1.22	1.27	1.32	0.048	0.050	0.052
C	0.58	0.63	0.68	0.023	0.025	0.027
D	1.57	1.62	1.67	0.062	0.064	0.066
E	0.15	0.20	0.25	0.006	0.008	0.001
F	0.05	0.10	0.15	0.002	0.004	0.006
G	0.75	0.80	0.85	0.030	0.032	0.034

Figure 12. 388-Pin PBGA Package - Dimensions (Continued)

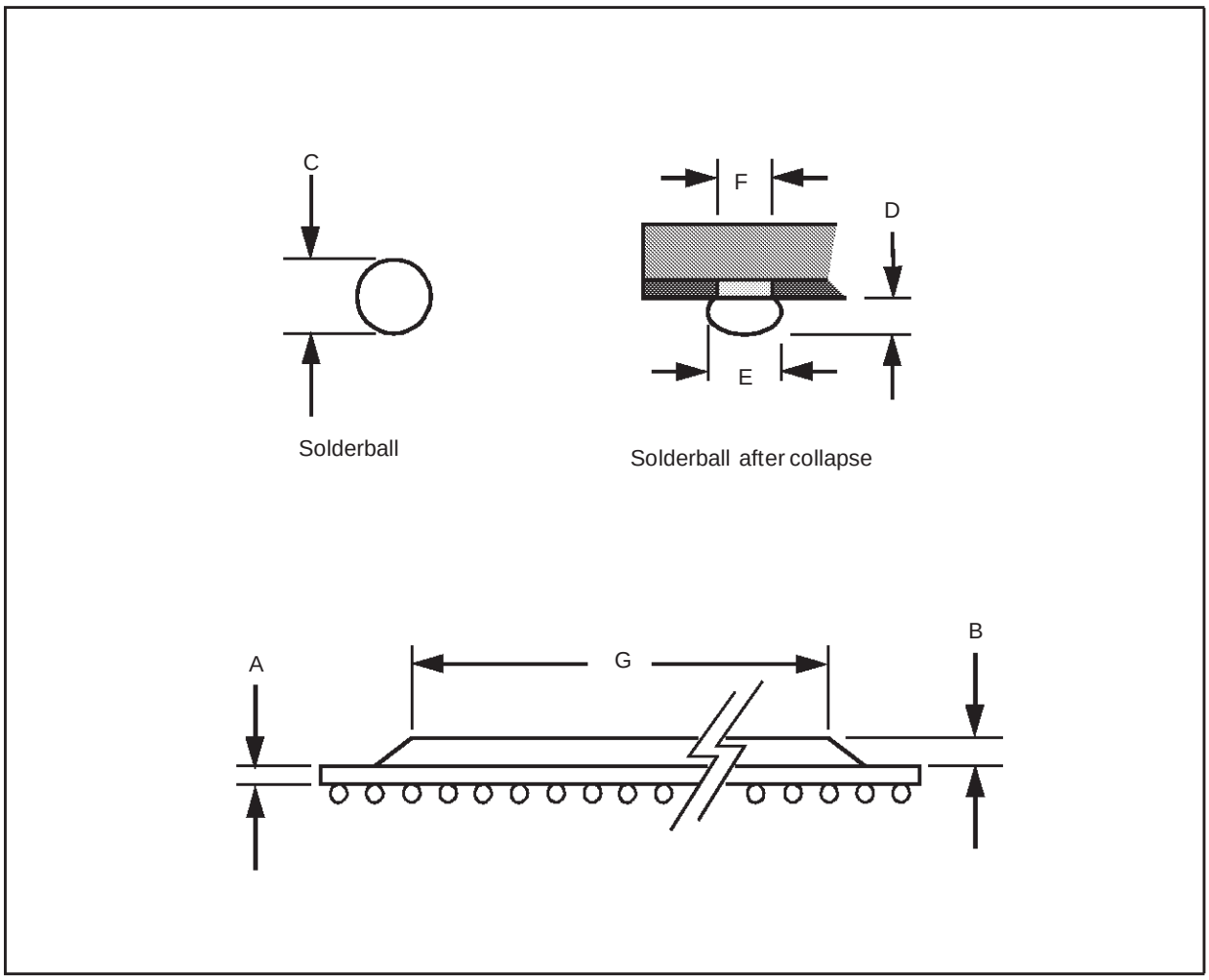
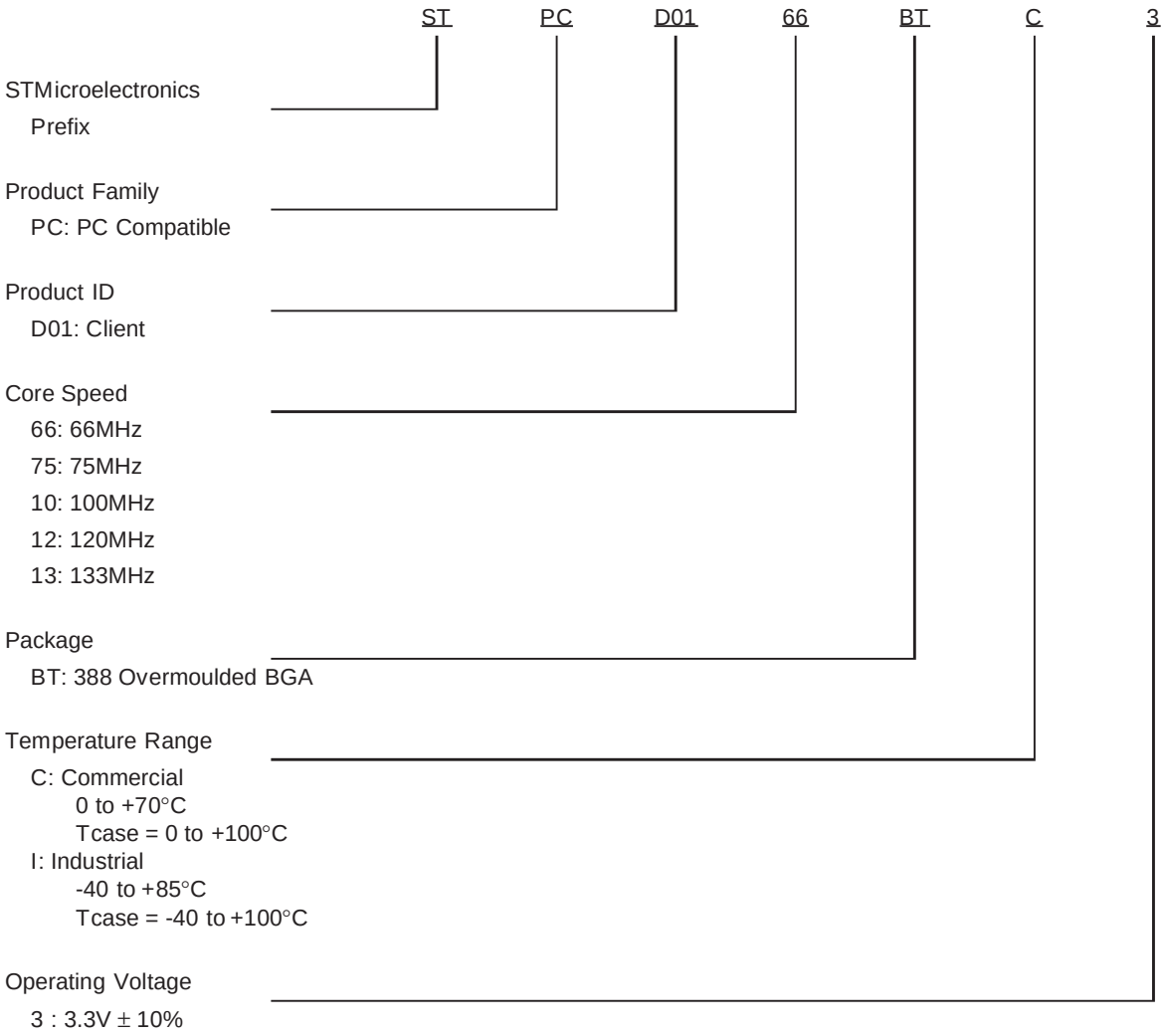


Table 14. PBGA388 - 388 Solder Ball Plastic 35mm x 35mm (Continued)

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.56	0.62	0.020	0.022	0.024
B	1.12	1.17	1.22	0.044	0.046	0.048
C	0.60	0.76	0.92	0.024	0.030	0.036
D	0.52	0.53	0.54	0.020	0.021	0.022
E	0.63	0.78	0.93	0.025	0.031	0.037
F	0.60	0.63	0.66	0.024	0.025	0.026
G		30.0			11.8	

5 ORDERING DATA

5.1 Ordering Codes



5.2 Available Part Numbers

Part Number	Core Frequency (MHz)	Temperature Range (C)	Operating Voltage (V)
STPCD0166BTC3	66	0 to + 70°	3.3V ± 10%
STPCD0175BTC3	75		
STPCD0110BTC3	100		
STPCD0112BTC3	120		
STPCD0113BTC3	133		

5.3 Customer Service

More informations are available on STMicroelectronics internet site *http://www.st.com/stpc*

For technical support, a mail-box is in place at *stpc.support@st.com*.