

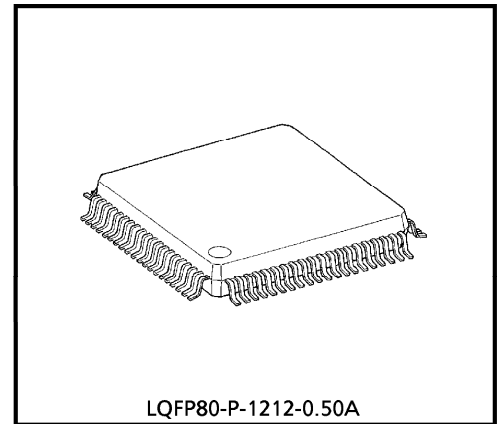
TC9317F

DTS MICROCONTROLLER (DTS-21)

The TC9317F is a 4bit CMOS microcontroller for digital tuning systems. It is capable of functioning at a low voltage of 3V and features a built-in PLL and LCD drivers. The CPU has 4bit parallel addition and subtraction instructions (e.g., AI, SI), logic operation instructions (e.g., OR, AND), composite judging and compare instructions (e.g., TM, SL), and time-base functions.

The package is an pin 80, 0.5-mm-pitch quad flat pack package. In addition to various input/output ports and a dedicated key-input port, which are controlled by powerful input/output instructions (IN 1~3, OUT 1~3), there are many dedicated LCD pins, a PWM output port, a buzzer port, a 6bit A/D converter, a serial interface, an IF counter, and other pins. A digital tuning system (DTS) is formed in conjunction with prescalers TD6134AF, TD7101F, or TD7103F.

Low-voltage and low-current consumption make this microcontroller suitable for portable DTS equipment.



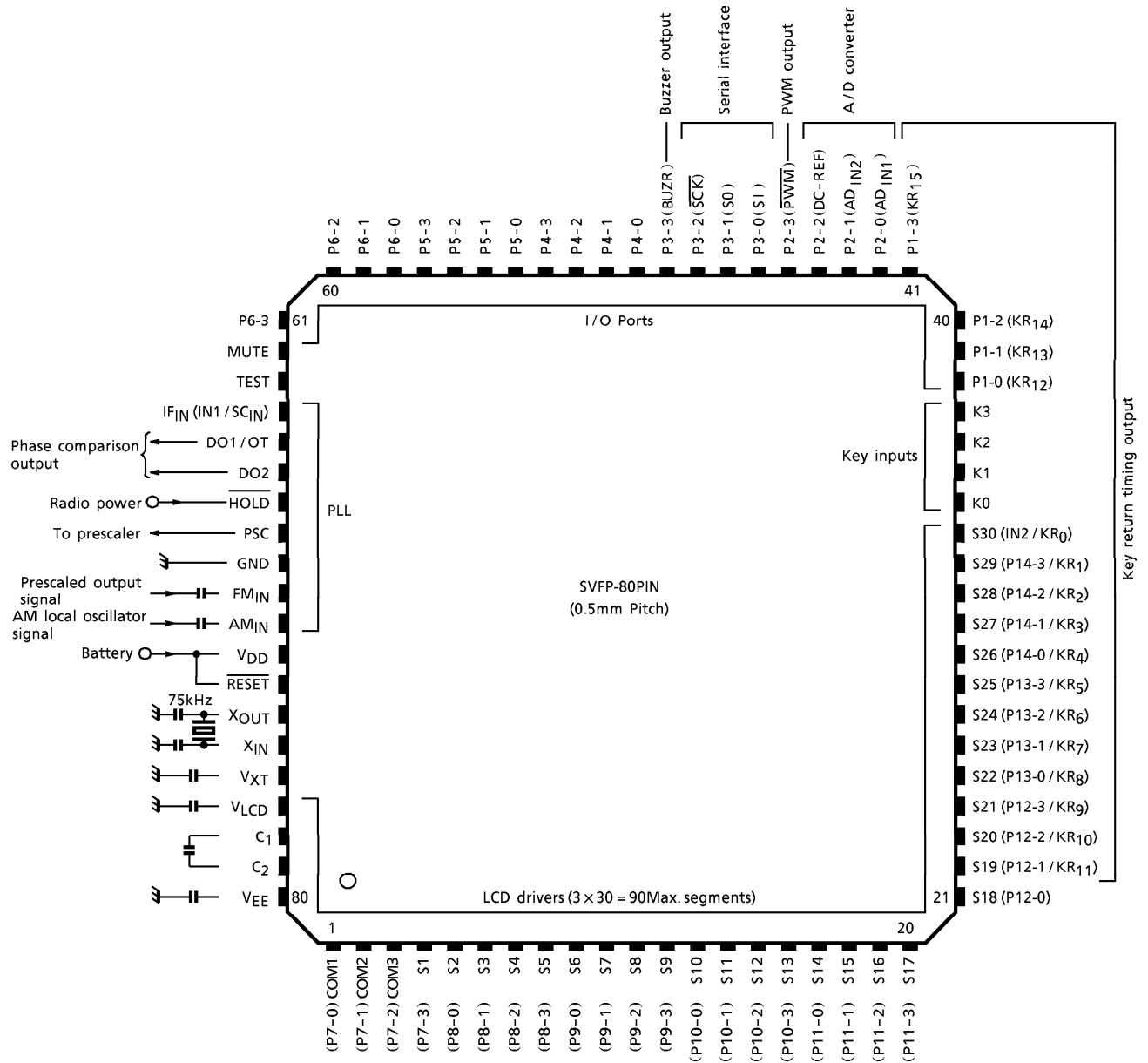
Weight : 0.45g (Typ.)

FEATURES

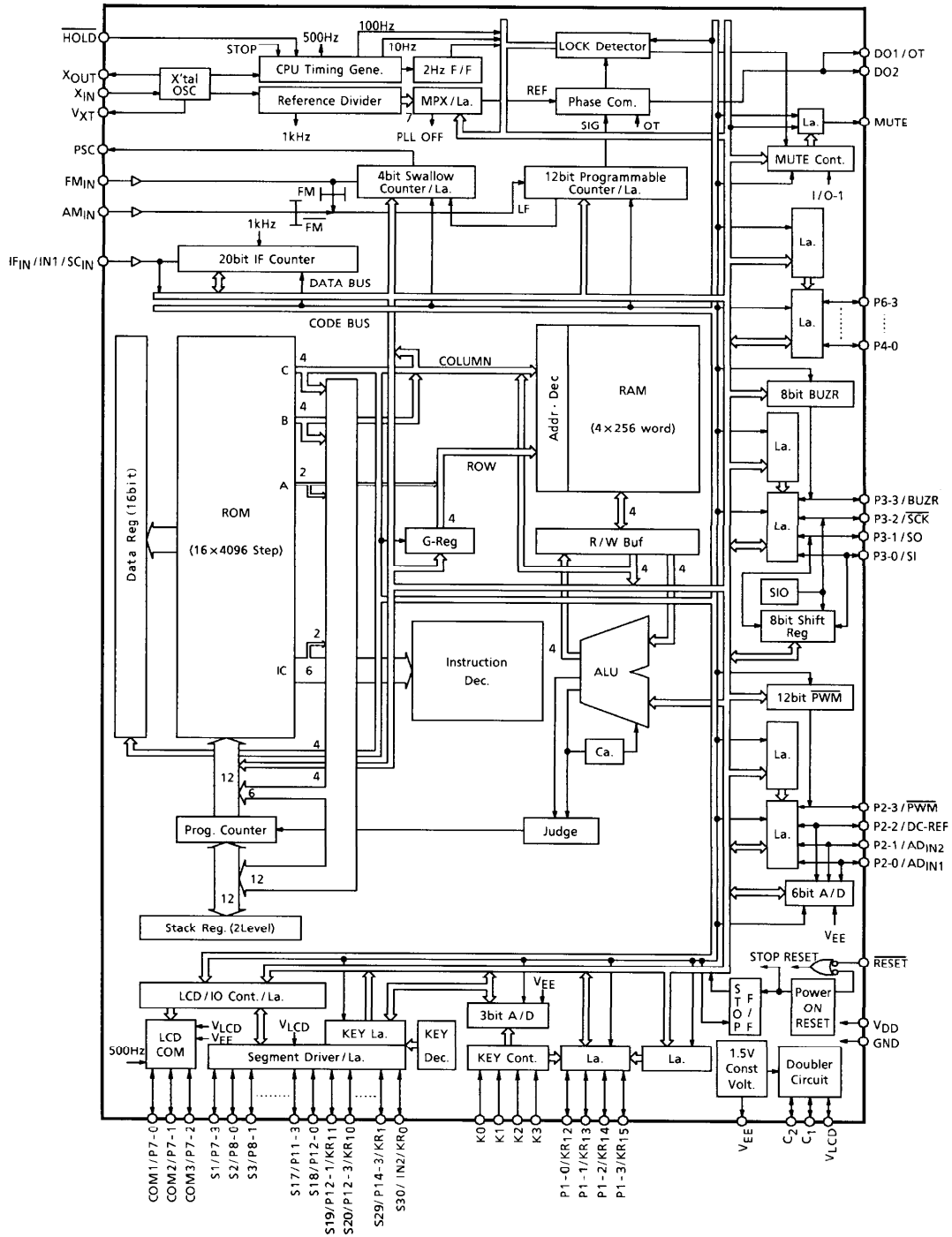
- 4bit microcontroller for digital tuning systems.
- Operating voltage $V_{DD} = 1.8 \sim 3.6V$, with low current consumption because of CMOS circuitry (with only CPU operating, when $V_{DD} = 3V$, $I_{DD} = 100\mu A$ max.)
- Features built-in 1/3-duty, 1/2-bias LCD drivers and a built-in 3V booster circuit for the display.
- Data memory (RAM) and ports are easily backed up.
- Program memory (ROM): 16bit \times 4096 steps
- Data memory (RAM) : 4bit \times 256 words
- 62-instruction set (all one-word instructions)
- Instruction execution time : $40\mu s$ (with 75kHz crystal) (MVGS, DAL instructions : $80\mu s$)
- Many addition and subtraction instructions (12 types addition, 12 types subtraction)
- Powerful composite judging instructions (TMTR, TMFR, TMT, TMF, TMTN, TMFN)
- Data can be transmitted between addresses on the same row.

- Register indirect transfer available (MVG D, MVG S).
- 16 powerful general registers (located in RAM)
- Stack levels : 2
- JUMP or CAL instruction can be used anywhere in the 4096 steps of program memory (ROM) as there are no pages or fields.
- 16bit of any address in the 1024 steps in program memory (ROM) can be referenced (DAL instruction).
- Features independent frequency input pins (FM_{IN} and AM_{IN}) and two (DO1 and DO2) phase comparison outputs for FM and AM.
- In FM or TV mode, a swallow counter is formed with prescalers TD6134AF, TD7101F or TD7103F, and signals of up to 250MHz can be received.
- Seven reference frequencies can be selected by program.
- Powerful input/output instructions (IN 1~3, OUT 1~3)
- Dedicated input ports (K₀~K₃) for key input. 33 LCD drive pins (90 segments maximum) available.
- 25 I/O ports: 24 with input/output programmable in 1bit units, and one output-only port. The three IF_{IN1}, IF_{IN2}, and DO1 pins can be switched by instruction to IN1 (input-only) or OT (output-only). All LCD output pins can be switched in 1bit units to I/O ports. (The S30 pin switches to an IN port).
- Three back-up modes available by instruction : only CPU operation, crystal oscillation only, clock stop.
- Features a built-in 2Hz timer F/F and a built-in 10/100Hz interval pulse output (internal port for time base).
- Allows PLL lock status detection.
- 12 of the LCD segment outputs (S19~S30) can also operate as key return timing outputs (KR0~KR11). The I/O ports are not dedicated key return timing outputs but can have other uses as well.
- Built-in 20bit, general-purpose IF counter can detect stations during auto-tuning by counting the intermediate frequencies of each band.
- Built-in 8bit buzzer output circuit can produce 254 different tone signals.
- Built-in 12bit PWM circuit can be used as a simple D/A converter.
- Features a built-in 2-channel, 6bit A/D converter.
- To prevent CPU malfunctions, a built-in supply voltage drop detection circuit shuts down the CPU when voltage falls below 1.5V.

PIN CONNECTION (TOP VIEW)

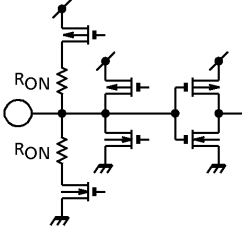
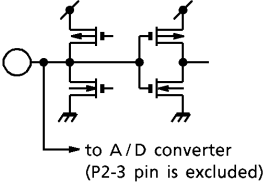


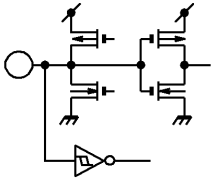
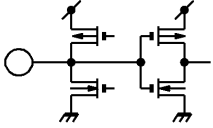
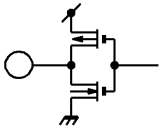
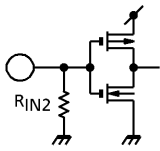
BLOCK DIAGRAM

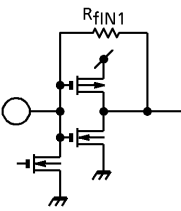
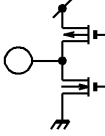


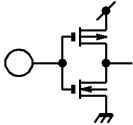
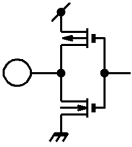
PIN FUNCTION

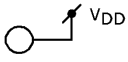
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	COM1/P7-0	LCD common output/input-output ports	Output common signals to the LCD panel. Through a matrix with pins S1~S30, a maximum of 90 segments can be displayed.	
2	COM2/P7-1		Three levels, V_{LCD} , V_{EE} , and GND, are output at 83Hz every 2ms.	
3	COM3/P7-2		V_{EE} is output after SYSTEM RESET and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0". These pins can also be programmed as I/O ports.	
4~21	S1/P7-3 S18/P12-0	LCD segment output/input-output ports	Segment signal output pins for the LCD panel. Together with COM1, COM2, and COM3, a matrix is formed that can display a maximum of 90 segments. These pins can also be programmed as I/O ports. (Port S30, however, can only be programmed as an input pin).	
22~33	S19/P12-1 / KR11 S30/IN2 / KR0	LCD segment output/input-output ports (IN port)/Key return timing output	The signals for the key matrix and the segment signals from pins S19 / KR11~S30 / KR0 are output on a time division basis. 4x12=48 key matrix can be created in conjunction with key input ports K0~K3.	
34~37	K0~K3	Key input ports	4bit input ports for key matrix input. When the key return timing outputs (KR0~KR11) of the LCD segment pins are combined in a matrix with the key return timing outputs (KR12~KR15) I/O port 1 (P1-0~P1-3) pins, data from a maximum of 4x16=64 keys can be input. An A/D comparator with a programmable 3bit threshold level is used as the input circuit. Input is selectable between pull-down, pull-up, or high impedance, making it possible to construct different types of key matrices. These key input ports may also be used as a sequential compare method 4-channel, 3bit A/D converter. The WAIT mode is released when high level is applied to key input ports set to pull-down.	

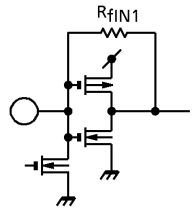
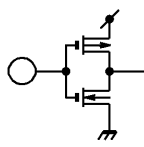
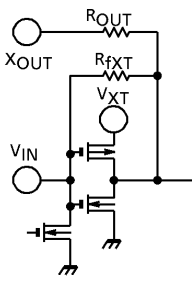
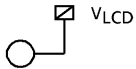
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
38~41	P1-0 / KR12 P1-3 / KR15	Input/output port 1/Key return timing output port	<p>The input and output of these 4bit I/O ports can be programmed in 1bit units. Can be programmed to output key matrix timing signals. To form the key matrix, load resistance has been built into both the N-channel and P-channel sides. A key matrix combined with the LCD segment output can be formed, as well as a push-key matrix that does not need a key matrix diode.</p> <p>By altering the input to I/O ports set to input, the CLOCK STOP and WAIT modes can be released, and the MUTE bit of the MUTE pin can be set to "1".</p>	
42~45	P2-0 / ADIN1 P2-1 / ADIN2 P2-2 / DC-REF P2-3 / $\overline{\text{PWM}}$	I/O port 2 / A/D analog voltage input / A/D analog voltage input / Reference voltage input / PWM output	<p>4bit I/O ports. Input and output may be programmed in 1bit units. Pins P2-0 through P2-2 can also be used for analog input to the built-in 6bit, 2-channel A/D converter. Conversion time of the built-in A/D converter using the successive comparison method is 280μs. The necessary pin can be programmed to A/D analog input in 1bit units, and P2-2 can be set to the reference voltage input. Internal power supply (V_{DD}) or constant voltage (V_{EE}) can be used as the reference voltage. In addition, constant voltage (V_{EE}) can be input to the A/D analog input so battery voltage, etc., can be easily detected. The reference voltage input, for which a built-in operational amp is used, has high impedance.</p> <p>Pin P2-3 can also take over the output of the built-in 12bit PWM. The PWM output is a continuous 73.26Hz pulse, whose duty is converted in 256 steps (8bit). In addition, a further 4bit are output every 16 PWM pulse cycles (218.5ms).</p> <p>The A/D converter, PWM output, and their control are all executed by program.</p>	 <p>to A/D converter (P2-3 pin is excluded)</p>

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
46~49	P3-0 / SI P3-1 / SO P3-2 / \overline{SCK} P3-3 / BUZR	I/O port 3 / Serial data input / Serial data output / Serial clock input-output / Buzzer output	4bit I/O ports, whose input/output can be programmed in 1bit units. Pins P3-0 through P3-2 also function as input/output pins for the serial interface circuit (SIO). The SIO serially inputs 4bit or 8bit data from the SI pin at the \overline{SCK} pin's clock edge, and serially outputs data from the SO pin. For the serial operation clock (\overline{SCK}) there is an internal/external option, and a rising/falling shift option. Moreover, because the SO pin can be switched to serial input (SI), LSI control and communication between controllers is simple. All SIO input pins use built-in Schmitt circuits. The P3-3 pin also functions as the output for the built-in buzzer circuit. The buzzer sound can be output in 254 different tones between 18.75kHz and 147Hz, and at a duty of 50%. The SIO, the buzzer output, and all associated controls can be programmed.	
50~61	P4-0 P6-3	I/O port 4 I/O port 6	The input and output of these 16bit I/O ports can be programmed in 1bit units.	
62	MUTE	Muting output port	1bit output port. Normally, this port is used for muting control signal output. This pin can set the internal MUTE bit to "1" according to a change in the input of I/O port 1. MUTE bit output logic can be changed; PPL phase difference can also be output using this pin.	
63	TEST	TEST mode control input	Input pin used for controlling TEST mode. High level indicates TEST mode, while low level indicates normal operation. The pin is normally used at low level or no-connection (NC). (A pull-down resistor is built in).	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
64	IF _{IN} / IN1 / SC _{IN}	IF signal input / Input port / Frequency measuring input	<p>IF counter's IF signal input pin for counting the IF signals of the FM and AM bands and detecting the automatic stop position.</p> <p>The input frequency is between 0.35~12MHz (0.2V_{p-p}-min). A built-in input amp and C coupling allow operation at low-level input.</p> <p>The IF counter is a 20bit counter with optional gate times of 1, 4, 16, and 64ms. 20 bits of data can be readily stored in memory.</p> <p>The IF counter can also be used as a timer when not being used as an IF counter.</p> <p>This input pin can be programmed for use as an input port (IN port). It can also be used to measure the frequency with the IF counter (SC_{IN}). CMOS input is used when the pin is set as an IN port.</p> <p>Note: When the pin is set for SC_{IN}, use DC coupling and input a square wave.</p>	
65 66	DO1 / OT DO2	Phase comparison output / Output port Phase comparison output	<p>PLL's phase comparison tri-state output pins.</p> <p>When the programmable counter's prescaler output is higher than the reference frequency, output is at high level. When output is lower than the reference frequency, output is at low level. When output equals the reference frequency, high impedance output is obtained.</p> <p>Because DO1 and DO2 are output in parallel, optimal filter constants can be designed for the FM / VHF and AM bands.</p> <p>Pin DO1 can be programmed to high impedance or programmed as an output port (OT). Thus, the pins can be used to improve lock-up time or used as output ports.</p>	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
67	$\overline{\text{HOLD}}$	HOLD mode control input	<p>Input pin for request/release HOLD mode.</p> <p>Normally, this pin is used to input radio mode selection signals or battery detection signals.</p> <p>HOLD mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. When the CKSTP instruction is executed, request/release of the HOLD mode depends on the internal MODE bit. If the MODE bit is "0" (MODE-0), executing the CKSTP instruction while the $\overline{\text{HOLD}}$ pin is at low level stops the clock generator and the CPU and changes to memory back-up mode. If the MODE bit is "1" (MODE-1), executing the CKSTP instruction enters memory back-up mode regardless of the level of the $\overline{\text{HOLD}}$ pin. Memory back-up is released when the $\overline{\text{HOLD}}$ pin goes high in MODE-0, or when the level of the $\overline{\text{HOLD}}$ pin level in MODE-1.</p> <p>When memory back-up mode is entered by executing a WAIT instruction, any change in the $\overline{\text{HOLD}}$ pin input releases the mode.</p> <p>In memory back-up mode, current consumption is low (below $1\mu\text{A}$), and all the output pins (e.g., display output, output ports) are automatically set to low level.</p>	
68	PSC	Prescaler control output	<p>Output pin that controls the switching of two modulus prescaler ratios between 1/15 and 1/16.</p> <p>When the programmable counter is used in pulse swallow frequency division mode, this output pin controls the external prescaler ratio.</p> <p>High : 1/16, Low : 1/15</p>	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
72	V _{DD}	Power-supply pins	<p>Pins to which power is applied. Normally, V_{DD} = 1.8~3.6V (3.0V typ.) is applied.</p> <p>In back-up mode (when CKSTP instructions are being executed), voltage can be lowered to 1.0V. If voltage falls below 1.5V while the CPU is operating, the CPU stops to prevent malfunction (STOP mode). When the voltage rises above 1.5V, the CPU restarts.</p> <p>STOP mode can be detected by checking the STOP F/F bit. If necessary, execute initialization or adjust clock by program.</p> <p>When detecting or preventing CPU malfunctions using an external circuit, STOP mode can be invalidated and rendered non-operative by program. In that case, all four bits of the internal TEST port should be set to "1".</p> <p>If more than 1.8V is applied when the pin voltage is 0, the device's system is reset and the program starts from address "0". (Power on reset)</p> <p>Note: To operate the power on reset, the power supply should start up in 10~100ms.</p>	
69	GND			<p>Programmable counter input pin for the 16bit pulse swallow frequency division method.</p> <p>This pin inputs the external prescaler output signals.</p> <p>A built-in input amp and C coupling allow operation at low-level input.</p> <p>Note: When in the PLL OFF mode or when set to AMIN input, the input is pulled down.</p>
70	FM _{IN}	FM programmable counter input	<p>Note: To operate the power on reset, the power supply should start up in 10~100ms.</p>	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
71	AM _{IN}	AM local oscillator signal input	Programmable counter input pin when using the 12bit direct dividing method. Normally, the pin inputs AM band local oscillation signals. Built-in input amp operates with low-level input using a C coupling. Note: When in PLL OFF mode or when set to FMIN input, the input is pulled down.	
73	RESET	Reset input	Input pin for system reset signals. Reset takes place while at low level; at high level, the program starts from address "0". Normally, if more than 1.8V is supplied to V _{DD} when the voltage is 0, the system is reset (Power on reset). Accordingly, this pin should be set to high level during operation.	
74	X _{OUT}	Crystal oscillator pins	Crystal oscillator pins A reference 75kHz crystal oscillator is connected to the X _{IN} and X _{OUT} pins. The oscillator stops oscillating during CKSTP instruction execution. The V _{X_T} pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.1μF typ.) is connected.	
75	X _{IN}			
76	V _{X_T}			
77	V _{LCD}	Voltage doubler boosting pin	Voltage doubler boosting pin for driving the LCD. A capacitor (0.1~3.3μF typ.) is connected to boost the voltage. The V _{LCD} pin outputs voltage (3.0V), which has been doubled from the constant voltage (V _{EE} : 1.5V) using the capacitors connected between C ₁ and C ₂ . That potential is supplied to the LCD drivers. If the internal V _{LCD} OFF bit is set to "1" by program, an external power supply can be input through the VLCD pin to drive the LCD. At this time, the V _{LCD} /2 potential, whose V _{LCD} voltage is divided using registers, is output from the C ₂ pin.	
78	C ₁			
79	C ₂			

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
80	V _{EE}	Constant voltage supply pin	1.5V constant voltage supply pin for driving the LCD. A stabilizing capacitor (0.47 μ F typ.) is connected. This is a reference voltage for the A/D converter, key input, and the LCD common output's bias potential.	—

- (Note) 1. When the device is reset (voltage higher than 1.8V, or when $\overline{\text{RESET}} = \text{low} \rightarrow \text{high}$) I/O ports are set to input, the pins for LCD output and I/O ports are set to LCD output, the pins for I/O ports and additional functions (e.g., SIO, A/D converter) are set to I/O port input pins, while the IF_{IN}/IN1/SC_{IN} pins become IF input pins.
2. When in PLL OFF mode (when the four bits in the internal reference ports all show "1"), the IF_{IN}/SC_{IN} and FM_{IN}/AM_{IN} pins are pulled down, and DO1 and DO2 are at high impedance.
3. When in CLOCK STOP mode (during execution of CKSTP instruction), the output ports and the LCD output pins are all at low level, while the constant voltage circuit (V_{EE}), the voltage doubler circuit (V_{LCD}), and the power supply for the crystal oscillator (V_{XT}) are all off.
4. When the device is being reset, the contents of the output ports and internal ports are undefined and initialization by program is necessary.
5. If the pins for LCD output and I/O ports are set to I/O ports, because the V_{LCD} potential is used as the power supply for their input and output, attention must be paid to the input potential when the ports are set to input, and to the high-level output current when set to output.

DESCRIPTION OF OPERATION

○ CPU

The CPU consists of: program counter, stack register, ALU, program memory, data memory, G-register, data register, carry F/F and judge circuit.

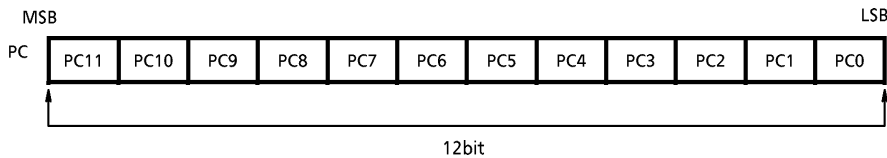
1. Program counter (PC)

This counter consists of a 12bit binary up-counter and is for addressing program memory (ROM). It is cleared by system reset and a program starts from address 0.

Normally, when one instruction is executed, it is incremented by one.

However, when JUMP or CAL instruction is executed, the address designated in the operand of the instruction will be loaded.

When an instruction having the skip function (AIS, SLTI, TMT, RNS instruction, etc.) is executed and, if the result is a condition to be skipped it is incremented by two and skips next instruction.



2. Stack register (STACK)

It is a register consisting of 2 × 12 bits.

When subroutine call instruction is executed, a value of the contents of program counter + 1, that is, return address is stored in this register.

The contents of this register is loaded into program counter when return instruction (RN, RNS instruction) is executed.

This stack level is 2 levels and the nesting also is 2 levels.

3. ALU

It has the following functions: binary 4bit parallel add-subtraction, logical operation, comparison, multiple bit judge.

The contents of data memory are directly treated in every operation because this CPU has no accumulator.

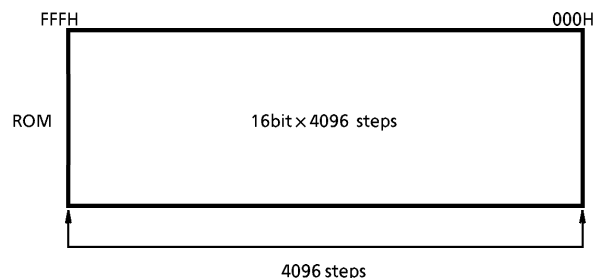
4. Program memory (ROM)

It consists of 16 bits×4096 steps and stores programs. The usable address range is 4096 steps from address 000H to FFFH.

There is no concept of page and field in program memory, JUMP and CAL instructions are freely usable in 4096 steps. Any address in program memory can be used as data area. When DAL instruction is executed, the contents of 16 bits are loaded into data register.

(Note) Set the data area in program memory to an address outside the program loop.

(Note) When DAL instruction is executed, the address of program memory designatable as data area is within 1024 steps from 000H to 3FFH.



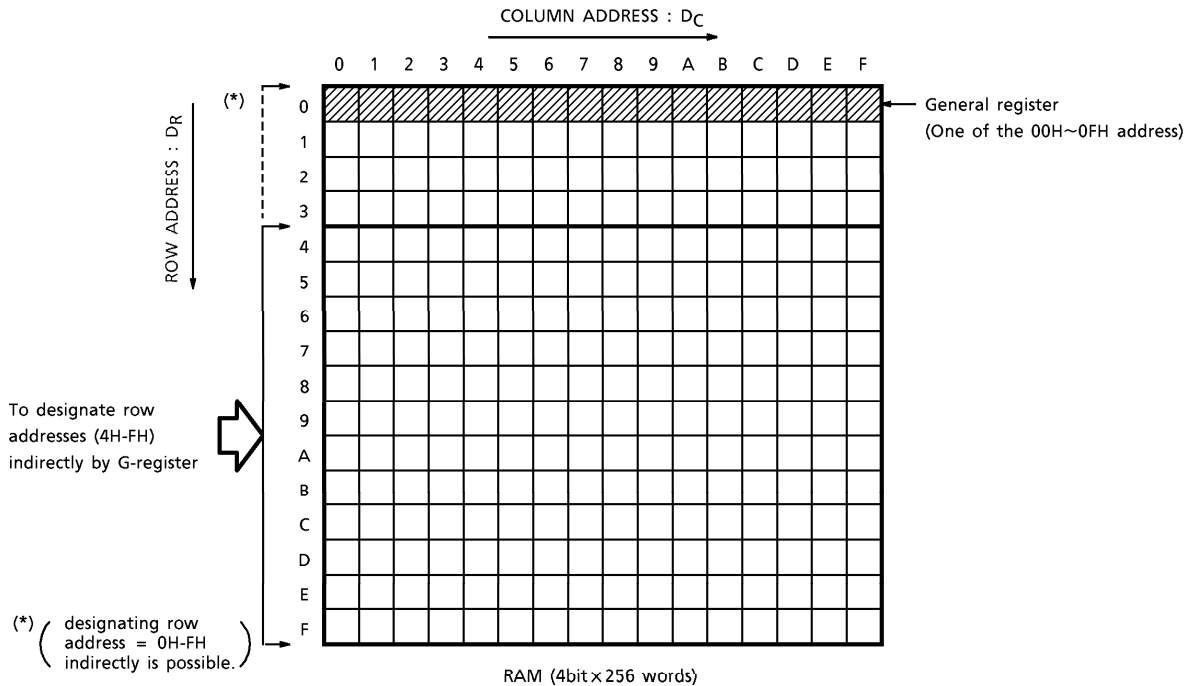
5. Data memory (RAM)

It consists of 4bit×256 words and is used for data storage. These 256 words are expressed by the row address (4 bits) and column address (4 bits). 192-words in data memory (row address = 4H~FH address) are indirectly addressed by G-register. For this reason, when processing data within this area, it is necessary to process after the row address is designated by G-register in advance.

The address 00H~0FH in data memory is called general register. This is also usable for designating only the column address (4 bits). These 16 general registers are used for operation and transfer with the data memory and are also usable as ordinary data memories.

(Note) The column address (4 bits) designating general register become the register number of general register.

(Note) It is possible to designate all row addresses (0H~FH address) indirectly by G-register.



6. G-Register (G-REG)

It is a 4bit register for addressing row addresses (DR = 4H~FH address) of 192 words of data memory. The contents of this register are valid when MVGD / MVGS instruction is executed and have nothing to do when other instructions are executed. This register is used as one port and the contents are set when OUT1 instruction of I/O instructions is executed. (Refer to Register Port, item 1.)

7. Data register (DATA REG)

It is a register consisting of 1 x 16bit. When DAL instruction is executed, the 16bit data of any address between 000H~3FFH in program memory is loaded. This register is treated as one of port and when IN1 instruction of I/O instructions is executed, it's contents are loaded into data memory by 4 bits unit. (Refer to register port, item2.)

8. Carry F/F (CF/F)

This is set if carry or borrow is generated as a result of execution of the calculation instruction and reset if neither is generated.

The contents of carry F/F changes only when addition /subtraction instruction is executed and remain unchanged when other instructions are executed.

9. Judge circuit (J)

When an instruction with the skip function is executed, it judges the skip condition. When the skip condition is satisfied, the program counter is incremented by two and the subsequent instruction is skipped.

There are 29 instructions having the skip function. (Refer to item 11, Instruction Function, Table of Operational Instruction marked "**".)

10. Table of instruction set

Total 62 kinds of instruction sets are available, and instructions are all one word.

These instructions are expressed in a 6bit instruction code.

HIGH ORDER LOW ORDER 2BIT ORDER 4BIT		00	01	10	11
		0	1	2	3
0000	0	AI M, I	AD r, M	TMTR r, M	SLTI M, I
0001	1	AIS M, I	ADS r, M	TMFR r, M	SGEI M, I
0010	2	AIN M, I	ADN r, M	SEQ r, M	SEQI M, I
0011	3	AIC M, I	AC r, M	SNE r, M	SNEI M, I
0100	4	AICS M, I	ACS r, M	LD r, M	TMTN M, N
0101	5	AICN M, I	ACN r, M	ST M, r	TMT M, N
0110	6	ORIM M, I	ORR r, M	MVGD r, M	TMFN M, N
0111	7	ANIM M, I	ANDR r, M	MVGS M, r	TMF M, N
1000	8	SI M, I	SU r, M	CALL ADDR ₁	IN1 M, C
1001	9	SIS M, I	SUS r, M		IN2 M, C
1010	A	SIN M, I	SUN r, M		IN3 M, C
1011	B	SIB M, I	SB r, M		OUT1 C, M
1100	C	SIBS M, I	SBS r, M	JUMP ADDR ₁	OUT2 C, M
1101	D	SIBN M, I	SBN r, M		OUT3 C, M
1110	E	XORI M, I	XORR r, M		DAL ADDR ₂ , r
1111	F	MVIM M, I	MVSR M ₁ , M ₂		RN, RNS, WAIT CKSTP, NOOP

11. Table of functions and operation of instruction

(Explanation of symbols in the table)

M	: Data memory address Generally one of data memory addresses 00H~3FH
r	: General register One of data memory addresses 00H~0FH
PC	: Program counter (12bit)
STACK	: Stack register (12bit)
G	: G-register (4bit)
DATA	: Data register (16bit)
I	: Immediate data (4bit)
N	: Bit position (4bit)
—	: ALL "0"
C	: Port code No. (4bit)
C _N	: Port code No. (4bit)
R _N	: General register No. (4bit)
ADDR ₁	: Program memory address (12bit)
ADDR ₂	: High order 6bit of program memory address in page 0
Ca	: Carry
b	: Borrow
IN1~IN3	: Port treated by execution of IN1~IN3 instruction
OUT1~OUT3	: Port treated by execution of OUT1~OUT3 instruction
()	: Contents of register or data memory
[] _C	: Contents of port indicated by Code No. C
[]	: Contents of data memory shown by the contents of register or data memory
[] _P	: Contents of program memory (16bit)
IC	: Instruction code (6bit)
※	: Instruction with skip function
D _C	: Data memory column address (4bit)
D _R	: Data memory row address (2bit)

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC 6bit	A 2bit	B 4bit	C 4bit
Addition instruction	AI M, I		Add immediate data to memory	$M \leftarrow (M) + I$	000000	D _R	D _C	I
	AIS M, I	※	Add immediate data to memory, then skip if carry	$M \leftarrow (M) + I$ Skip if carry	000001	D _R	D _C	I
	AIN M, I	※	Add immediate data to memory, then skip if not carry	$M \leftarrow (M) + I$ Skip if not carry	000010	D _R	D _C	I
	AIC M, I		Add immediate data to memory with carry	$M \leftarrow (M) + I + ca$	000011	D _R	D _C	I
	AICS M, I	※	Add immediate data to memory with carry, then skip if carry	$M \leftarrow (M) + I + ca$ Skip if carry	000100	D _R	D _C	I
	AICN M, I	※	Add immediate data to memory with carry, then skip if not carry	$M \leftarrow (M) + I + ca$ Skip if not carry	000101	D _R	D _C	I
	AD r, M		Add memory to general register	$r \leftarrow (r) + (M)$	010000	D _R	D _C	R _N
	ADS r, M	※	Add memory to general register, then skip if carry	$r \leftarrow (r) + (M)$ Skip if carry	010001	D _R	D _C	R _N
	ADN r, M	※	Add memory to general register, then skip if not carry	$r \leftarrow (r) + (M)$ Skip if not carry	010010	D _R	D _C	R _N
	ACr, M		Add memory to general register with carry	$r \leftarrow (r) + (M) + ca$	010011	D _R	D _C	R _N
	ACS r, M	※	Add memory to general register with carry, then skip if carry	$r \leftarrow (r) + (M) + ca$ Skip if carry	010100	D _R	D _C	R _N
	ACN r, M	※	Add memory to general register with carry, then skip if not carry	$r \leftarrow (r) + (M) + ca$ Skip if not carry	010101	D _R	D _C	R _N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC 6bit	A 2bit	B 4bit	C 4bit
Subtraction instruction	SI M, I		Subtract immediate data from memory	$M \leftarrow (M) - I$	001000	D _R	D _C	I
	SIS M, I	※	Subtract immediate data from memory, then skip if borrow	$M \leftarrow (M) - I$ Skip if borrow	001001	D _R	D _C	I
	SIN M, I	※	Subtract immediate data from memory, then skip if not borrow	$M \leftarrow (M) - I$ Skip if not borrow	001010	D _R	D _C	I
	SIB M, I		Subtract immediate data from memory with borrow	$M \leftarrow (M) - I - b$	001011	D _R	D _C	I
	SIBS M, I	※	Subtract immediate data from memory with borrow, then skip if borrow	$M \leftarrow (M) - I - b$ Skip if borrow	001100	D _R	D _C	I
	SIBN M, I	※	Subtract immediate data from memory with borrow, then skip if not borrow	$M \leftarrow (M) - I - b$ Skip if not borrow	001101	D _R	D _C	I
	SU r, M		Subtract memory from general register	$r \leftarrow (r) - (M)$	011000	D _R	D _C	R _N
	SUS r, M	※	Subtract memory from general register, then skip if borrow	$r \leftarrow (r) - (M)$ Skip if borrow	011001	D _R	D _C	R _N
	SUN r, M	※	Subtract memory from general register, then skip if not borrow	$r \leftarrow (r) - (M)$ Skip if not borrow	011010	D _R	D _C	R _N
	SB r, M		Subtract memory from general register with borrow	$r \leftarrow (r) - (M) - b$	011011	D _R	D _C	R _N
	SBS r, M	※	Subtract memory from general register with borrow, then skip if borrow	$r \leftarrow (r) - (M) - b$ Skip if borrow	011100	D _R	D _C	R _N
	SBN r, M	※	Subtract memory from general register with borrow, then skip if not borrow	$r \leftarrow (r) - (M) - b$ Skip if not borrow	011101	D _R	D _C	R _N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC 6bit	A 2bit	B 4bit	C 4bit
Comparison instruction	SLTI M, I	※	Skip if memory is less than immediate data	Skip if $(M) < I$	110000	D _R	D _C	I
	SGEI M, I	※	Skip if memory is greater than or equal to immediate data	Skip if $(M) \geq I$	110001	D _R	D _C	I
	SEQI M, I	※	Skip if memory is equal to immediate data	Skip if $(M) = I$	110010	D _R	D _C	I
	SNEI M, I	※	Skip if memory is not equal to immediate data	Skip if $(M) \neq I$	110011	D _R	D _C	I
	SEQ r, M	※	Skip if general register is equal to memory	Skip if $(r) = (M)$	100010	D _R	D _C	R _N
Transfer instruction	SNE r, M	※	Skip if general register is not equal to memory	Skip if $(r) \neq (M)$	100011	D _R	D _C	R _N
	LD r, M		Load memory to general register	$r \leftarrow (M)$	100100	D _R	D _C	R _N
	ST M, r		Store general register to memory	$M \leftarrow (r)$	100101	D _R	D _C	R _N
	MVSR M ₁ , M ₂		Move memory to memory in the same row	$(D_R, D_{C1}) \leftarrow (D_R, D_{C2})$	011111	D _R	D _{C1}	D _{C2}
	MVIMM, I		Move immediate data to memory	$M \leftarrow I$	001111	D _R	D _C	I
	MVGD r, M		Move memory to destination memory referring to G-register and general register	$[(G), (r)] \leftarrow (M)$	100110	D _R	D _C	R _N
	MVGSM, r		Move source memory referring to G-register and general register to memory	$M \leftarrow [(G), (r)]$	100111	D _R	D _C	R _N
Input and output instruction	IN1 M, C		Input IN1 port data to memory	$M \leftarrow [IN1]_C$	111000	D _R	D _C	C _N
	OUT1 C, M		Output contents of memory to OUT1 port	$[OUT1]_C \leftarrow (M)$	111011	D _R	D _C	C _N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC 6bit	A 2bit	B 4bit	C 4bit
Input and output instruction	IN2 M, C		Input IN2 port data to memory	$M \leftarrow [IN2]_C$	111001	D _R	D _C	C _N
	OUT2 C, M		Output contents of memory to OUT2 port	$[OUT2]_C \leftarrow (M)$	111100	D _R	D _C	C _N
	IN3 M, C		Input IN3 port data to memory	$M \leftarrow [IN3]_C$	111010	D _R	D _C	C _N
	OUT3 C, M		Output contents of memory to OUT3 port	$[OUT3]_C \leftarrow (M)$	111101	D _R	D _C	C _N
Logical operation instruction	ORR r, M		Logical OR of general register and memory	$r \leftarrow (r) \vee (M)$	010110	D _R	D _C	R _N
	ANDR r, M		Logical AND of general register and memory	$r \leftarrow (r) \wedge (M)$	010111	D _R	D _C	R _N
	ORIM M, I		Logical OR of memory and immediate data	$M \leftarrow (M) \vee I$	000110	D _R	D _C	I
	ANIM M, I		Logical AND of memory and immediate data	$M \leftarrow (M) \wedge I$	000111	D _R	D _C	I
	XORIM M, I		Logical exclusive OR of memory and immediate data	$M \leftarrow (M) \oplus I$	001110	D _R	D _C	I
	XORR r, M		Logical exclusive OR of general register and memory	$r \leftarrow (r) \oplus (M)$	011110	D _R	D _C	R _N
Bit judge instruction	TMTR r, M	※	Test general register bits by memory bits, then skip if all bits specified are true	Skip if $r[N(M)] = \text{all "1"}$	100000	D _R	D _C	R _N
	TMFR r, M	※	Test general register bits by memory bits, then skip if all bits specified are false	Skip if $r[N(M)] = \text{all "0"}$	100001	D _R	D _C	R _N
	TMT M, N	※	Test memory bits, then skip if all bits specified are true	Skip if $M(N) = \text{all "1"}$	110101	D _R	D _C	N
	TMF M, N	※	Test memory bits, then skip if all bits specified are false	Skip if $M(N) = \text{all "0"}$	110111	D _R	D _C	N

INST. GR.	MNEMONIC	SKIP FUNCTION	EXPLANATION OF FUNCTION	EXPLANATION OF OPERATION	MACHINE LANGUAGE (16bit)			
					IC 6bit	A 2bit	B 4bit	C 4bit
Bit judge instruction	TMTN M, N	※	Test memory bits, then not skip if all bits specified are true	Skip if M(N) = not all "1"	110100	D _R	D _C	N
	TMFN M, N	※	Test memory bits, then not skip if all bits specified are false	Skip if M(N) = not all "0"	110110	D _R	D _C	N
Subroutine instruction	CALL ADDR ₁		Call subroutine	STACK ← (PC) + 1 and PC ← ADDR ₁	1010	ADDR ₁ (12bit)		
	RN		Return to main routine	PC ← (STACK)	111111	00	—	—
	RNS	※	Return to main routine and skip unconditionally	PC ← (STACK) and skip	111111	01	—	—
Jump instruction	JUMP ADDR ₁		Jump to the address specified	PC ← ADDR ₁	1011	ADDR ₁ (12bit)		
Other instruction	DAL ADDR ₂ , r		Load program memory in page 0 to DATA register	DATA ← [ADDR ₂ + (r)] _P in page 0	111110	ADDR ₂ (6bit)	R _N	
	WAIT P		At P = "0" H, the condition is CPU waiting (Soft wait mode)	Wait at condition P	111111	10	0000	P
			At P = "1" H, except for clock generator, all function is waiting (Hard wait mode)					
	CKSTP		Clock generator stop	Stop clock generator in $\overline{\text{HOLD}} = "0"$	111111	10	1000	—
	NOOP		No operation	—	111111	11	—	—

(Note 1) Low order 4 bits out of the program memory address 10 bits designated by DAL instruction are to be indirectly address according to contents of the general register. DAL instruction execution time is 80μs (2 machine cycles).

(Note 2) MVGS instruction execution time is 80μs (2 machine cycles).

○ I/O map

All ports within the device are expressed by a matrix of 6 I/O instructions (OUT1~3 instruction, IN1~3 instruction) and a 4bit code number.

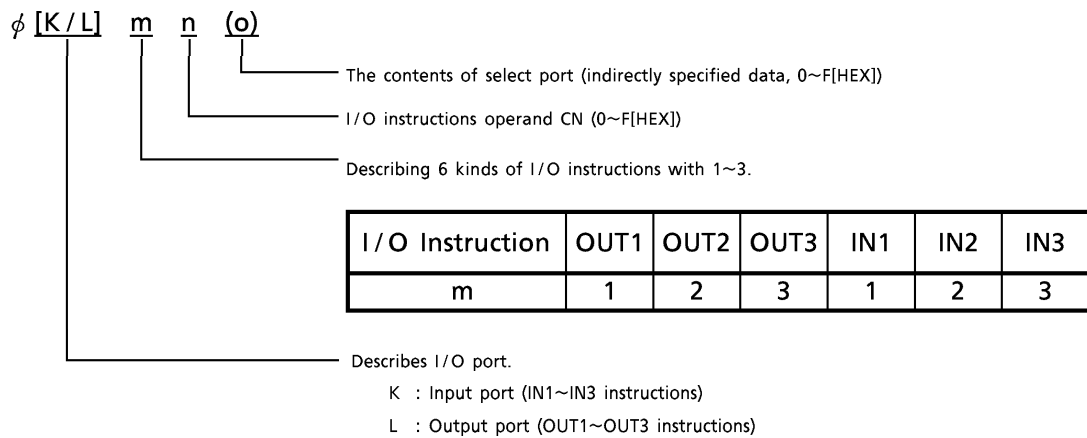
The allocation of these ports is described as I/O map in the following page. In this I/O map, port names treated in execution of I/O instructions are assigned on the axis of ordinates and port code numbers on the axis of abscissas. The G-register and data register are treated also as ports. The OUT1~3 instruction and IN1~3 instruction are designated at an output port and input port, respectively.

(Note 1) The oblique lined ports shown on the I/O map are actually not existed in the device. If data are outputted to a non-existing output port when an output instruction is executed, other ports or the contents of data memory are not especially affected. If a non-existing input port is specified when an input instruction is executed, the contents loaded to data memory is all "1".

(Note 2) Ports with *mark out of output ports on the I/O map are unused ports. Data outputted to these ports will become "don't care".

(Note 3) The contents of the ports expressed by 4 bits, Y1 corresponds to LSB of data of the data memory and Y8 correspond to MSB.

Ports that are designated by 6 I/O instructions and No. C are expressed in coding as follows.



(Example) The G-register setting is allotted in the code "F" of OUT1 instruction. At this time the encoded expression is " ϕ L1F".

I/O map

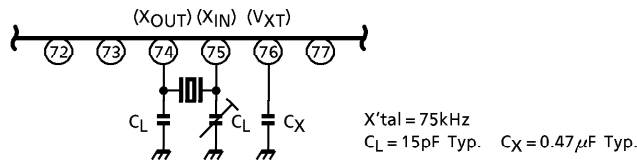
I/O CODE	φL1 OUT1 INSTRUCTION								φL2 OUT2 INSTRUCTION								φL3 OUT3 INSTRUCTION								φK1 IN1 INSTRUCTION								φK2 IN2 INSTRUCTION								φK3 IN3 INSTRUCTION							
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8																
0	*	IF offset + 1		FM	AD SEL0	AD SEL1	REF SEL0	REF SEL1	A/D control	A/D control	A/D control	A/D control	AD0	AD1	AD2	AD3	A/D data	A/D data	A/D data	A/D data	AD0	AD1	AD2	AD3	A/D data	A/D data	A/D data	A/D data	AD0	AD1	AD2	AD3																
1	Programmable counter #1	#2	*		STA	DREF ON	AD1 ON	AD2 ON	SIO control	SIO control	SIO control	SIO control	f0	f1	f2	f3	IF data	IF data	IF data	IF data	AD4	AD5	BUSY	1	IF data	IF data	IF data	IF data	AD4	AD5	BUSY	1																
2	PA	PB	PC	PD	edge	SCK-INV	SCK-1/O	SIO ON	SIO control	SIO control	SIO control	SIO control	f4	f5	f6	f7	IF data	IF data	IF data	IF data					IF data	IF data	IF data	IF data																				
3	R0	R1	R2	R3	STA	SO-1/O	4/8 bit	*	SIO control	SIO control	SIO control	SIO control	f8	f9	f10	f11	IF data	IF data	IF data	IF data	BUSY	COUNT	SIO F/F	1	SIO control data	SIO control data	SIO control data	SIO control data	BUSY	COUNT	SIO F/F	1																
4	*	SCON	IF/INT	*	S0	S1	S2	S3	SIO output data	SIO output data	SIO output data	SIO output data	f12	f13	f14	f15	IF data	IF data	IF data	IF data	S0	S1	S2	S3	SIO input data	SIO input data	SIO input data	SIO input data	S0	S1	S2	S3																
5	STA/STP	Manual	G0	G1	S4	S5	S6	S7	SIO output data	SIO output data	SIO output data	SIO output data	f16	f17	f18	f19	IF data	IF data	IF data	IF data	S4	S5	S6	S7	SIO input data	SIO input data	SIO input data	SIO input data	S4	S5	S6	S7																
6	MUTE	I/O	POL	UNLOCK	2Hz F/F	Timer	#4	#5	Timer reset	TEST data	TEST data	TEST data					UNLOCK	IN1	UNLOCK	IN1	2Hz F/F	10Hz	100Hz	F/F	STOP	Timer	Timer	Timer	Timer	Timer	Timer																	
7	UNLOCK RESET	OTC	OT	HZ	K51	K52	K54	K58	Key scan start	Key scan start	Key scan start	Key scan start	UNLOCK	ENABLE	IN1	UNLOCK	IN1	UNLOCK	IN1	F/F	ENABLE	IN1	UNLOCK	IN1	Key scan digit	Key scan digit	Key scan digit	Key scan digit	Key scan digit	Key scan digit	Key scan digit																	
8	PW0/B0	PW1/B1	PW2/B2	PW3/B3	KE1	KE2	KE4	KE8	Key scan end	Key scan end	Key scan end	Key scan end	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	KR1	KR2	KR4	KR8	Key input data	Key input data	Key input data	Key input data	Key input data	Key input data	Key input data	Key input data																
9	PW4/B4	PW5/B5	PW6/B6	PW7/B7	KC0	KC1	KC2	KC3	Key scan control	Key scan control	Key scan control	Key scan control	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	K0	K1	K2	K3	Key input data	Key input data	Key input data	Key input data	Key input data	Key input data	Key input data	Key input data																
A	PW8	PW9	PW10	PW11	KSD1	KSD2	KSD4	KSD8	key scan data select	key scan data select	key scan data select	key scan data select	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	K0	K1	K2	K3	Key scan data	Key scan data	Key scan data	Key scan data	Key scan data	Key scan data	Key scan data	Key scan data																
B	PWM ON	BUZR ON	PWM/BUZR	Buffer transfer									UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK	UNLOCK					Key scan data	Key scan data	Key scan data	Key scan data	Key scan data	Key scan data	Key scan data	Key scan data																
C	#0	#1	#2	#3									HOLD	1	1	1	HOLD	1	1	1																												
D									SEG data select	SEG data select	SEG data select	SEG data select																																				
E					S1	S2	S4	S8																																								
F	#0	#1	#2	#3	COM1	COM2	COM3	SEG	SEG-1 data	SEG-1 data	SEG-1 data	SEG-1 data	COM1	COM2	COM3	SEG	SEG	SEG	SEG	I/O control select	I/O control select	I/O control select	I/O control select	COM1	COM2	COM3	SEG	SEG	SEG	SEG	SEG	SEG																
					COM1	COM2	COM3	SEG	SEG-2 data	SEG-2 data	SEG-2 data	SEG-2 data	COM1	COM2	COM3	SEG	SEG	SEG	SEG	I/O control data	I/O control data	I/O control data	I/O control data	COM1	COM2	COM3	SEG	SEG	SEG	SEG	SEG	SEG	SEG															
					COM1	COM2	COM3	SEG					IO-0	IO-1	IO-2	IO-3	IO-3	IO-3	IO-3	IO-3	d0	d1	d2	d3	IO-0	IO-1	IO-2	IO-3	IO-3	IO-3	IO-3	IO-3	IO-3															
													d4	d5	d6	d7	d4	d5	d6	d7	d4	d5	d6	d7	d4	d5	d6	d7	d4	d5	d6	d7	d4	d5	d6	d7												
													d8	d9	d10	d11	d8	d9	d10	d11	d8	d9	d10	d11	d8	d9	d10	d11	d8	d9	d10	d11	d8	d9	d10	d11												
													d12	d13	d14	d15	d12	d13	d14	d15	d12	d13	d14	d15	d12	d13	d14	d15	d12	d13	d14	d15	d12	d13	d14	d15												

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○ Connection of crystal resonator

Connect a 75kHz crystal resonator to crystal oscillator terminal of the device (XIN, XOUT) as shown below.

This oscillation signal is supplied to clock pulse generator, reference frequency divider and generates various CPU timing signals and reference frequency signals. The crystal circuit uses voltage (VXT = 1.3V Typ.) supplied from a built-in regular voltage circuit as power supply. Because of this, it can stabilize the crystal resonator and reduce the consumption current.



(Note) Use a crystal oscillator of good starting characteristic such as low CI value.

○ System reset

When "L" level signal is input to the $\overline{\text{RESET}}$ terminal or more than 0~1.8V is supplied to the VDD terminal (Power on reset), system reset is applied to a device. After standby period of 100ms has passed after system reset, a program will start from address 0.

Since it normally uses POWER ON RESET function, fix $\overline{\text{RESET}}$ terminal at "H" level.

(Note 1) During system reset and the subsequent stand-by period, LCD common and segment outputs are fixed at "L" level.

(Note 2) The internal ports shown in the following table are fixed after system reset, but the other ports are not fixed. Accordingly it is necessary to initialize them by program.

Fixed internal port

PORT FIXED TO "0"	PORT FIXED TO "1"
SC _{ON} bit (ϕ L14)、Manual bit (ϕ L15) IO, POL, UNLOCK bit (ϕ L16) DO1 control port (ϕ L17) PWM _{ON} , BUZR _{ON} , PWM/BUZR, Transfer bit (ϕ L1B) Test port (ϕ L1C、 ϕ L26) CKSTP MODE bit (ϕ L1E) AD control port (ϕ L20、 ϕ L21) SIO control port (ϕ L22、 ϕ L23) Timer port (ϕ K26) Key scan start, control port (ϕ L27、 ϕ L290~ ϕ L295) V _{LCD} OFF bit (ϕ L2FF) IO-1~IO-6 IO control port (ϕ L3F0~ ϕ L3F5)	Reference port (ϕ L13) MUTE bit (ϕ L16) IF/ $\overline{\text{IN}}$ 1 (ϕ L14) Key scan end port (ϕ L28) DISP OFF bit (ϕ L2FF) SEG bit (LCD/IO switching bit ; ϕ L2E0~ ϕ L2EF、 ϕ L2F0~ ϕ L2FE)

○ Backup mode

When CKSTP or WAIT instruction is executed, the following three kinds of backup modes are selected.

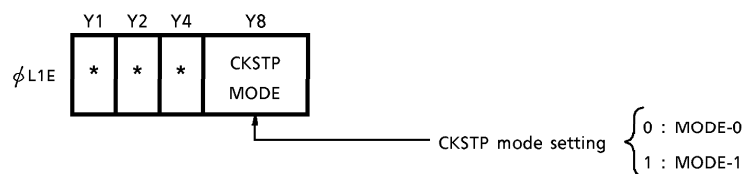
1. Clock stop mode

It is a function to stop operating system and holds the operation state of device just before stop with low current consumption (below $1\mu\text{A}$ at $V_{DD}=3.0\text{V}$). At this time the crystal oscillation stops and the LCD display driver terminal and output ports are all fixed at "L" level or OFF state automatically. The supply voltage can be reduced to 1.0V in this clock stop mode.

Program stops at the address of executing CKSTP instruction when CKSTP instruction is executed. If clock stop mode is released, the next address is executed after lapse of stand-by time of 100ms.

(1) Clock stop mode setting

The clock stop mode setting has two kinds of mode. The setting is selected by CKSTP MODE bit. This bit is accessed when OUT1 instruction designated [CN = EH] in the operand is executed.



① MODE-0

In this mode, CKSTP instruction is executed while $\overline{\text{HOLD}}$ terminal is "L" level, it becomes clock stop mode. If CKSTP instruction is executed while $\overline{\text{HOLD}}$ terminal is "H" level, it does the same operation as that of NOOP instruction.

② MODE-1

In this mode, CKSTP instruction is executed regardless of the level of $\overline{\text{HOLD}}$ terminal, it becomes clock stop mode.

(Note) The PLL will be off state while CKSTP instruction is executed.

(2) Released condition of clock stop mode

① MODE-0

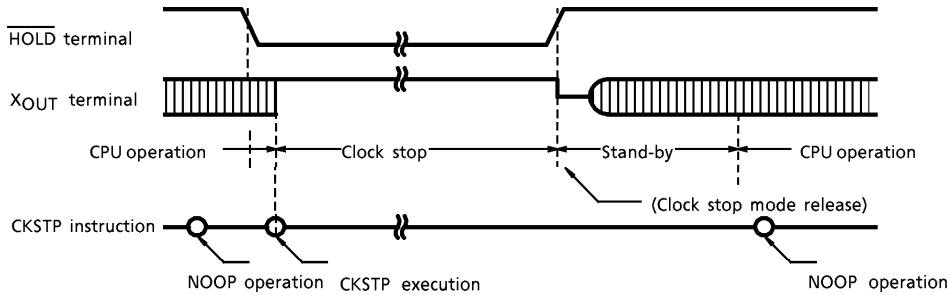
When clock stop mode is set by this mode, the clock stop mode is released when $\overline{\text{HOLD}}$ terminal is "H" level or changing the input condition of I/O port (P1-0~3) set at input port.

② MODE-1

When clock stop mode is set by this mode, the clock stop mode is released by $\overline{\text{HOLD}}$ terminal or changing the input condition of I/O port (P1-0~3) set at input port.

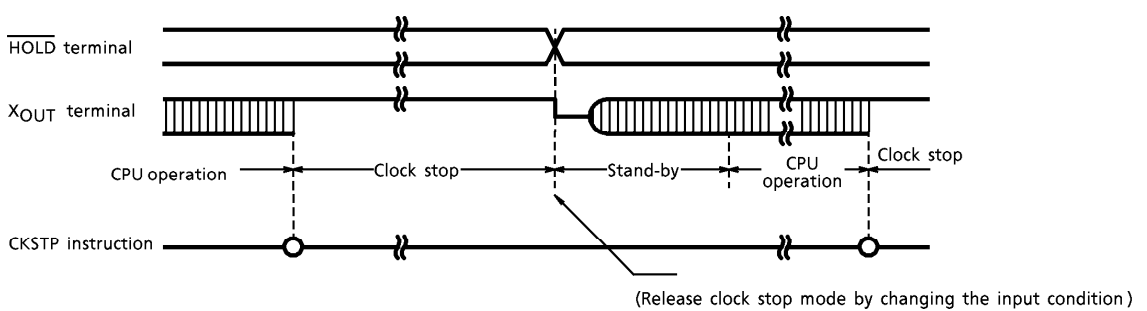
(3) Clock stop mode timing

① MODE-0



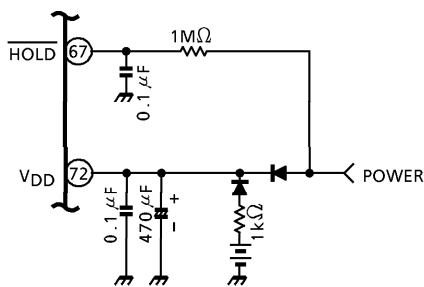
It sets to clock stop mode when CKSTP instruction is executed while $\overline{\text{HOLD}}$ terminal is "L" level.

② MODE-1

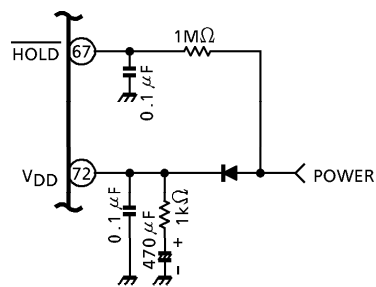


(It sets to clock stop mode whenever CKSTP instruction is executed.)

(4) Example of circuit (example of MODE-0 circuit)



Example of backup circuit using battery



Example of backup circuit using capacitor

2. Wait mode

This mode stops system and holds the operation state of a device just before stop and therefore reduces current consumption. In this mode there are two kinds as follows:

- HARD WAIT mode
- SOFT WAIT mode

Program stops at the address of executing WAIT instruction when WAIT instruction is executed. If WAIT mode is released, the next address will be executed without stand-by time.

(1) SOFT WAIT mode

It stops only CPU operation internal a device when WAIT instruction is executed at designated operand port [P=0H]. At this time others such as crystal oscillator and display circuit, etc. operate properly. SOFT WAIT mode is efficient in reducing current consumption for use in the program of clock function at clock operation.

(Note) Current consumption differs depending on the program.

(2) HARD WAIT mode

It stops all operations except crystal oscillation circuit when WAIT instruction is executed at designated operand port [p=1H]. For this reason, this mode can reduce further current consumption than SOFT WAIT mode. At this time, CPU and display circuit stop operation and LCD display output terminals are all fixed at "L" level automatically.

(10 μ A Typ. at V_{DD} = 3V)

(3) WAIT mode setting

It will be in waiting condition whenever WAIT instruction is executed.

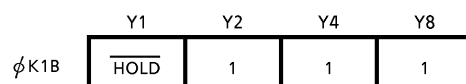
(Note) It will be PLL off condition during HARD WAIT mode but not during SOFT WAIT mode. Therefore, it is necessary to set PLL off condition by program before SOFT WAIT mode is executed.

(4) Released condition of WAIT mode

The WAIT mode is released under one of following conditions;

1. When the input level of $\overline{\text{HOLD}}$ terminal changes,
2. When "H" level is inputted to key input terminal (K0~K3) (only when key input mode)
3. When 2Hz timer F/F is set to "1", (only SOFT WAIT mode)
4. When input level of I/O port (P1-0~3) set in input port is changed,

3. $\overline{\text{HOLD}}$ input port



The $\overline{\text{HOLD}}$ terminal is used as an input port. Data is read in the data memory when IN1 instruction designated [C_N=BH] in the operand.

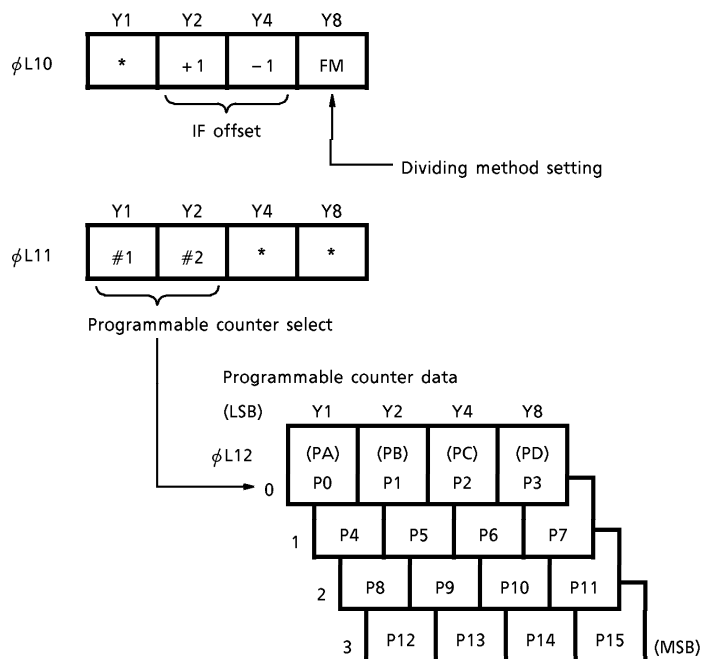
When this clock stop mode is set, it is necessary to access to this port before CKSTP instruction is executed. It may not be clock stop mode when CKSTP instruction is executed without accessing to this port.

○ Programmable counter

It consists of external 2-modulus prescaler, 4bit + 12bit programmable counter and port to control these. Programmable counter controls ON/OFF according to the contents of reference port.

1. Programmable counter control port

It is a port to control frequency division number, frequency division system and IF correction (IF offset) at FM band.



(Note) Whenever accessing to $\phi L12$, the $\phi L11$ data is +1 incremented.

The frequency division system and IF offset are accessed by OUT1 instruction designated [C_N = 0H] in the operand.

The frequency division number setting is accessed by OUT1 instruction designated [C_N = 1H, 2H] in the operand and write to PA~PD bit ($\phi L12$).

This port is divided by the programmable counter select port ($\phi L11$) and the programmable counter data corresponding to the select port is set by setting data to them.

After the programmable data select is set to "3", set the programmable counter data (P12~P15) and all of P0~P15 data are updated. Because of this, make sure to access to P12~P15 port and set the P12~P15 port data at last even if changing only partially.

The programmable counter select is +1 incremented whenever accessing to the programmable counter data ($\phi L12$). Normally the setting can easily be done by setting "0" to the programmable counter select port and accessing to the programmable counter data successively.

2. Setting of frequency division system

The pulse swallow system or the direct frequency division system are selected according to FM port.

At AM band mode, the direct frequency division system is selected. When SW band, FM band or VHF/TV band mode, it selects the pulse swallow system which combines with external 2-modulus prescalers of TD6134AF, TD7101F and TD7103F.

FM	FREQUENCY DIVISION SYSTEM	EXAMPLE OF RECEIVING BAND	OPERATION FREQUENCY RANGE	INPUT TERMINAL	FREQUENCY DIVISION NUMBER (Note 2)	PRESCALER
0	Direct frequency division system	MW/LW	0.5~12MHz	AM _{IN}	n	None
1	(1/15 or 1/16) Pulse swallow system	SW	(Note 1) 1.5~35MHz	FM _{IN}	n	TD7101F
	1/4 × (1/15 or 1/16) Pulse swallow system	FM	(Note 1) 50~150MHz		4·n	TD6134AF TD7101F TD7103F
	1/8 × (1/15 or 1/16) Pulse swallow system	VHF/TV	(Note 1) 50~250MHz		8·n	TD6134AF TD7103F

(Note 1) It indicates the input frequency range for each prescaler of TD6134F, TD7101F and TD7103F.

(Note 2) The “n” denotes a programmed divided frequency value.

3. IF correction function at FM band

In the pulse swallow system, the actual frequency division number can be ±1 variable without changing programmable frequency division value by ΔIF + 1 port and ΔIF – 1 port.

This is used for IF offset condition at FM band.

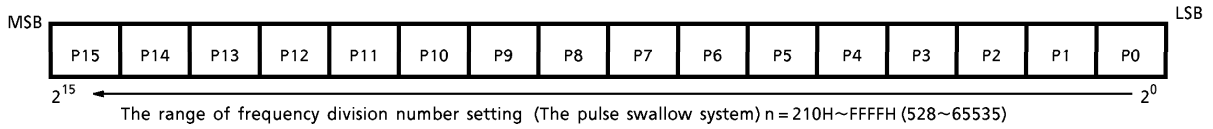
At the direct division system, the IF offset function does not operate.

ΔIF + 1	ΔIF – 1	FREQUENCY DIVISION NUMBER (VHF)	FREQUENCY DIVISION NUMBER (FM OR HF)
0	0	2·n	n
0	1	2·(n – 1)	n – 1
1	0	2·(n + 1)	n + 1
1	1	Inhibit	Inhibit

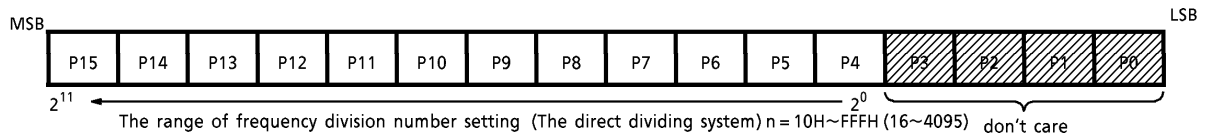
4. Setting of frequency division number

Set frequency division number of the program counter in binary number to P0~P15bit.

- The pulse swallow system (16 bits)



- The direct frequency division system (12 bits)



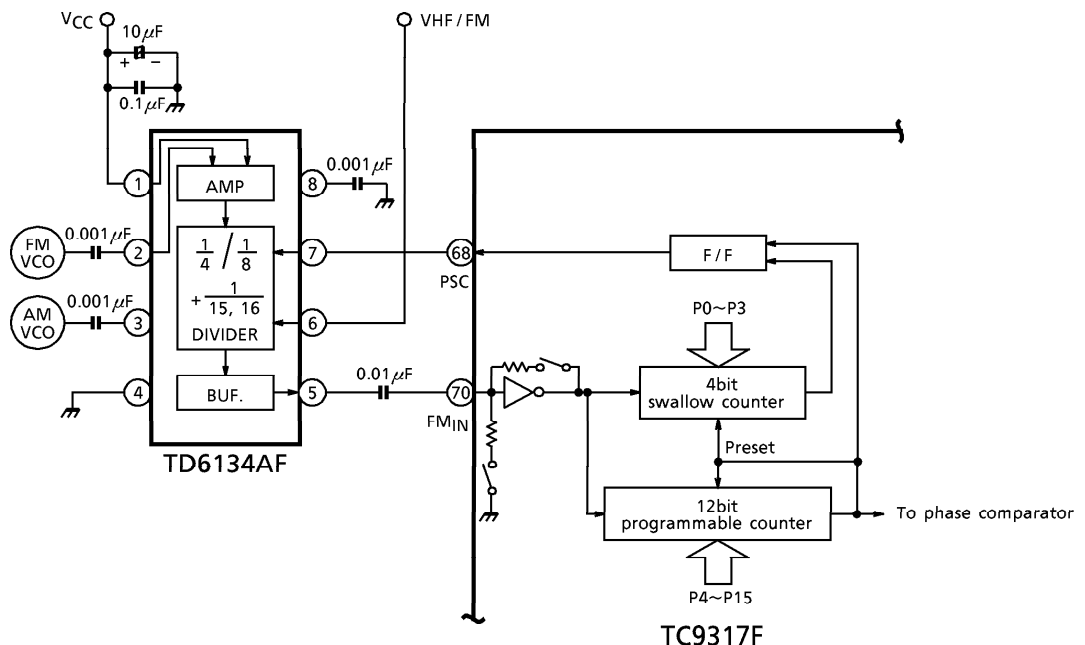
(Note) Since offset is not provided to the program counter, a programmed division number will become an actual division number. However when a prescaler is used, the actual dividing value will become 4 times of the programmed value in case of FM band mode and 8 times at VHS/TV band mode.

(Note) In the direct frequency division system, the P0~P3 ports data (ϕ L11) become unconcerned and P4 port are used as LSB.

5. Programmable counter circuit configuration

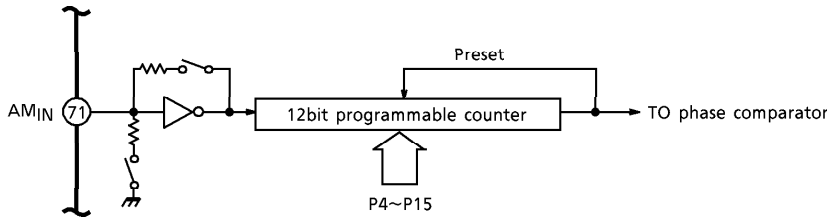
- Circuit configuration of the pulse swallow system

The circuit consists of : 2-modulus prescaler (TD6134AF, TD7101F, TD7103F), 4bit swallow counter and 12bit binary counter. At FM band, 1/4 divider is added to the front stage of the prescaler and 1/8 divider is added at VHF/TV band. The diagram with prescaler (TD6134AF) as shown below.



● Circuit configuration of direct frequency division system

In this case, the external prescaler is unnecessary and a 12bit programmable counter is used.



(Note) Both FM_{IN} and AM_{IN} terminals have built-in an amplifier respectively, and are operable at small amplitude with coupled capacitors. When the input terminal not selected according to the frequency division system and PLL off mode (Setting be reference port) the input is pull-down.

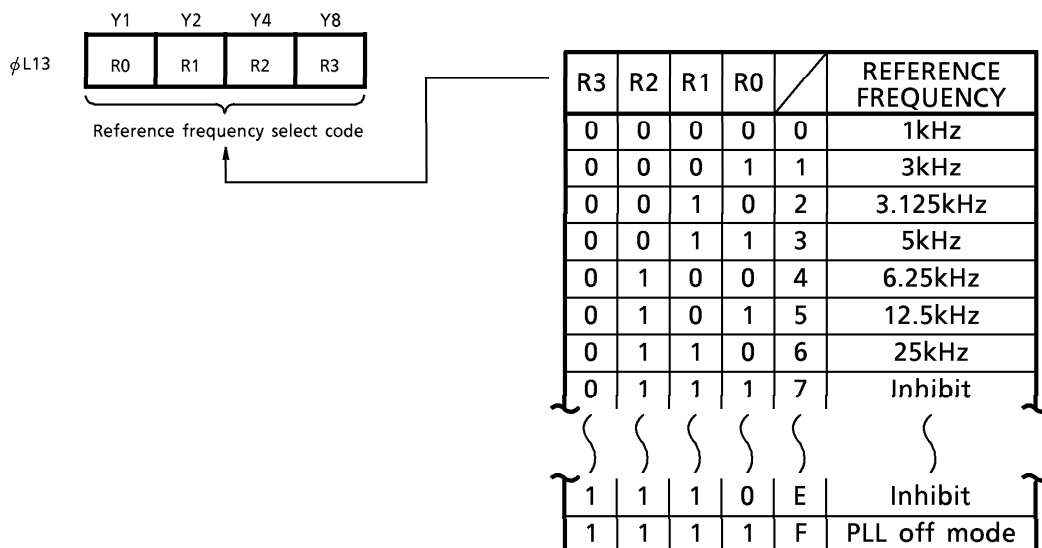
○ Reference frequency divider

This frequency divider generates 7 kinds of PLL reference frequency signals 1, 3, 3.125, 5, 6.25, 12.5 and 25kHz by dividing external 75kHz crystal oscillation signal.

This frequency selection is executed by the contents of reference port. The selected signal is used as reference frequency of the phase comparator as described below. According to the contents of the reference port, PLL ON/OFF is performed.

1. Reference port

It is an internal port to select the 7 kinds of reference frequency signals. This port is accessed when OUT1 instruction designated [C_N=3H] in the operand (φL13) is executed. When the contents of reference port are all "1", the programmable counter, IF counter and reference counter will stop and be in PLL off mode.



○ Phase comparator & lock detection port

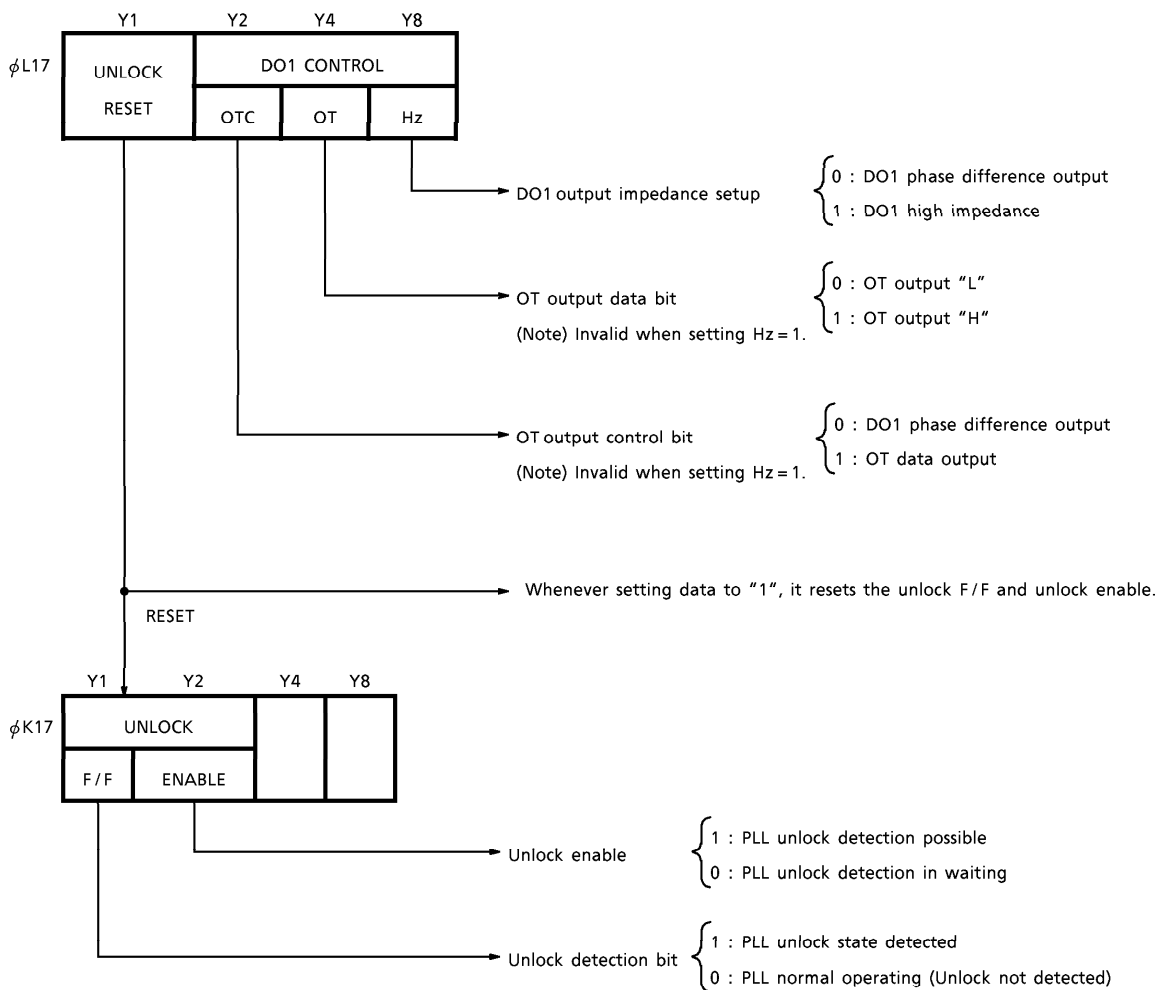
The phase comparator compares the phase between reference frequency signal supplied from reference frequency divider and programmable counter dividing output to output the difference. It controls VCO through a low pass filter so that the frequency and phase difference of these two signals can be equivalent.

Because two tri-state buffers DO1 and DO2 terminals are outputted from the phase comparator, the filter constant can be optimally designed for each FM/VHF band and AM band.

The DO1 terminal is usable as general output terminal by means of DO1 control port. This terminal is capable of setting to high impedance. By using two terminals of DO1 & DO2, it is possible to improve the characteristics of PLL loop lock-up type, etc.

The lock detection port is capable of detecting the lock state of PLL circuit.

1. DO1 control port and unlock detection port



UN3	UN2	UN1		PHASE DIFFERENCE
0	0	0	0	$0\mu\text{s} \sim +6.66\mu\text{s}$
0	0	1	1	$-13.3\mu\text{s} \sim 0\mu\text{s}, +6.66\mu\text{s} \sim +20\mu\text{s}$
0	1	0	2	$-13.3\mu\text{s} \sim -26.6\mu\text{s}, +20\mu\text{s} \sim +33.3\mu\text{s}$
0	1	1	3	$-26.6\mu\text{s} \sim -40\mu\text{s}, +33.3\mu\text{s} \sim +46.6\mu\text{s}$
1	0	0	4	$-40\mu\text{s} \sim -53.3\mu\text{s}, +46.6\mu\text{s} \sim +60\mu\text{s}$
1	0	1	5	$-53.3\mu\text{s} \sim -66.6\mu\text{s}, +60\mu\text{s} \sim +73.3\mu\text{s}$
1	1	0	6	$-66.6\mu\text{s} \sim -80\mu\text{s}, +73.3\mu\text{s} \sim +86.6\mu\text{s}$
1	1	1	7	Under $-80\mu\text{s}$, Over $+86.6\mu\text{s}$

Each OTC, OT and Hz bit of DO1 control port is a control bit as below condition.

- DO1 output terminal is used as general output port.
- DO1 output terminal is set to high-impedance state without outputting DO1 output phase difference.

These are set by program according to the specification.

The UNLOCK F/F bit detects the phase difference between the programmable counter divider output and the reference frequency when the phase is about 180° shift. If the phase difference does not accord at this time, that is, if in unlock state, UNLOCK F/F will be set. UNLOCK F/F will be reset whenever setting "1" to UNLOCK RESET bit.

DO output detects the phase difference at the cycle of reference frequency. It's necessary to access the UNLOCK F/F that its has more time than a cycle of reference frequency after resetting the UNLOCK F/F. Because ENABLE bit is prepared. After confirm that UNLOCK enable bit sets to "1", UNLOCK F/F is accessed.

UNLOCK enable bit is reset whenever setting "1" to UNLOCK RESET bit.

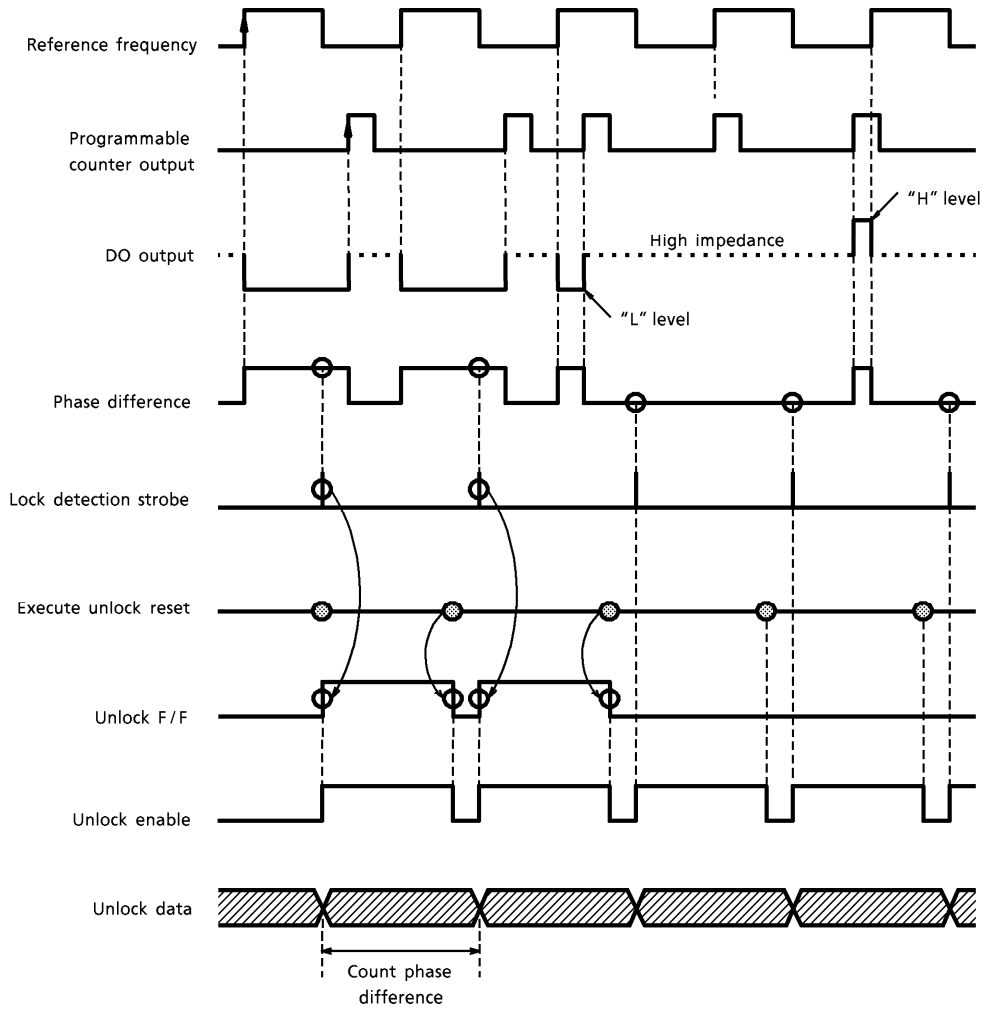
UNLOCK F/F detects when the phase is about 180° shift. It has the unlock data port that uses at more accurate detection of the phase difference. This port detects the phase difference as shown before table and is capable of detecting between $-80\mu\text{s} \sim +86.6\mu\text{s}$. However if setting to high reference frequency (at 25, 12.5kHz setting), it can't detect under the half cycle of the reference frequency.

UNLOCK data port detects data constantly in the phase width between $-180^\circ \sim 180^\circ$ of the reference frequency cycle. Normally after it is detected by UNLOCK F/F, the UNLOCK data will be referred.

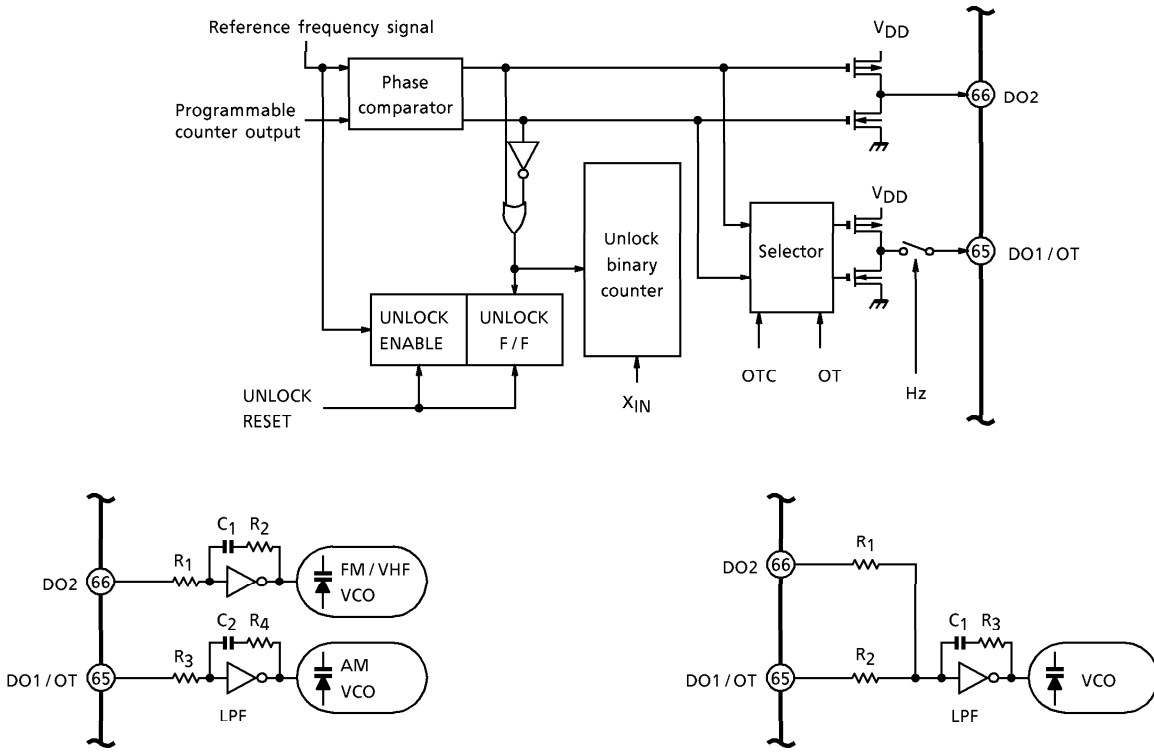
Control of each port and data loading are performed when OUT1/IN1 instruction designated [CN=7H or 8H] in the operand is executed.

(Note) When PLL OFF mode, the DO output becomes high impedance. However when DO1 is set as output port (OT output), the output data will be outputted directly.

2. Phase comparator and unlock port timing

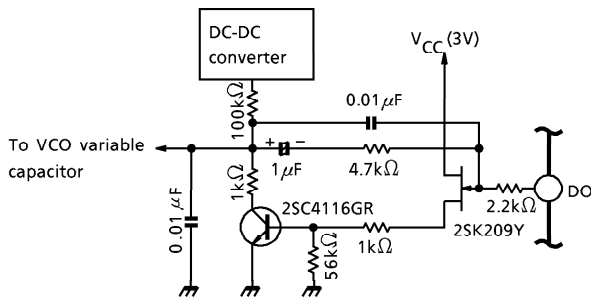


3. Phase comparator and unlock port circuit construction



In case of setting the filter constant for each band

In case of using LPF in common
(Switching of filter constant is done by setting DO1 to high impedance.)



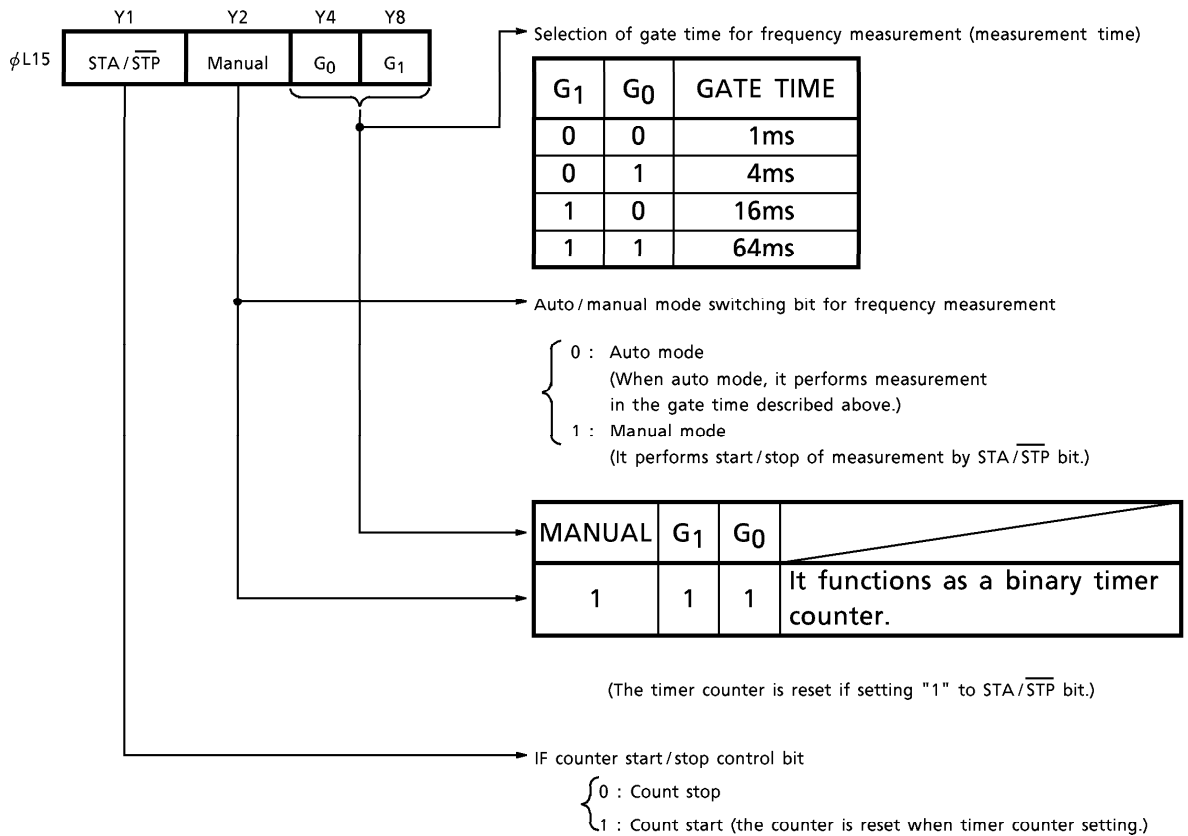
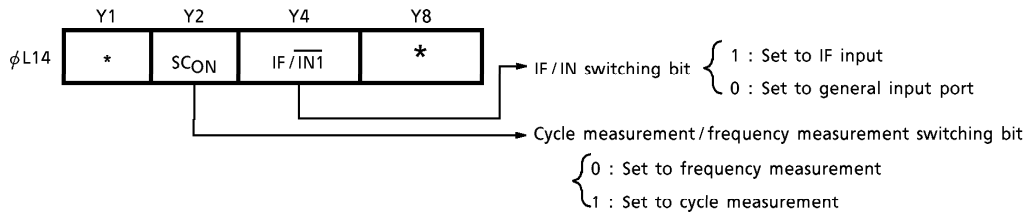
Example of active low pass filter circuit (for reference)

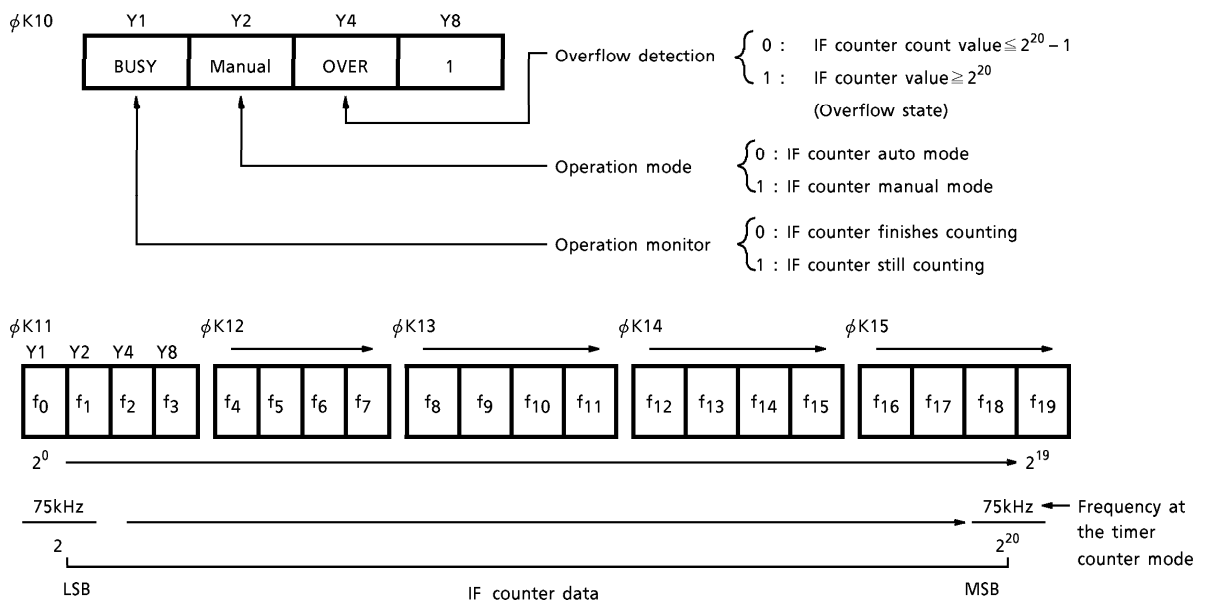
(Note) Since the above filter circuit is just an example, the actual circuit should be examined and designed in accordance with the system band construction and desired characteristics.

○ IF counter

It is a 20bit general IF counter for counting FM/AM intermediate frequency (IF) and can be used for detecting the auto stop signal, etc. It also has a function to measure the cycle of a low frequency pilot signal. When not counting IF, this general IF counter can be used as a timer. The IF counter consists of 20bit binary counter and control port.

1. IF counter control port, data port





(Note) The IF counter becomes disable at PLL off mode.
(It becomes enable at timer counter.)

(1) IF counter auto mode (frequency measurement)

The method to use IF counter auto mode is to set IF terminal to IF input by means of IF/IN switching bit and set $SCON$ bit to "0".

To set the gate time for IF input frequency bandwidth and STA/\overline{STP} bit to "1" while manual bit "0", then the IF counter is operated.

During the set gate time, the 20bit binary counter is inputted a clock pulse from IF terminal, counted the inputted pulse and finished. Whether IF counter counting has finished or not, it can be judged by referring to BUSY bit. The OVER bit becomes "1" when a pulse number of more than 20 count value is inputted.

The frequency inputted to IF input terminal can be measured by loading $f_0 \sim f_{19}$ IF data after judging that both BUSY bit and OVER bit are "0".

(2) IF counter Manual mode (frequency measurement)

When the IF frequency is measured by the gate time which controlled by an internal time base (10Hz, etc.), the manual mode is used.

In this mode, the setting IF counter input is set the same as auto mode. The $G0/G1$ bit data should be set except "1". Counting starts if setting Manual and STA/\overline{STP} bits to "1". Counting stops if setting "0" to STA/\overline{STP} bit and data will be loaded in binary.

(3) IF counter cycle mode (cycle measurement)

It is used for measuring the low frequency when it couldn't be measured by the frequency measurement.

In the cycle measurement, the cycle can be measured by judging this pulse number during the inputting reference clock (75kHz) to the 20bit binary counter.

As this input terminal, it uses as the IF input terminal, it switches to SC_{IN} terminal if setting SC_{ON} bit to "1".

It sets Manual, G0 and G1 bits to "0" when SC_{IN} setting.

The start of the cycle measurement is as same as the frequency measurement, the counting data is loaded after confirming the operation state by BUSY bit.

(Note) Input rectang waveform by means of DC coupling when SC_{IN} input.

(Note) The BUSY bit will not be "0" unless inputting a clock pulse to SC_{IN} bit.

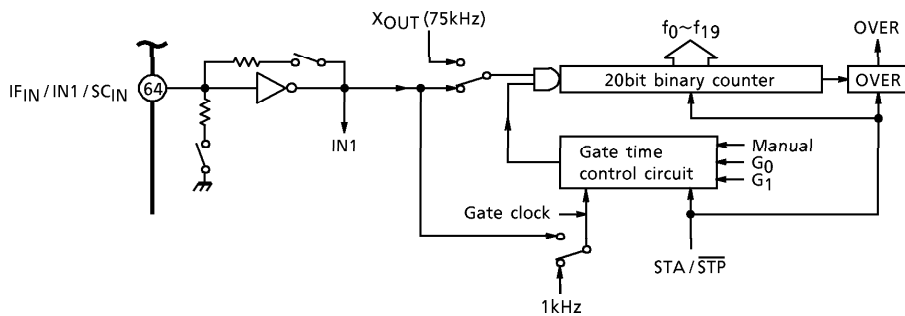
(4) Timer counter mode

When not using IF counter, it can be used as a timer binary counter.

If setting each Manual, G0 and G1 bit to "1", it will start counting a 75kHz clock in binary as reference clock.

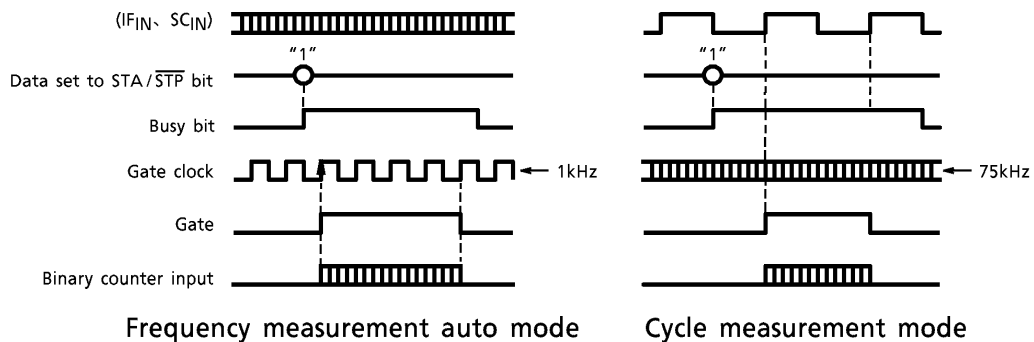
This counter will be reset whenever setting STA/ \overline{STP} bit to "1".

2. IF counter circuit configuration



The IF counter consists of input amplifier, gate time control circuit and 20bit binary counter. The IF counter becomes OFF state when PLL OFF mode, but when timer counter is setting, the IF counter can be operatable.

(Note) As an amplifier is built-in at IF_{IN} terminal, small amplitude operation is possible in coupling with capacitor.



○ LCD driver

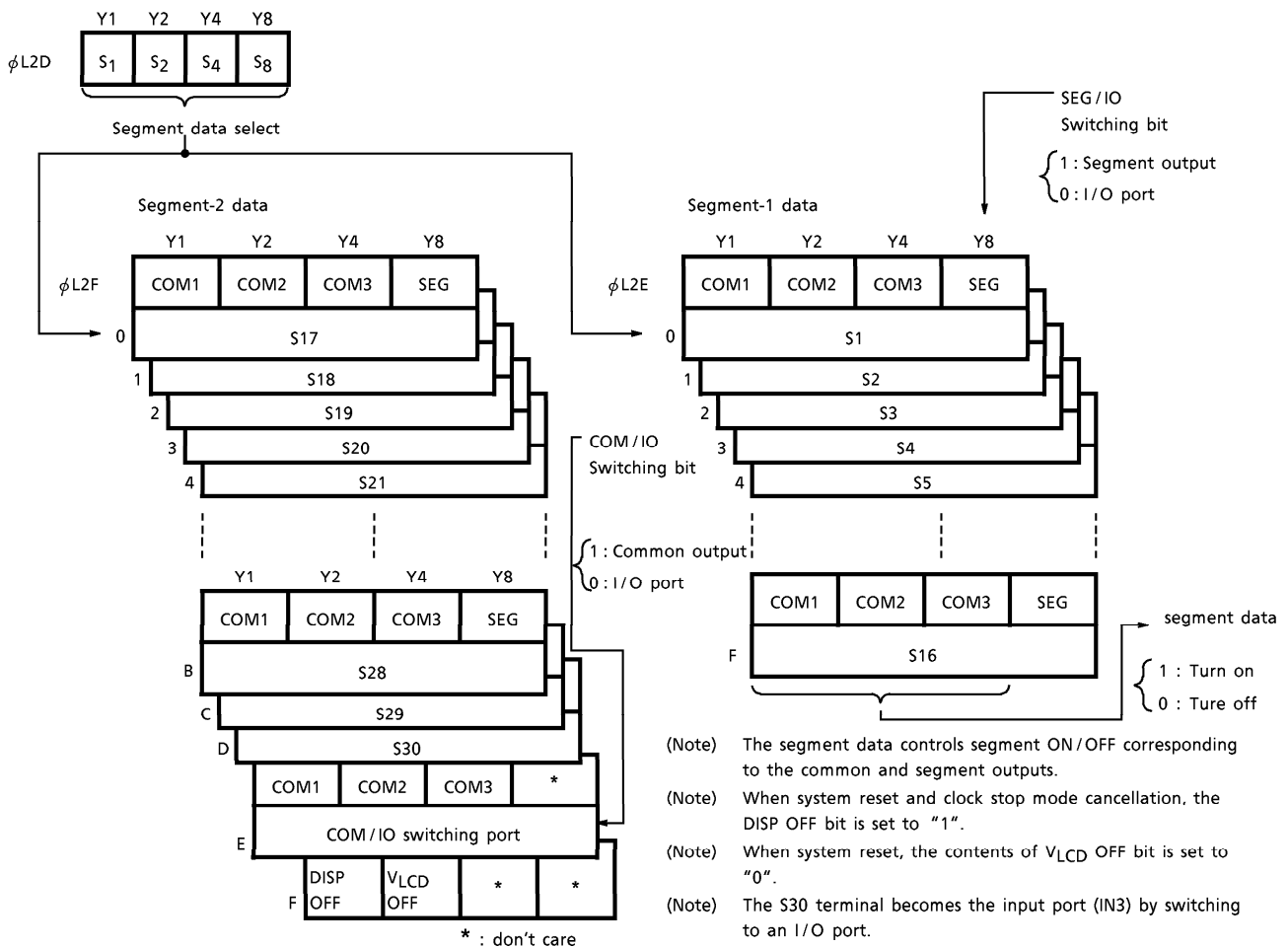
The LCD driver is of 1/3 duty and 1/2 bias drive (167Hz frame frequency) method. The common output outputs three voltage potentials of V_{LCD} , $V_{LCD}/2$ (V_{EE}) and GND. The segment output outputs two voltage potentials of V_{LCD} and GND. It is possible to display maximum 90 segments by combining three common outputs and 30 segment outputs.

The LCD driver segment output of $S_{19} \sim S_{30}$ is used both as the key return output for loading key matrix data.

As the LCD driver is built-in a constant voltage circuit for display ($V_{EE} = 1.5V$) and voltage circuit to double ($V_{LCD} = 3.0V$), the contrast of LCD display will not change even if supply voltage varies. The LCD driver is capable of switching to I/O port in a unit of 1bit and can be programmed according to the system.

(In this case, set V_{LCD} OFF bit to "1" and connect V_{LCD} terminal to V_{DD} terminal to use.)

1. LCD driver port



The LCD driver control port consists of segment data select port and segment data port. These ports are accessed when OUT2 instruction designated [CN=DH-FH] in the operand is executed. The LCD driver can use both as I/O port and this control is done by SEG/IO control bit (ϕ L2E, ϕ L2F). It will be segment output if setting "1" to this bit and I/O port if "0".

The LCD driver segment data is set at the segment data port (ϕ L2E, ϕ L2F). The LCD display turns off if setting "0" to the segment data port and turns on if setting "1". The segment-2 data (ϕ L2FF) designated FH at the segment select port are DISP OFF bit and V_{LCD} OFF bit. The DISP OFF bit can turn off LCD display completely without setting segment data.

If setting "1" to this bit, the common output will be non-selected waveform and the LCD display will be completely OFF. The contents of the segment is held at this time and the preceding display will appear as it is if setting "0" to DISP OFF bit.

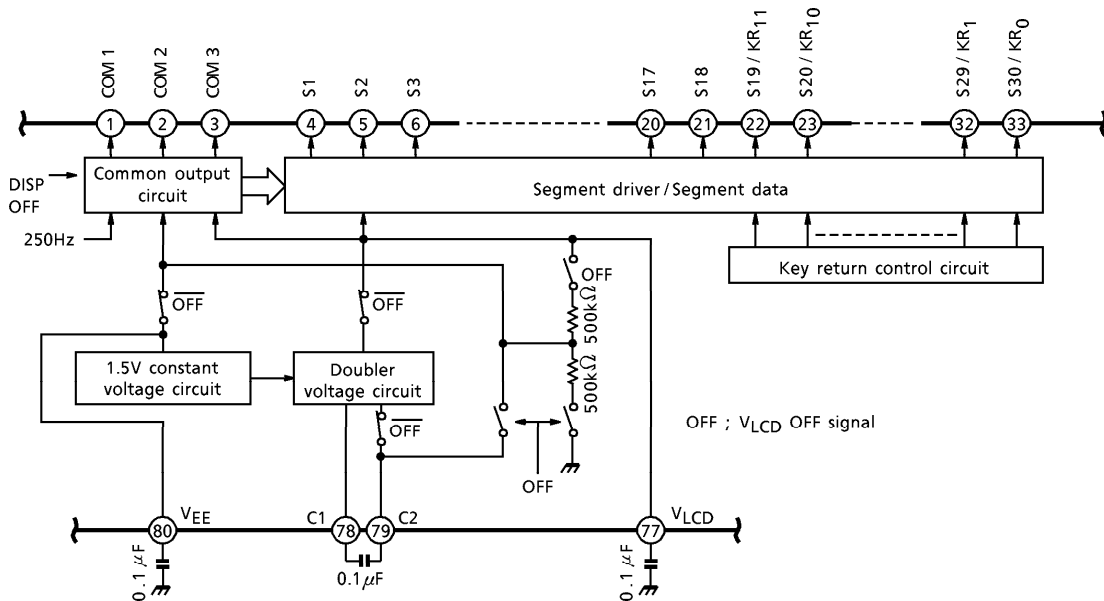
The segment data is rewritable during DISP OFF state. The DISP OFF bit be set to "1" after reset or after CKSTP instruction is executed.

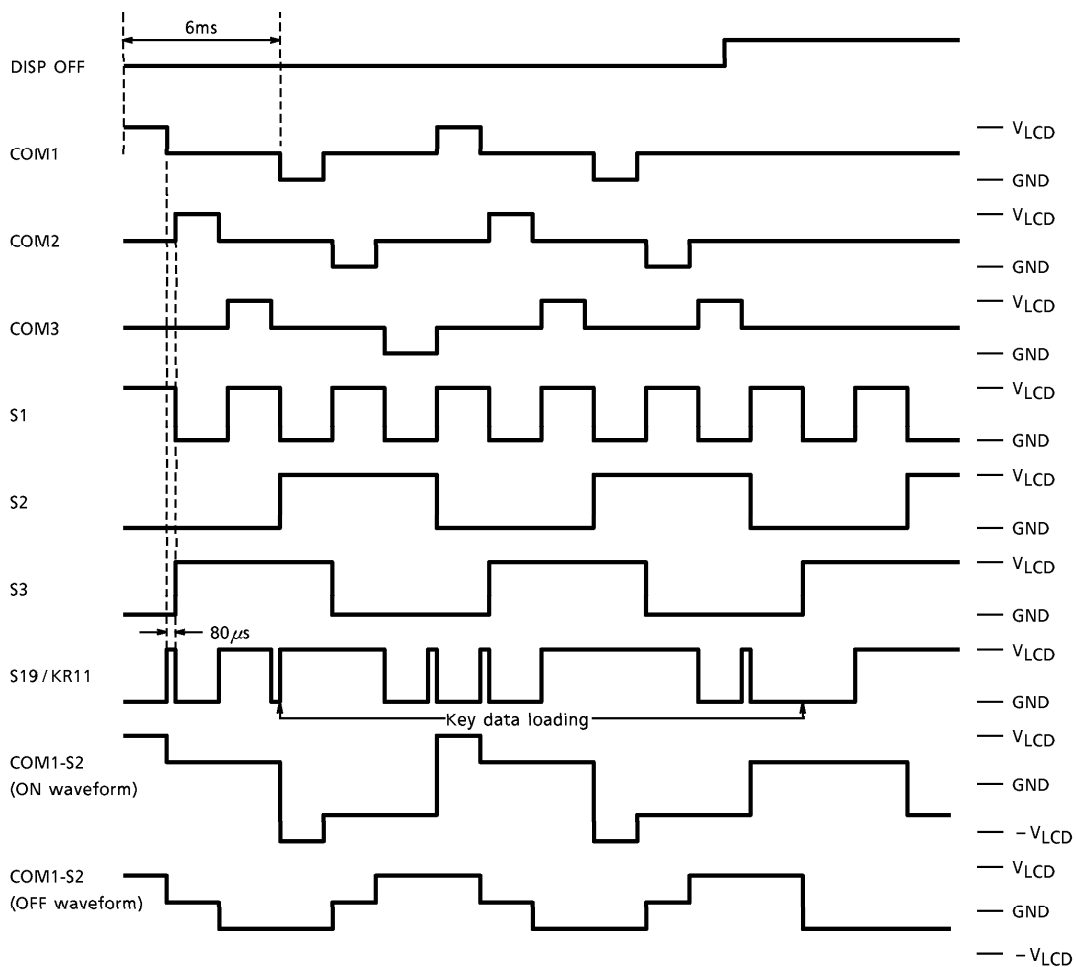
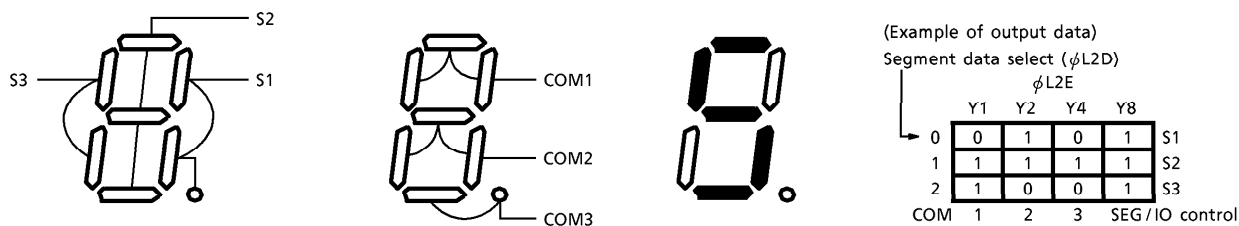
In case of using LCD terminal as I/O port, avoid LCD drive voltage supply booster (V_{LCD} terminal) as much as possible. The reason is that current consumption may increase dramatically by supply voltage (The relation between V_{LCD} and V_{DD} levels). In this case, the doubler voltage circuit is off state by setting "1" to V_{LCD} OFF bit and used as external input, then used connect V_{LCD} terminal to V_{DD} . At this time, LCD display contrast changes by supply voltage change, it's necessary to stabilize of supply voltage.

Further it can use the external supply which is efficient in changing the liquid crystal drive voltage by means of V_{LCD} OFF bit.

These data are outputted after they were divided by the segment data select port (ϕ L2D). The segment output $S_{19}\sim S_{30}$ terminal also uses both as the key return timing signal to load key matrix data. The segment output becomes the GND level by the timing as loaded a key data.

2. LCD driver circuit configuration





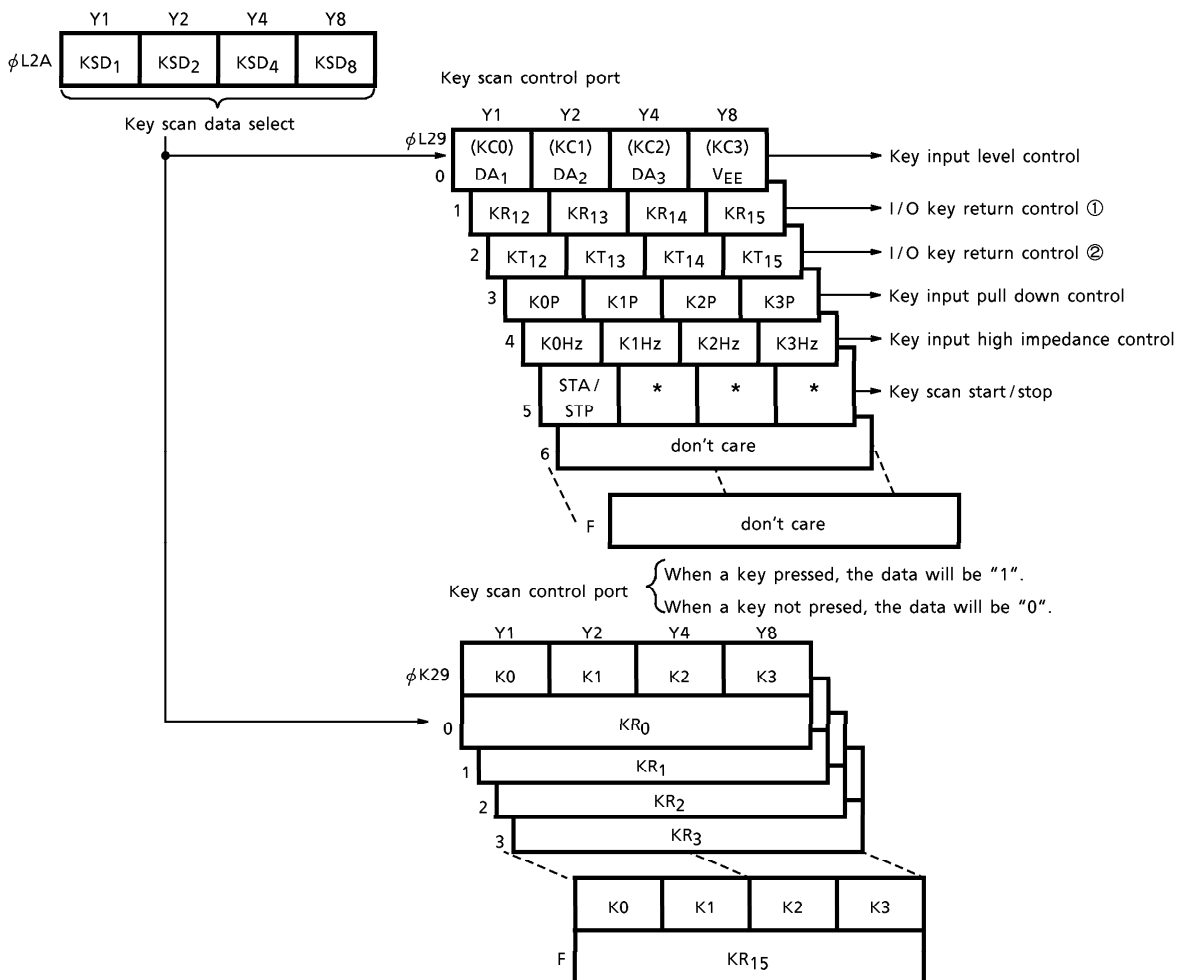
The LCD driver wave voltage potential outputs V_{LCD} and GND voltage potentials and half the intermediate level of these voltage potentials. A key return signal is outputted from S19~S30 when this switching is performed. When loading key data, it becomes "L" level during 80µs.

(Note) When CKSTP instruction or initialization is executed, the common and segment terminal will be "L" level.

○ Key input & key return timing

Since there are four kinds of the key loading method, please design according to the system.

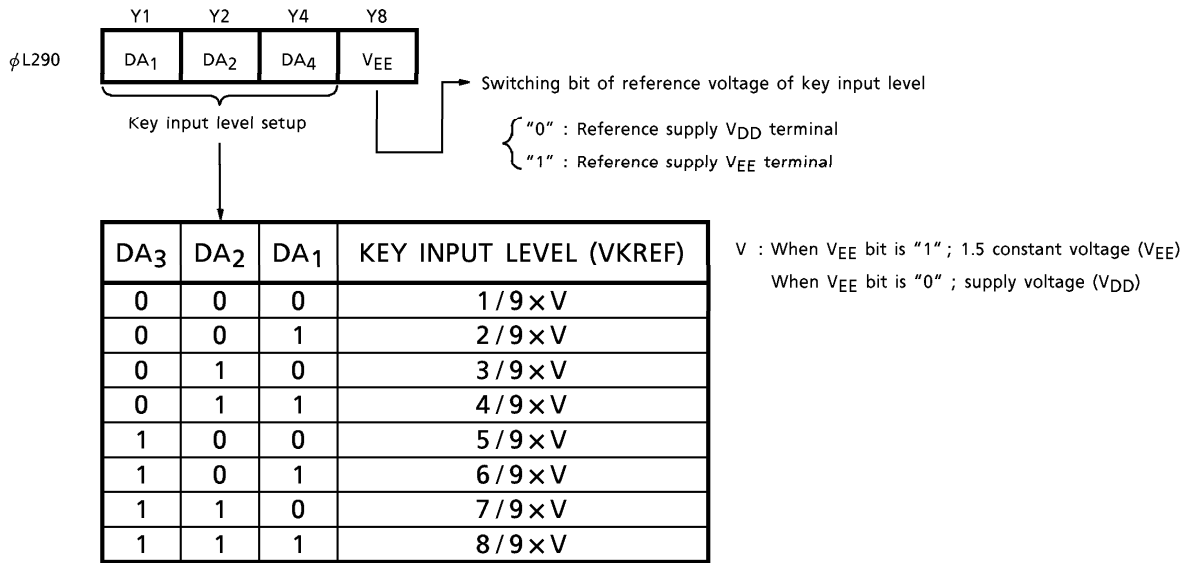
1. Key control port and key scan data port



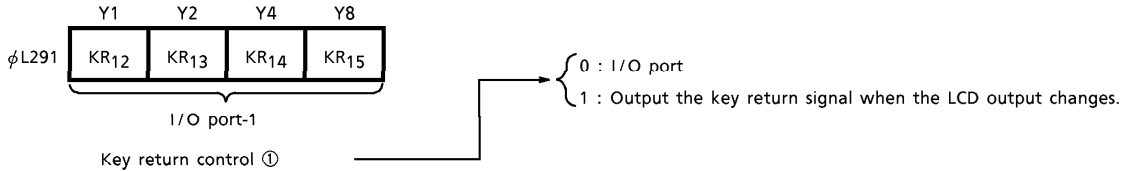
The key scan control port is a port to execute the input level setting control key scan start/stop, setting of I/O port output form (P1-0~P1-3) and key input form.

The key scanned key data are inputted to the key scan data port ($\phi K29$), and loaded into data memory by accessing to this port.

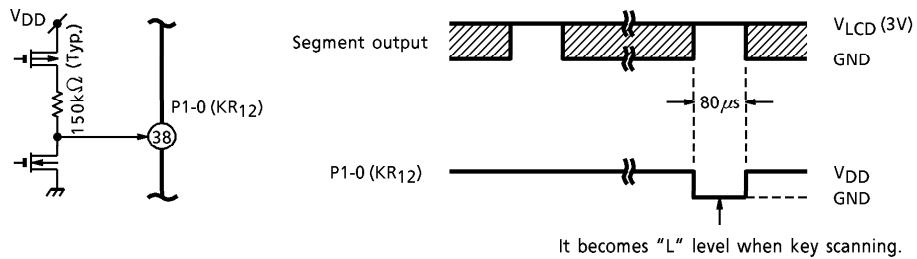
These ports are divided by the key scan data select port ($\phi L2A$), and by setting data to this port data corresponding to this data are accessed. When accessing to the key scan control port ($\phi L29$) or key scan data port, the key scan data select port ($\phi L2A$) is +1 incremented.



It is a port to perform the key input level setting. The reference level of key input supply can be switched to V_{EE} terminal or supply voltage (V_{DD} terminal) by means of V_{EE} bit. By comparing the level that divides the reference supply by means of DA bit to the key input terminal level as shown in the above table, the result will be outputted to the key scan data port and key input data port.

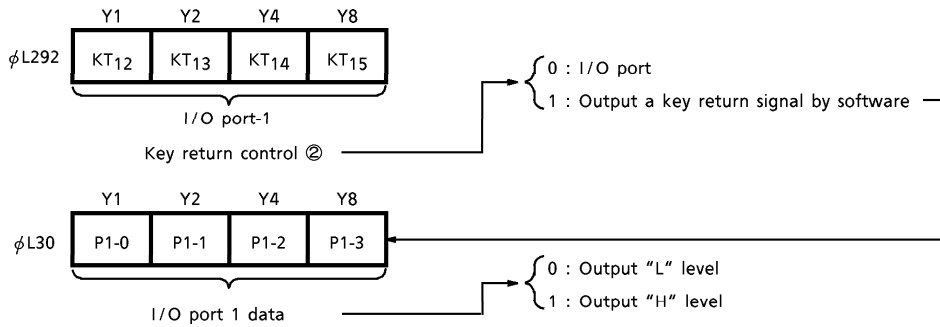


If setting "1" to this port, it becomes the output form as described below.

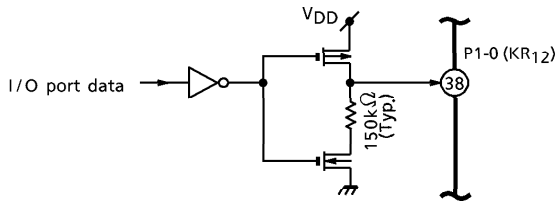


[Output circuit and timing when setting KR₁₂ bit to "1"]

The KR₁₂~KR₁₅ bits correspond to P1-0~P1-3 terminal, respectively. If setting "0" to this bit, it becomes an I/O port.



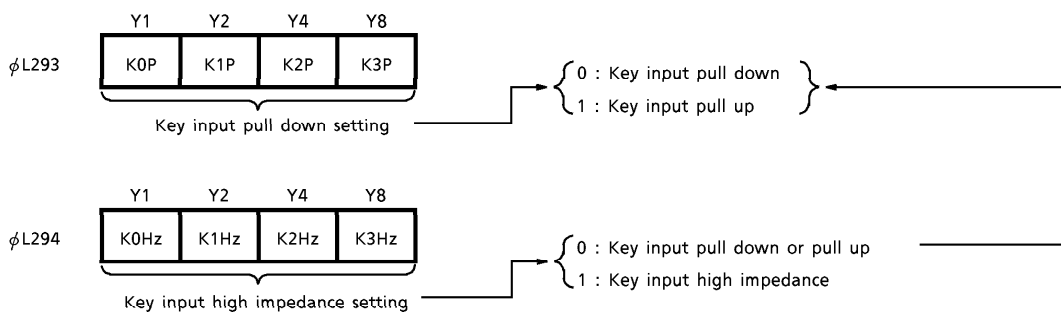
If setting "1" to the port of I/O port-1 key return control ②, it becomes the output form as described below. The "H" and "L" level settings of this output are controlled by the I/O port-1 data.



[Output circuit when setting KT₁₂ bit to "1"]

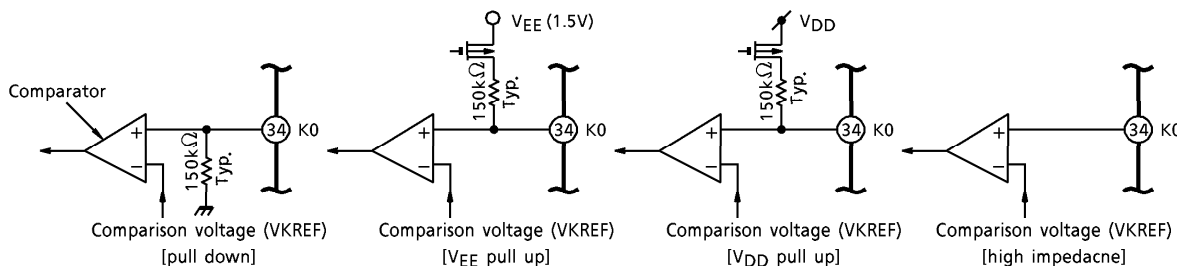
Each KT₁₂~KT₁₅ bit corresponds to P1-0~P1-3, respectively. If setting "0" to this bit, it becomes an I/O port.

When operating a key scan by means of the I/O port-1 key scan control port ① & ②, the contents of I/O-1 control port is necessary to set the bit corresponding to the port to make key scan operate (the output port state [ϕ L3F0]) to "1". In case of setting "1" to each of KR and KT bit, the KT bit is given priority.



These ports perform the input form setting of key input. The input form is set under the condition as below.

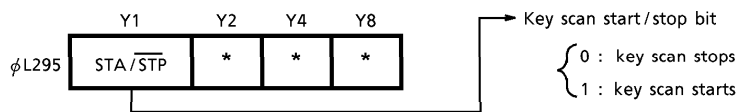
K0Hz	K0P	INPUT FORM
0	0	Pull down
0	1	V _{EE} pull up
1	0	V _{DD} pull up
1	1	High impedance



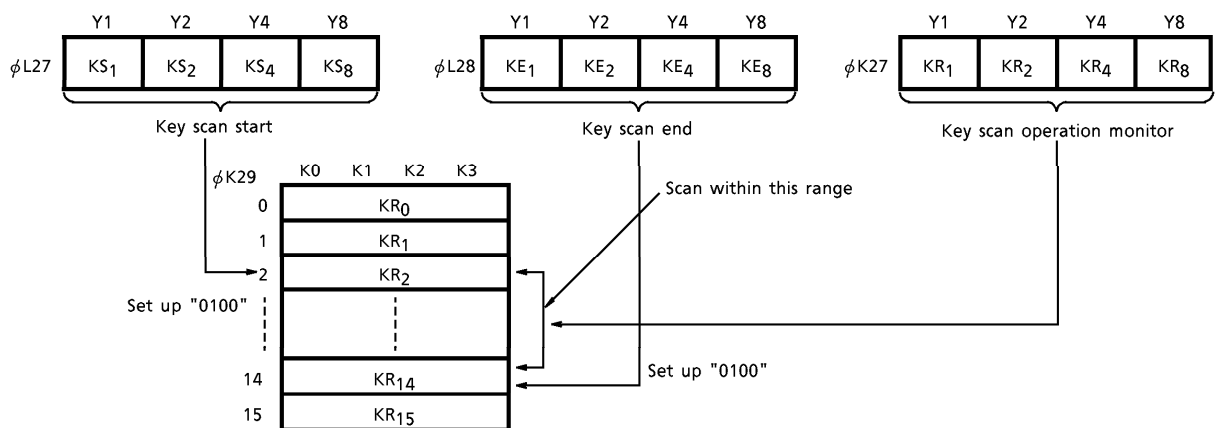
It will always be pull-down at pull down setting. At pull up setting, it will be pull-up only when LCD segment changes, otherwise it becomes high impedance.

At pull-down or pull-up setting, the key input terminal configures a key matrix in combination with the key return output signal. At high impedance setting, it can be used as a 3bit A/D converter of the sequential comparison method by software.

Each of K0P~K3P bits and K0Hz~K3Hz bits correspond to K0~K3 terminal. The key input terminal at pull-down setting, if "H" level ($V_{DD} \times 0.6V$ or more) is applied when WAIT mode, it cancels to execute WAIT instruction and it's possible to restart CPU operation. The CPU operation restarts only at "H" level setting and not at pull-up or high impedance setting.



Whenever setting "1" to STA/STP bit, it starts scanning from the key scan start port data. If setting "0" to this bit, it stops key scanning. When changing the key return control port or the contents of key scan start/end port described the following, to change after the key scan stopped and restart by setting "1" to STA/STP bit afterwards. If not set like this, a key except the ones between scan start data and scan end data may be loaded or key data within a cycle of scan may not be loaded.

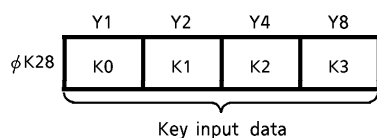


The key scan start and end ports are ports to set up the range in which a key scan is performed and they perform scanning within the range between start data and end data. Set the data of these ports to be "start data value ≤ end data value".

Which key line is loaded during scan operation can be judged by referring to the key scan operation monitor.

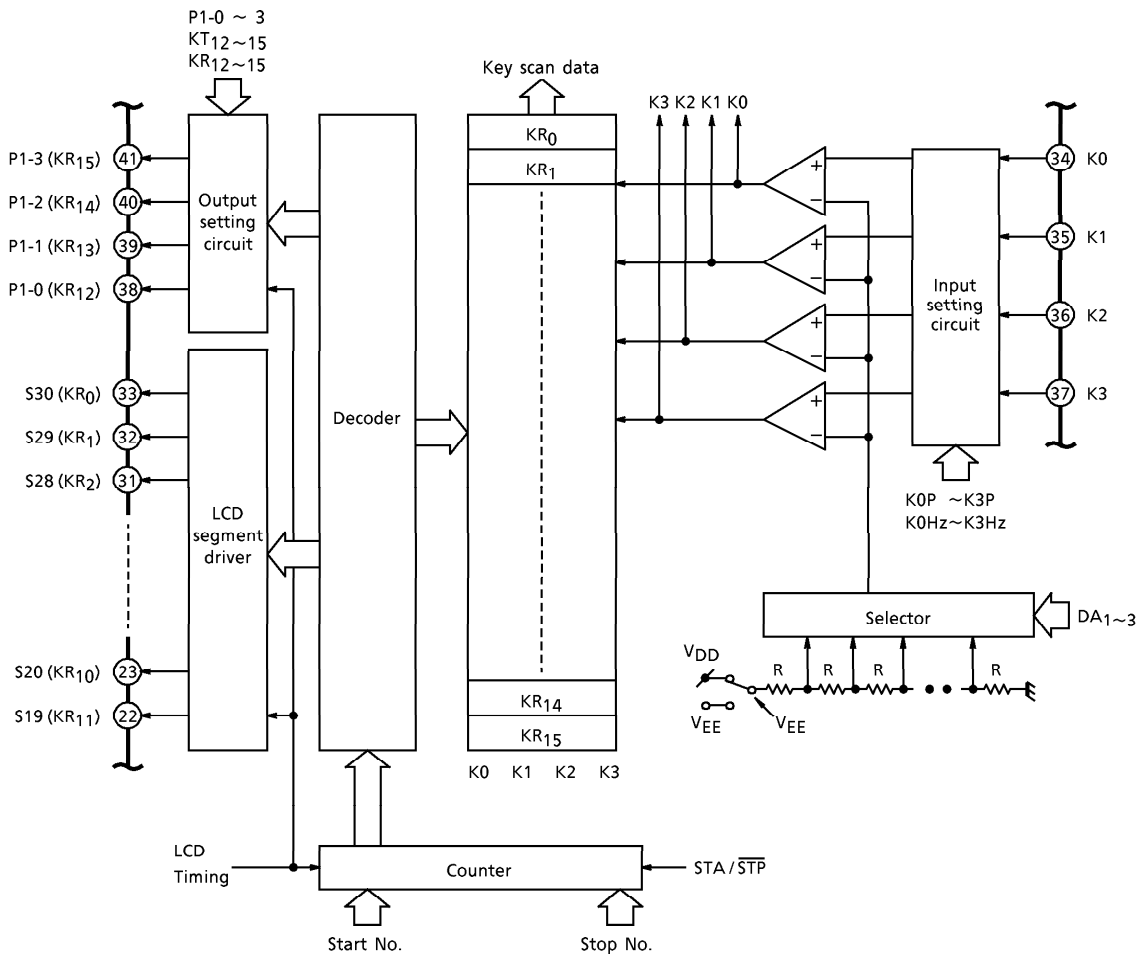
The key scan data ($\phi K29$) outputs "1" when a key pressed, and "0" when not.

(Note) When supply voltage is less than 1.5V by CPU stop function, the CPU stopped. And just after restarted, the key scan data is unknown. Due to this load key scan data into data memory after judging that key scan scanned one cycle by referring to STOP F/F.



From the key input data port, the key input data is loaded into data memory directly. If this is higher than comparison voltage, it becomes "1" and "0" if lower. These ports are accessed when OUT2/IN2 instructions designated [CN=7H~AH] in the operand is executed.

2. Key scan circuit configuration

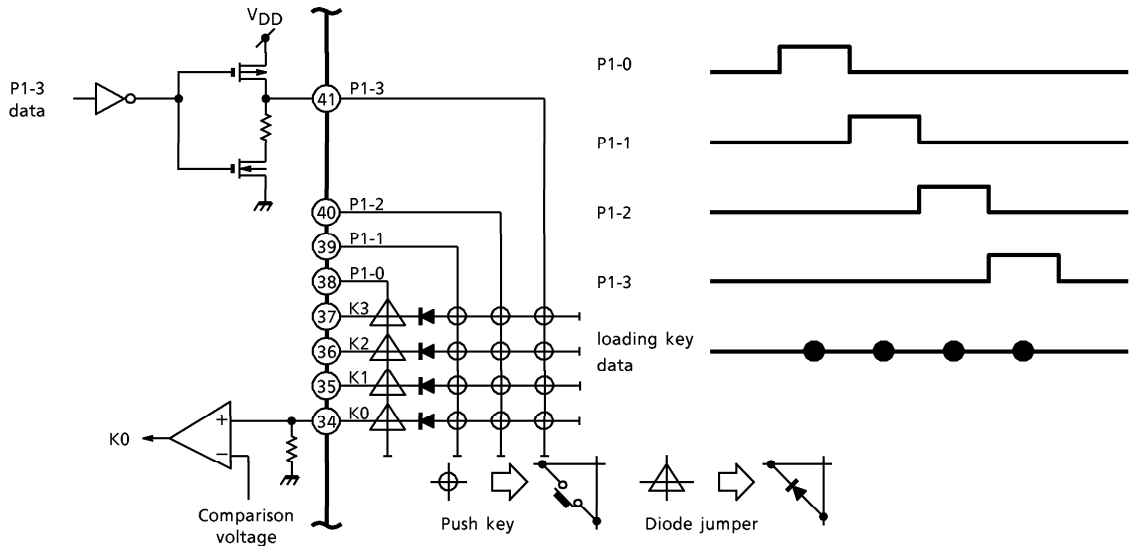


The key input of key scan circuit consists of input setting circuit, 3bit D/A converter, comparator and latch circuit for loading key data. The key return timing output consists of output setting circuit of I/O port, LCD segment driver and counter/decoder to control I/O port output unit.

3. Key matrix configuration

The key matrix can be configured in the following four ways.

(1) Key data loading by software



When loading key data by program, it configures the key matrix as above. The I/O port-1 data (ϕ K30) which you want to load the key line is "H" level, is pressed load. The key input port (ϕ L28) data into the data memory and judge whether the key or not. At this time, the I/O port -1 data not to be loaded should be set to "L" level. If a key is pressed, the key input port data "1" is loaded into data memory and "0" if not pressed. Only $4 \times 4 = 16$ key matrices are usable in this method. However, since data is loaded at high speed and the structure of high resistance is in N channel FET part of P1-0~P1-3, it is unnecessary to have a diode for preventing reverse current owing to double key press. As to the method for loading data by software, set the data to the port as described below.

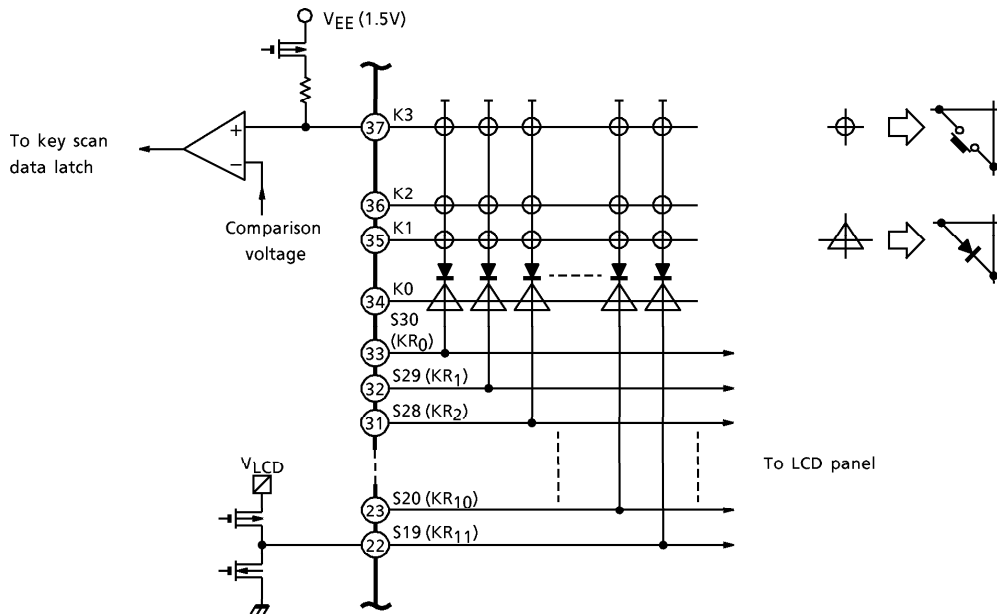
	DA1~DA3	V _{EE}	KR12~KR15	KT12~KT15	K0P~K3P	K0Hz~K3Hz
With jumper	4/9 V _{DD}	0	All "0"	All "1"	All "0"	All "0"
Without jumper	3/9 V _{DD}	0	All "0"	All "1"	All "0"	All "0"

(Note) In case of using as I/O output of I/O port -1, set the bit corresponding to KT12~KT15 to "0".

(Note) When configuring a diode jumper, voltage of diode V_F (-0.6V) lower than supply voltage is applied to the key input voltage. For this reason, the key input threshold value should be set low. As shown the above diagram, a diode for preventing reverse current owing to double key press is necessary. When configuring without a diode jumper, this diode is unnecessary.

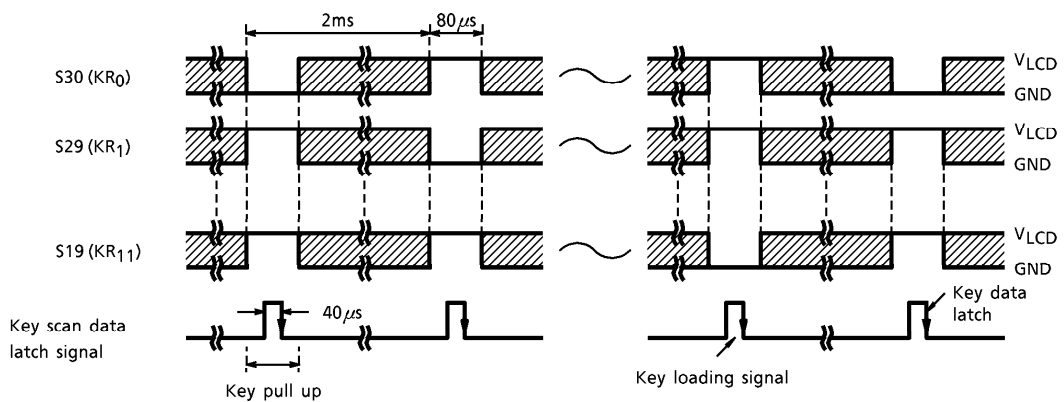
In such mode, adding "H" level (V_{DD} × 0.6V or above) at WAIT mode, WAIT instruction execution is canceled and CPU operation is restarted. (The "H" level at this time is not related to DA₁~DA₃ bits.)

(2) Key data loading by LCD segment output



(Note) Maximum $4 \times 12 = 48$ key matrices can be configured.

(Note) A push key and diode jumper cannot be mixed in the same key line. The position of diode jumper should be on the side of key return signal output.



In case of key data loading by means of LCD segment output, the key matrix as described in the preceding diagram is configured. A diode for preventing reverse current is necessary for this key matrix, therefore be careful for this diode and the diode jumper direction. In this case, V_{LCD} (3V) and GND voltage potentials are outputted from segment terminal when LCD output changes. When key data loading, the segment signal to load will be GND voltage potential at LCD output change and the key input terminal is pulled up to V_{EE} voltage potential. At this time, if a key is not pressed (or without diode jumper), V_{EE} level is inputted to the key input terminal and voltage worth of one diode voltage ($-0.6V$) is inputted from GND voltage potential if a key is pressed (or with diode jumper). The voltage potential inputted is compared with the D/A output level of which V_{EE} voltage potential is divided into nine and latches the signal compared to the key scan data port corresponding to the segment output line of key loading. This key data becomes "1" when a key is pressed and "0" when not. As to the method for key loading by means of LCD segment output, set up the data described below to the port.

DA ₁ ~DA ₃	V_{EE}	KR ₁₂ ~KR ₁₅	KT ₁₂ ~KT ₁₅	KOP~K3P	K0Hz~K3Hz
6/9 V_{EE}	1	All "0"	All "0"	All "1"	All "0"

If setting the range in which key scan is performed to the key scan start (ϕ L27) and key scan end (ϕ L28) and setting "1" to STA/ \overline{STP} bit after the above setting, key scan will load key data one after another within the setting range.

The time required to load one line key data takes 2ms. Due to this the key scan data (ϕ L29) will be loaded into data memory during referring to the key scan operation monitor.

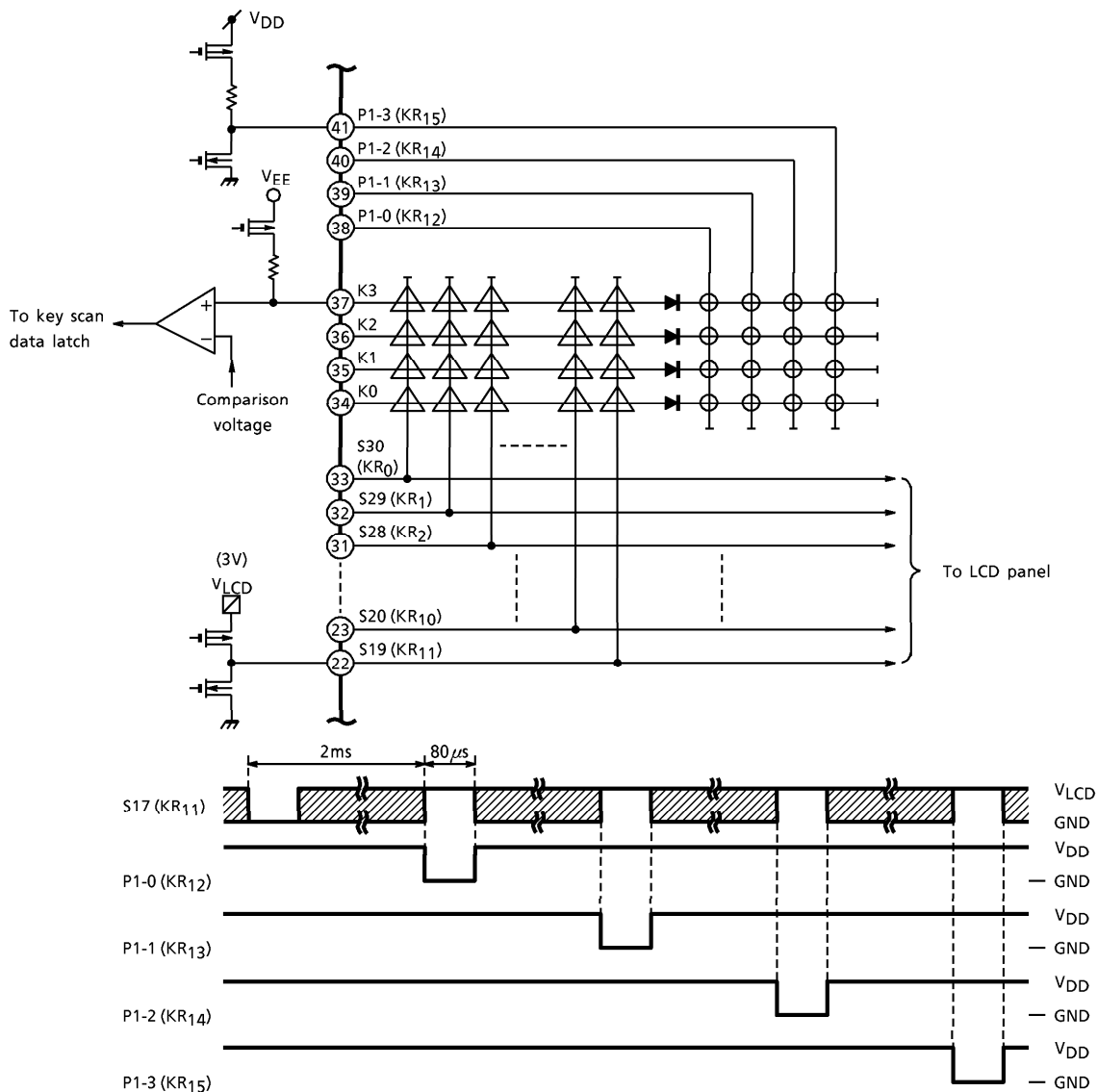
In case of changing the range in which key scan is performed, there are two ways as follows:

- Restart by setting "1" to STA/ \overline{STP} bit again after change.
- After stop the scan operation by setting "0" to STA/ \overline{STP} bit, change the range. Then start key scan again.

(Note) Because the diode jumper data is stored in the latch, the data memory space can be utilized efficiently by referring to the contents of stored latch without loading into data memory, as needed. After CPU operation has stopped by CPU stop function and just after CPU restart, the contents of this latch will be unknown.

(Note) The range in which key scan is performed is between KR₀~KR₁₁.

(3) Key data loading by means of LCD segment output and I/O port ①



The method to load key data by LCD segment output and I/O port is the same as that for loading key data by LCD segment output (3-(2)) except the following setting.

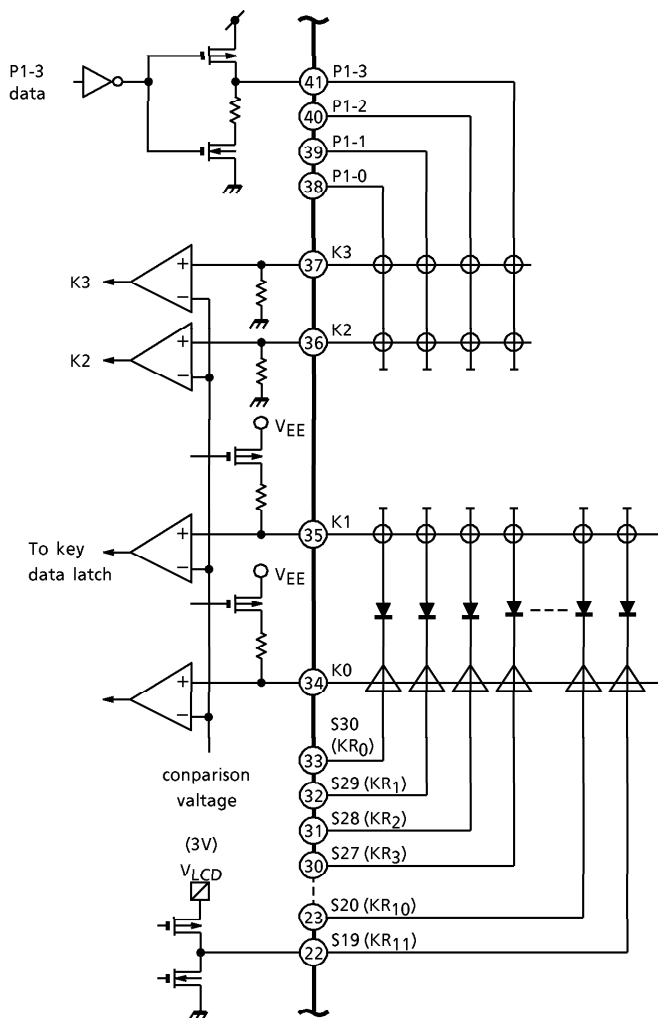
KR ₁₂ ~KR ₁₅	KT ₁₂ ~KT ₁₅
All "1"	All "0"

(Note) In case of using as I/O output of I/O ports (P1-0~P1-3), set the bit corresponding to KR₁₂~KR₁₅ to "0".

(Note) Maximum 4 × 16 = 64 key matrices can be configured.

(Note) The configuration equivalent to the item 3-(2), [key data loading by means of LCD segment output] is possible at KR₀~KR₁₅.

(4) Key data loading by LCD segment output and I/O port ②



It is a usage method combining the key loading method by software and LCD segment output. (Refer to 3-(1), (2).)

The characteristics of this method are below.

- It perform key loading on the I/O port side at high speed.
- It's possible to expand keys by allocating the keys which need not to load at high speed on the LCD segment output side.

As to key loading, the I/O port side performs it at input data port (ϕ K28) and the segment output side at key scan data port (ϕ K29).

Accessing to the key input data port can be done by switching comparison voltage of key input. The setting of this method is performed as described below.

Setting of I/O port side

KR ₁₂	KR ₁₃	KR ₁₄	KR ₁₅	KT ₁₂	KT ₁₃	KT ₁₄	KT ₁₅
0	0	0	0	1	1	1	1

Key input setting

K0P	K1P	K2P	K3P	K0Hz	K1Hz	K2Hz	K3Hz
1	1	0	0	0	0	0	0

The key input settings on the I/O port side and on the LCD segment output side can be done in a unit of 1bit.

(Note) In WAIT mode, supplying "H" level ($V_{DD} \times 0.6V$ or more) to the key input terminal whose key input is set to pull down (K2 and K3 terminal in the above diagram), WAIT instruction execution is cancelled and CPU operation is restarted.

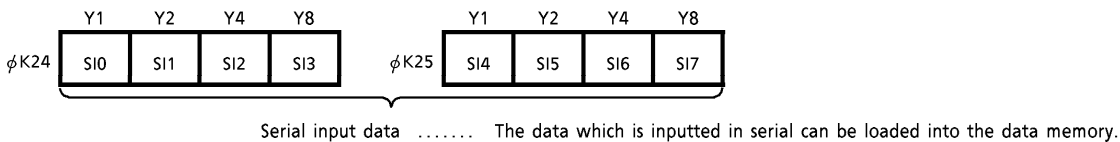
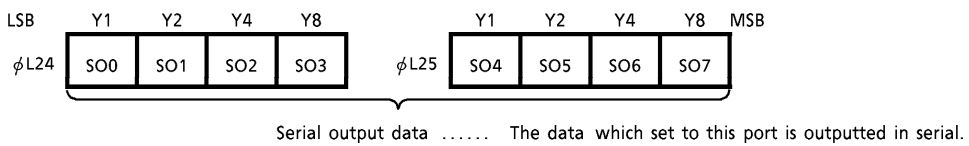
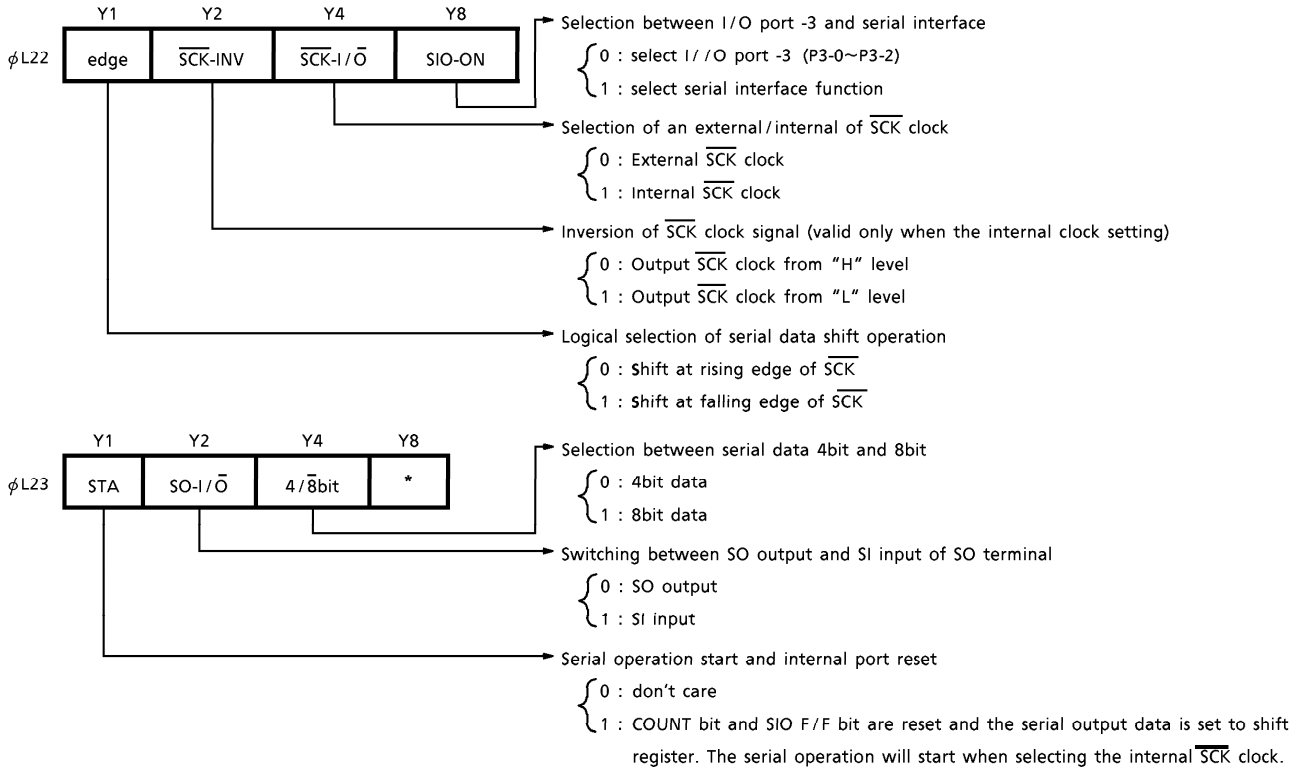
(Note) Key data on the segment side is loaded when LCD segment changes. Therefore, if at the same time loading data on the I/O port, the key input threshold level will be different and data on the segment side will be loaded by mistake. For this reason, control by key scan operation monitor will be required.

(Note) Set the contents of I/O port -1 control port (ϕ L3F0) to all "1" (output setting).

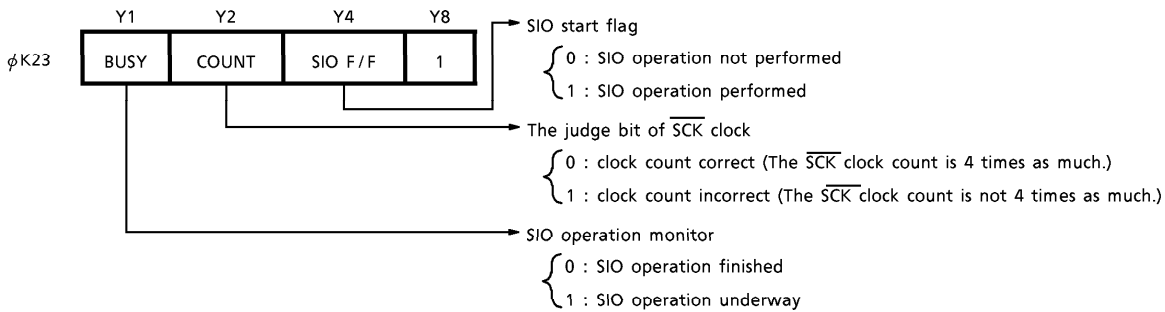
○ Serial interface

The serial interface is a serial I/O port to send/receive synchronously 4 or 8bit data with an internal/external serial clock. By means of SI, SO and \overline{SCK} terminals, it performs sending/receiving data of LSI (for expansion) and microcomputer, etc.

1. Serial interface control port and data port



(Note) As for the serial input data, the contents of shift register is directly accessed.
 (Note) After system reset, the contents of serial interface control port (ϕ L22, ϕ L23) is reset to "0".



The serial interface control and serial data are accessed when OUT2/IN2 instruction designated [CN=2H-5J] in the operand is executed. The serial interface terminal is combined with P3-0, P3-1, P3-2 of I/O port and if setting "1" to SIO ON bit, each I/O port-3 terminal is switched to SI, SO and \overline{SCK} terminal, respectively.

① \overline{SCK} -INW, \overline{SCK} -I/O bit

The \overline{SCK} -INV and \overline{SCK} -I/O bits are bits to set the input and output form of \overline{SCK} terminal. By means of this bit data, the condition as described following will be set.

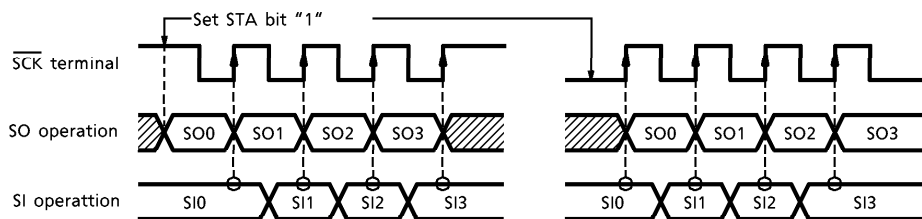
\overline{SCK} terminal state

INV	I/O	INPUT/OUTPUT	\overline{SCK} CLOCK WAVEFORM
0	0	Output	
1	0	Output	
*	1	Input	—

② Edge bit

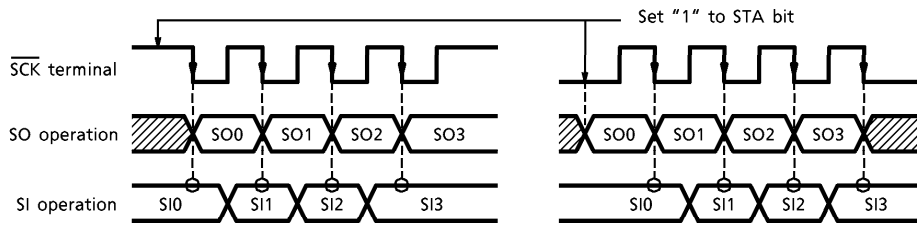
The edge bit sets the shift logic of serial data. By means of this data, data will be shifted as shown below.

- When edge = "0"



When setting the edge bit to "0", the SO output is outputted at rising edge of \overline{SCK} clock, and the SI input, as well as the SO output, is inputted to shift register at rising edge of clock.

- When edge = "1"

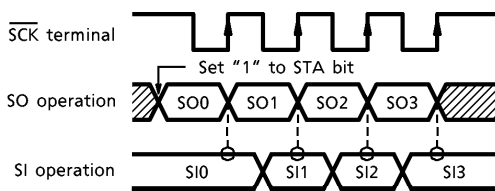


When setting edge bit to "1", SO output is outputted at falling edge of \overline{SCK} clock, and SI input as well as SO output is inputted to shift register at falling edge of clock.

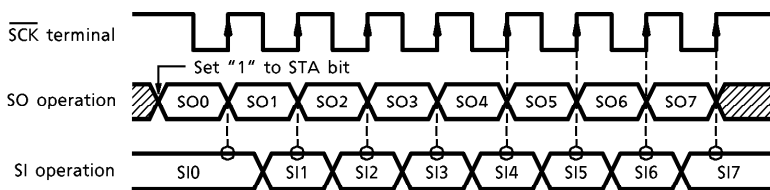
③ $4/\overline{8}$ bit

The $4/\overline{8}$ bit is a bit to select the serial data length. When this bit is "0", it becomes 4bit length and 8bit length when "1". If selecting the 4bit at an internal clock, \overline{SCK} clock outputs 4 clocks and 8 clocks if 8bit.

- When $4/\overline{8}$ bit is "0", (In case of edge = "0", SCK-INV = "0")



- When $4/\overline{8}$ bit is "1", (In case of edge = "0", SCK-INV = "0")

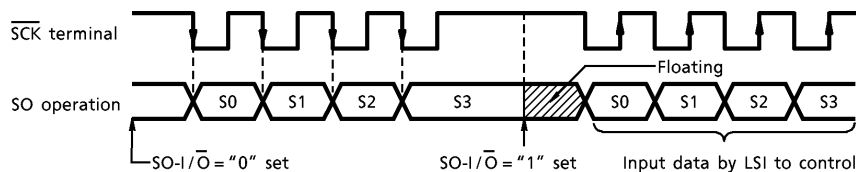


④ SO-I/ \bar{O} bit

The SO-I/ \bar{O} bit is a bit to set the serial input/output of SO terminal.

When setting SO-I/ \bar{O} bit to "0", SO terminal outputs the serial data. When setting this bit to "1", it becomes the serial data input.

By means of controlled this bit, LSI of serial bus system such as T-BUS which conducts data input/output by one terminal can easily be controlled.



(Note) In this case, it is necessary to pull up SO terminal for the floating timing.

In this system, when transmit mode, it performs SIO operation by setting data to the serial output data port. When receiving, it performs SIO operation after SO terminal is set to input and loads the contents of the serial input data port into the data memory. Also when selecting the serial interface, SI terminal is controllable as I/O port (P3-0). The I/O output (P3-0) can be used as strobe pulse terminal in T-BUS, etc.

(Note) When SI terminal is use as serial data input mode, P3-0 bit of I/O control port which corresponding to I/O port-3 should be set to "0".

⑤ Serial interface operation monitor

The operational state of serial interface can be judged by referring to BUSY, COUNT or SIO F/F bit.

Since BUSY bit will be "1" during SIO operation, control data switching and serial data access will be done when BUSY bit is "0".

The COUNT bit is a bit to judge whether data transmitting/receiving was performed in a unit of 4bit. In case shift operation is performed by multiple of 4, this bit outputs "0" and in case shift operation is not performed by multiple of 4, it outputs "1".

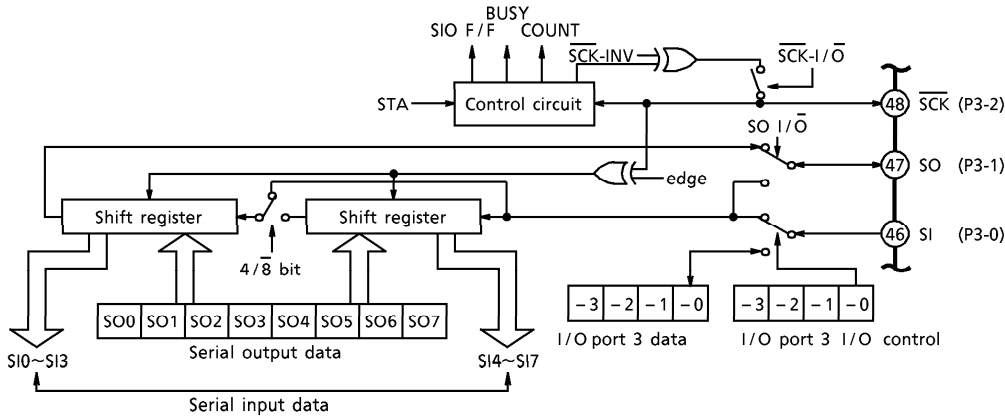
The SIO F/F bit is set to "1" when \overline{SCK} terminal starts clock operation.

The COUNT bit and SIO bit are all reset to "0" if setting "1" to STA bit. These two bits are mainly used when \overline{SCK} terminal is set to an external clock. It can be judged that information that an external clock was inputted and serial data was transferred/received and if operation was properly performed.

⑥ STA bit

Whenever setting "1" to STA bit during \overline{SCK} internal clock setting, serial output data will be set to shift register and clock pulse will be outputted from \overline{SCK} terminal to start shift operation. At the same time COUNT bit and SIO F/F bit will also be reset to "0".

2. Serial interface configuration



The serial interface consists of : control circuit, shift register and I/O port.

(Note) The SI terminal can directly be used as I/O port-3 (P3-0).

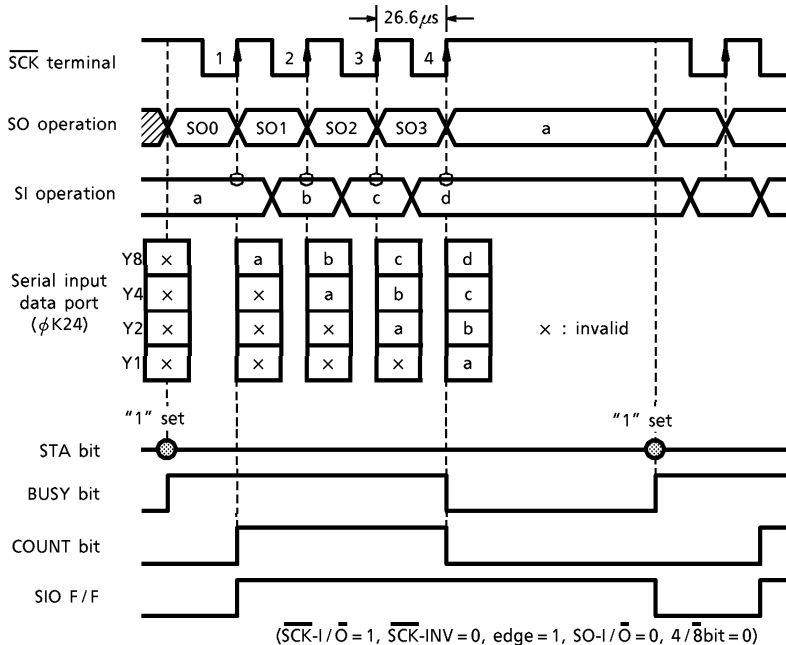
(Note) The contents of data set to serial output data do not accord with the contents of serial input data.

(Note) The SI terminal set as SI input, \overline{SCK} terminal set as \overline{SCK} input and SO terminal set at input will be all Schmitt inputs.

3. Serial interface timing

When setting \overline{SCK} clock to an internal clock, the clock frequency outputted from \overline{SCK} terminal is 37.5kHz (duty 50%).

The example of serial interface timing is as shown below.

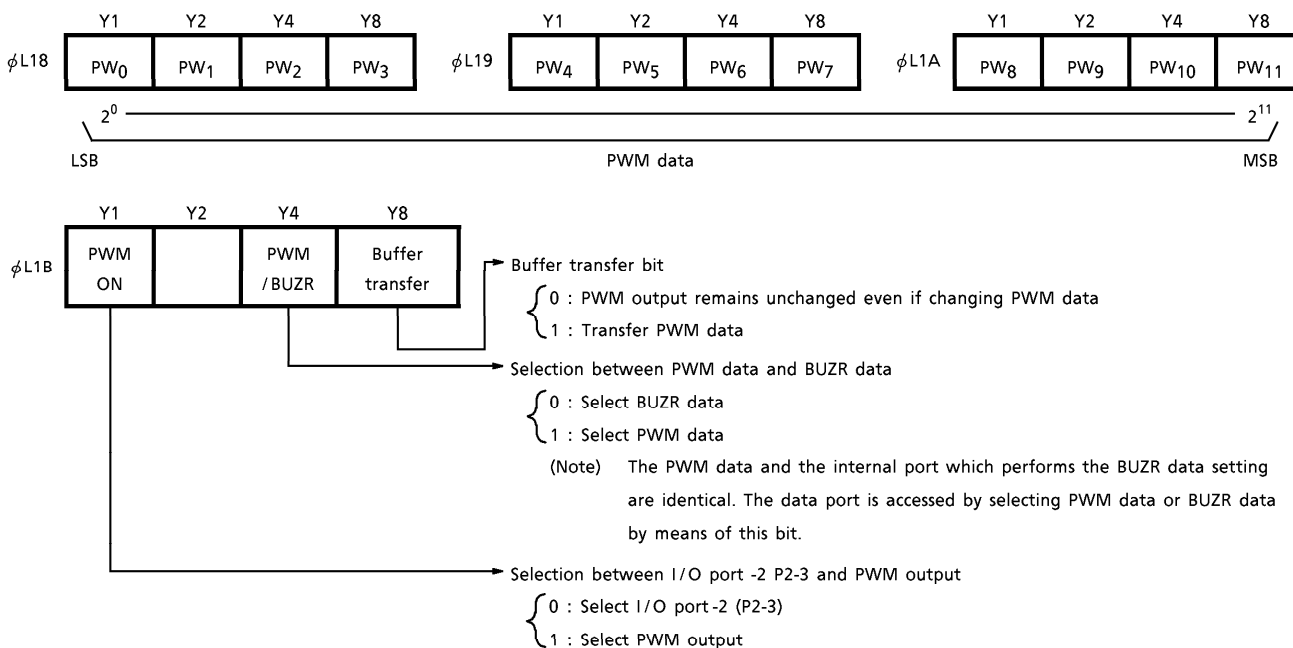


[Example of serial interface timing]

○ D/A converter (pulse-width modulation : PWM) output

The pulse-width modulation output (PWM) can obtain D/A conversion output easily by external low-pass filter. The PWM output is a 12bit resolution and has one-channel output.

1. PWM control port and data port



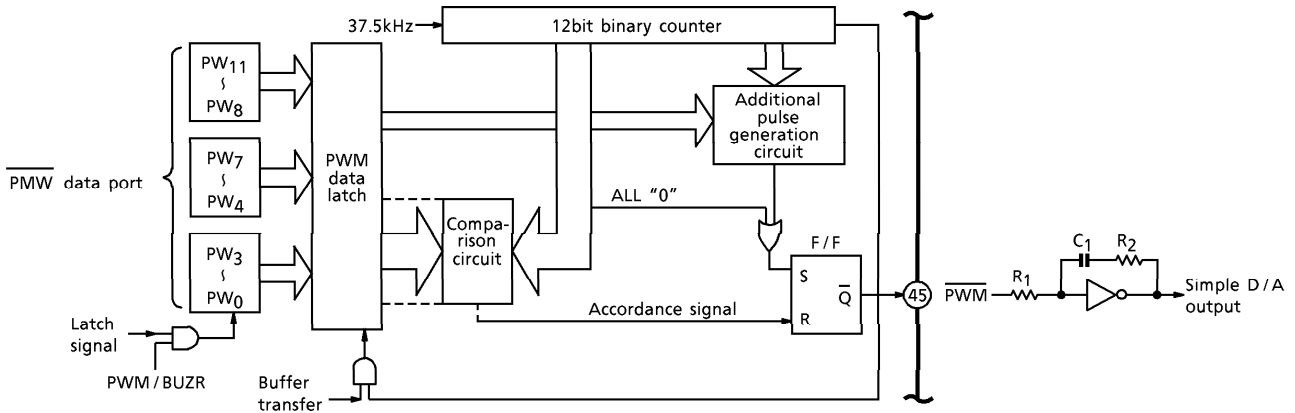
The \overline{PWM} output combines the P2-3 I/O port. When the setting of \overline{PWM} output, the P2-3 switches to \overline{PWM} output by setting \overline{PWM} ON bit to "1".

The PWM data setting is done after setting PWM/BUZR bit to "1" and buffer transfer bit to "0". If setting "1" to buffer transfer bit after PWM data setting, the PWM data will be transferred to PWM data latch. After setting "1" to buffer transfer bit, maximum times of 109ms is required. The \overline{PWM} output would not change if this bit is set to "0" before transferring to PWM data latch.

In PWM data, PW0 is LSB and PW22 is MSB. The high 8bit (PW4-11) data controls the pulse-width of pulse output. The low 4bit (PW0-3) data controls the position to output the pulse that was added during one cycle of \overline{PWM} output.

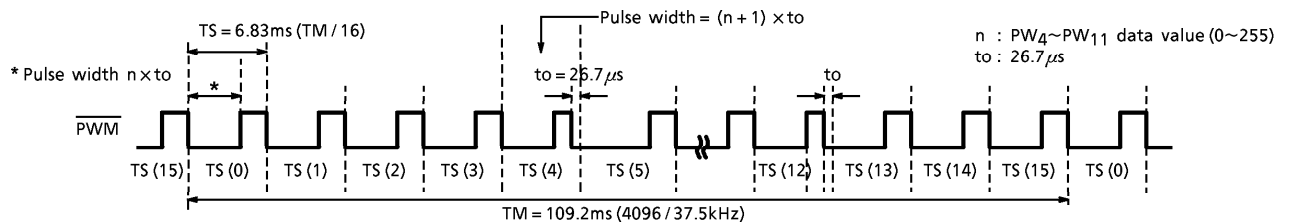
These data settings are performed when OUT1 instruction designated [CN = 8H~BH] in the operand is executed.

2. \overline{PWM} output circuit configuration



The \overline{PWM} output circuit consists of : 12bit binary counter, PWM latch and comparison circuit.

3. \overline{PWM} output waveform



Example of \overline{PWM} output timing (there are additional pulses in TS (4), TS (12): PW₁ bit "1")

PW DATA BIT	THE RANGE IN WHICH AN ADDITIONAL PULSE IS OUTPUTTED (○ MARKS THE POSITION TO BE ADDED).															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PW ₀									○							
PW ₁					○							○				
PW ₂			○				○			○				○		
PW ₃		○		○		○		○		○		○		○		○

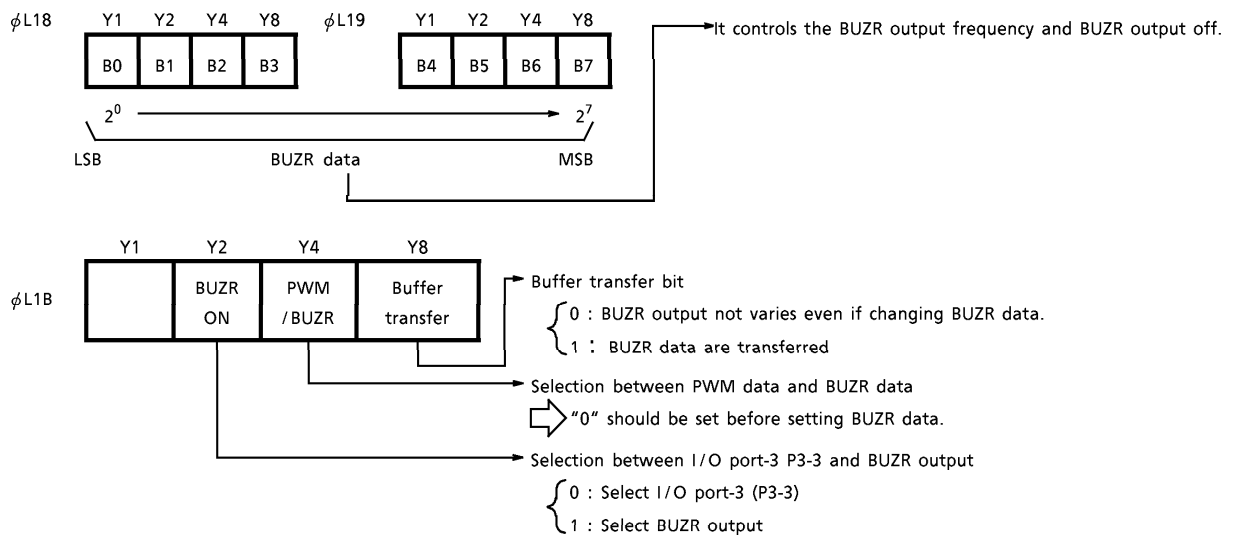
(Note) The above numbers indicate the i value of TS(i). When PW data bit is "1", the additional pulse is outputted to the above ○ position.

One wave cycle of \overline{PWM} output is $TM = 2^{12} / 37.5kHz = 109.2ms$ and it outputs a pulse of 12bit resolution. The high-order 8 bits, PW₄~PW₁₁ of PWM data controls the pulse-width of pulse output whose cycle is TS ($TS = TM / 16 = 6.834ms$). When the value of PW₄~PW₁₁ is n ($n = 0 \sim 255$), the low level pulse width whose cycle is TS will be $n \times to$ ($to = 1 / 37.5kHz$). The low-order 4 bits, PW₀-3 controls the position to output the additional pulse of "to" width in TS (i) ($i = 0 \sim 15$) between 16 sections within TM cycle. In the section where an additional pulse is outputted, the low level pulse-width will be $(n + 1) \times to$. When the low-order bit data are m ($m = 0 \sim 15$), an additional pulse is outputted at m point within TS (i) section. The section where this additional pulse is outputted is shown in the preceding table. (However, the additional pulse is not outputted within TS (0) section.)

○ Buzzer output (BUZR)

The buzzer output is usable for outputting the confirmation and alarm sounds when key operation or tuning scan mode. The buzzer frequency can freely be set and outputs a 50% duty waveform.

1. BUZR control port and data port



The BUZR output combines the P3-3 I/O port. When BUZR output setting, the BUZR on bit is set to "1", then the P3-3 output switches to BUZR output. The BUZR data setting will be done after setting both PWM /BUZR bit and buffer transfer bit to "0". If setting "1" to buffer transfer bit after BUZR data setting, the BUZR data will be transferred to the BUZR data latch and the BUZR frequency will change. The frequency of dividing 75kHz into $2 \times n$ (n : B0~B7 value) is outputted to BUZR output and the B0~B7 setting and frequency ranges are :

$$2 \leq n \leq 255 \quad \frac{75\text{kHz}}{2 \times 2} = 18.75\text{kHz} \leq f_{\text{BUZR}} \leq \frac{75\text{kHz}}{2 \times 255} = 147\text{Hz}$$

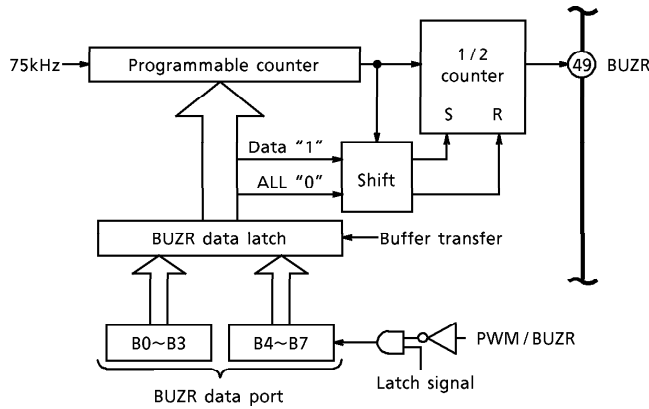
If the B0~7 setting is lower than 1, it will be the condition as described below.

B7	B6	B5	B4	B3	B2	B1	B0	BUZR OUTPUT
0	0	0	0	0	0	0	0	Fixed at "L" level
0	0	0	0	0	0	0	1	Fixed at "H" level

These data settings are performed when OUT1 instruction designated [$C_N = 8H \sim BH$] in the operand is executed.

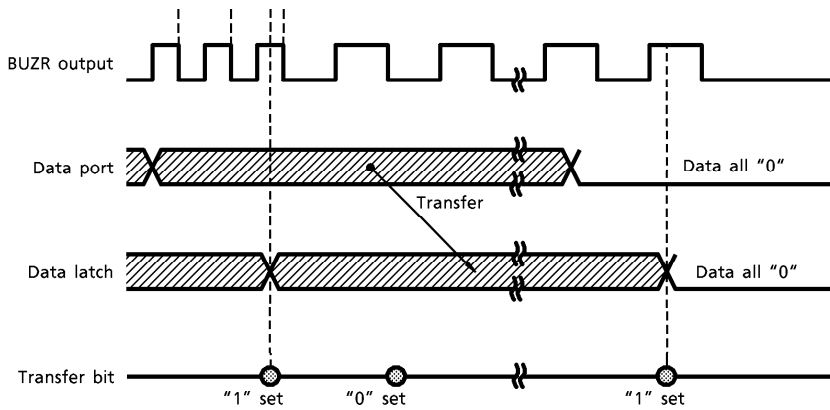
(Note) The BUZR ON bit will be reset to "0" after system reset.

2. BUZR circuit configuration



The BUZR circuit consists of : 8bit programmable counter, 1/2 counter, BUZR latch and BUZR port.

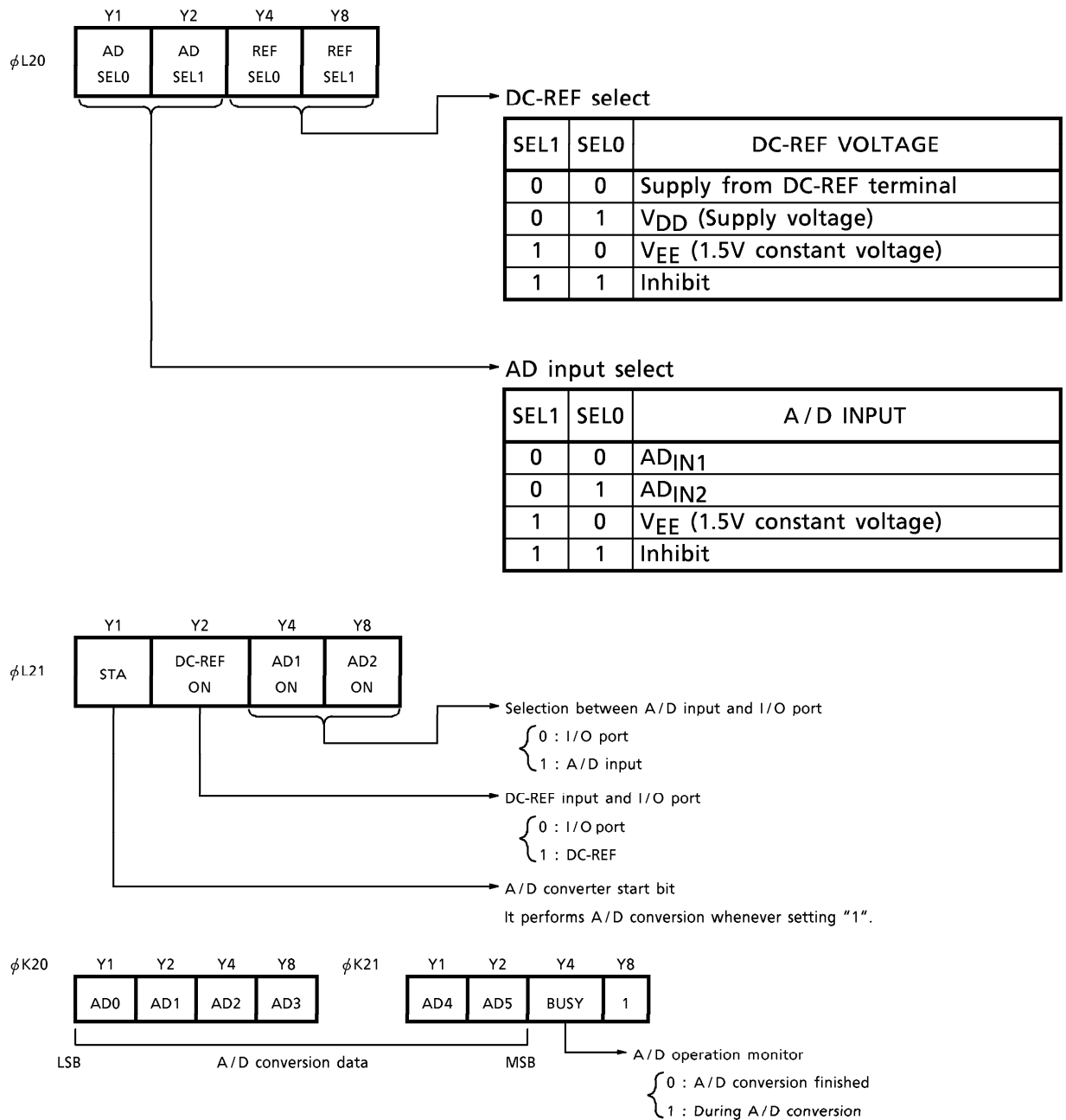
3. BUZR output timing



○ A/D converter

The A/D converter is a 2-channel, 6bit resolution and usable for measuring field strength and battery voltage.

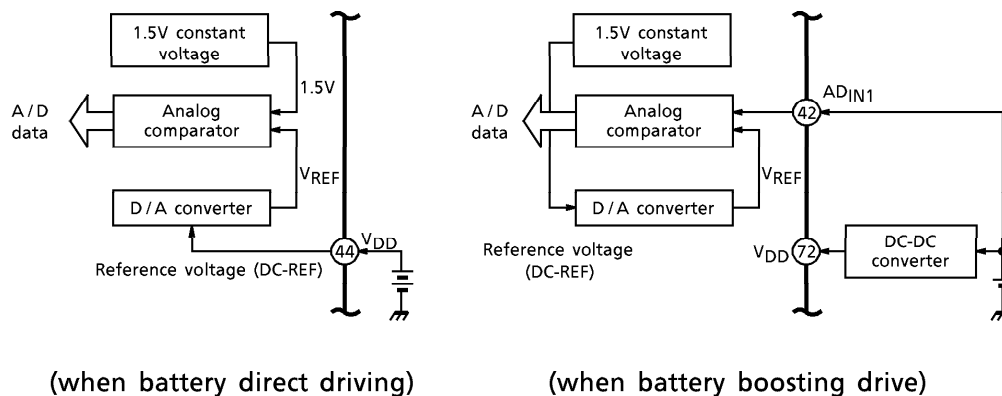
1. A/D converter control port and data port



The A/D converter is a 6bit resolution. The reference voltage of A/D conversion can select the external voltage (DC-REF terminal), supply voltage and 1.5V constant voltage (V_{EE}). The A/D conversion input is a multiplex method of 2-channel external input terminal (AD_{IN1} , AD_{IN2} terminal) and also switchable to 1.5V constant voltage (V_{EE}) as well.

Normally field strength and volume level are measured by selecting external voltage or supply voltage as reference voltage and A/D converting the external input level.

The A/D converter can also measure battery and supply voltages. It outputs a battery signal or performs control for backup mode when battery voltage or supply voltage drop. Following is the description as to this method.



(when battery direct driving)

(when battery boosting drive)

The V_{DD} supply voltage application system has two methods:

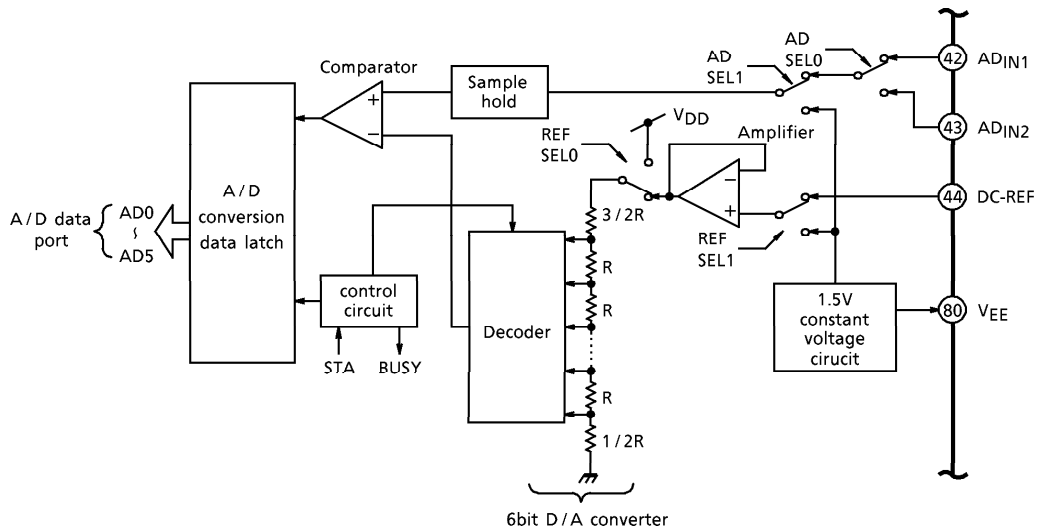
- Method to drive directly from battery.
- Method to drive LSI by boosting low voltage battery using DC-DC converter.

In the case of direct-driving from battery, by setting the reference voltage of A/D converter to supply voltage (V_{DD}) and A/D converting the internal 1.5V constant voltage, battery voltage is judged. If, for example, A/D converting when $V_{DD} = 3V$, the A/D bit data will be about 20H (32) and about 30H (48) when $V_{DD} = 2V$.

In case of boosting battery of low voltage, the battery voltage level can be judged by inputting battery voltage (battery voltage at this time must be $\leq 1.5V$) to A/DIN terminal and setting the internal 1.5V constant voltage (V_{EE}) to reference voltage for A/D conversion. For example, the A/D data when battery voltage = 1.5V will be about 3FH (63) and about 2BH (43) when 1.0V. The A/D converter does A/D conversion whenever setting "1" to STA bit and the conversion will complete after 7 machine cycles ($280\mu s$). Whether A/D conversion is completed can be judged by referring to BUSY bit. After A/D conversion is completed, the data will be loaded into data memory.

These controls are accessed when OUT2/IN2 instruction designated [CN=0H, 1H] in the operand is executed.

2. A/D converter circuit configuration



The A/D converter consists of : 6bit D/A converter, comparator, A/D conversion latch, control circuit, A/D data port and 1.5V constant voltage circuit (supply for LCD driver).

The A/D converter will latch the data to A/D conversion data latch sequentially by means of the 6bit sequential comparison method.

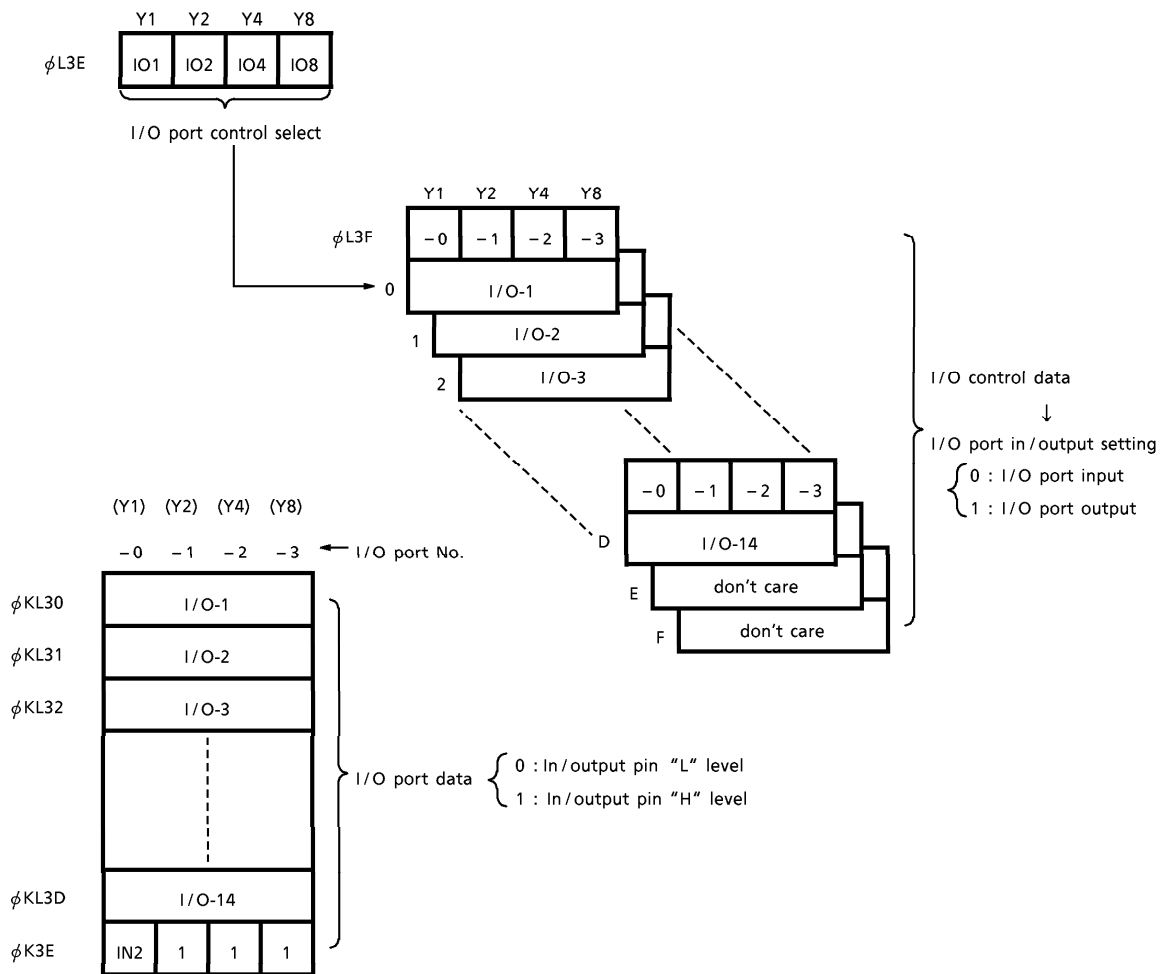
- (Note) The DC-REF terminal is built-in an amplifier and is high impedance input.
- (Note) During A/D conversion, a proper data is not obtainable even if referring to the A/D conversion data. Therefore, make sure to confirm that the conversion has finished by referring to the A/D operation monitor.

○ Input/output port (I/O port)

The I/O port consists of 56 ports (I/O port-1~I/O port-14), which are usable as control signal input /output. Within the 56 I/O ports, the I/O port-1, I/O port-2, I/O port-3 and I/O port-7~I/O port-14 combines a key return signal, A/D converter and PWM output, serial interface and buzzer output and LCD driver output, respectively.

The I/O port-7~I/O port-14 are normally used as LCD driver output.

1. I/O port control and I/O port data



(Note) After system reset, the contents of I/O-1~I/O-6 of the I/O control data will be set to "0" (input port).

(Note) The I/O-1, I/O-2...I/O-14 correspond to the terminal names of P1-0~3, P-20~3... P14-0~3, respectively.

(Note) The S30 terminal will be the input port (IN2) when I/O port switching.

The I/O port in/output will be set by the contents of I/O control data port. If setting to an input port, the bit of I/O control data port corresponding to the port should be set to "0" and "1" if output port.

The I/O control data port is divided by the I/O control select port (ϕ L3E). The I/O control data port should be accessed by setting data corresponding to the port you wish to set to I/O control select port. Normally whenever accessing to I/O control data port, the I/O control select data will be +1 incremented. Therefore, the I/O control data will be set successively after "OH" is set to the I/O control select.

When output port setting, the output state of I/O port is controlled when OUT3 instruction corresponding to each I/O port is executed. The contents of data just outputted will be loaded into data memory when IN3 instruction is executed.

When input port setting, the input state of I/O port is controlled when IN3 instruction corresponding to each I/O port is executed. At this time the contents of latch on the output side will never affect the input data.

The I/O port-7~14 combines the LCD driver output. In case of using even one terminal of LCD driver for I/O port, it is recommended to use after setting "1" to V_{LCD} OFF bit and connecting V_{LCD} terminal to V_{DD} terminal. (Refer to item of LCD driver)

I/O port-1~3 combines A/D converter and BUZR output. After system reset, these ports will be set to I/O port. Furthermore, after system reset, I/O port will be set to input port and combination terminal of LCD driver and I/O port will be set to LCD driver output.

In the I/O port-1, when the input state of I/O port designated at input port is changed, execution of WAIT/CKSTP instruction is cancelled and CPU operation is restarted. Likewise, when I/O bit of MUTE port is "1", MUTE bit of MUTE port will forcibly be set to "1" by changing of the input state.

(Note) In the combined terminal of LCD driver and I/O port, the I/O port input/output and I/O port data will be "don't care" when LCD driver setting.

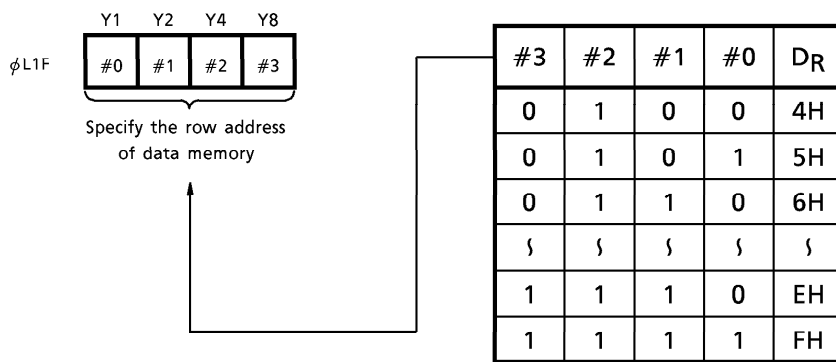
○ Register port

The G-register and data register mentioned in the description of CPU are used also as internal ports.

1. G-register (ϕ L1F)

It is a register for addressing data memory row addresses ($D_R = 4H\sim FH$) when MVGD/MVGS instruction is executed. This register is accessed when OUT1 instruction designated [$C_N = FH$] in the operand is executed.

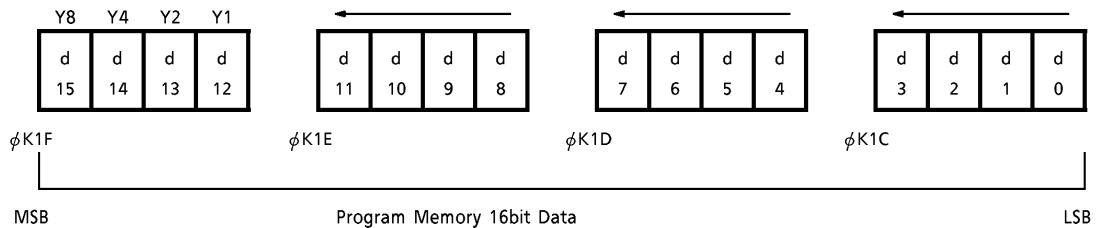
(Note) The contents of this register is valid only when MVGD/MVGS instruction is executed and not valid when other instructions are executed.



(Note) Also all the row addresses of data memory can indirectly be specified by setting data 0H~FH to G-register. ($D_R = 0H\sim FH$)

2. Data register (ϕ K1C~ ϕ K1F)

It is a 16bit register for loading program memory data when DAL instruction is executed. The contents of this register is loaded into data memory in a unit of 4 bits when IN1 instruction designated [$C_N = CH\sim FH$] in the operand is executed. This register can be used for loading LCD segment decoding operation, radio band edge data and coefficient data at "binary to BCD" conversion, etc.

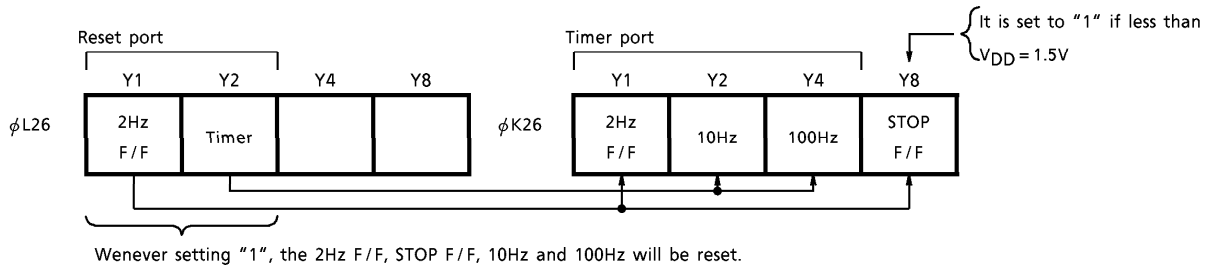


○ Timer & CPU stop function

The timer has 100Hz, 10Hz and 2Hz F/F bits. It is used for counting clock operation and tuning scan mode, etc.

The CPU STOP function is a function to stop CPU by voltage detection circuit when V_{DD} supply voltage drops lower than 1.5V, in order to prevent CPU miss-operation.

1. Timer port and STOP F/F bit

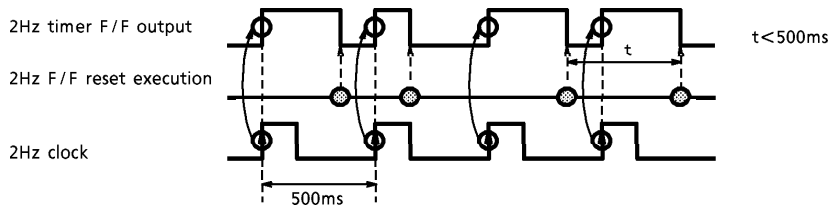


The timer port and STOP F/F bit are accessed when OUT2/IN2 instruction designated [$C_N = 6H$] in the operand is executed.

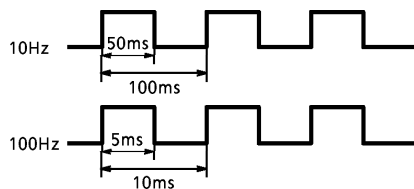
2. Timer port timing

The 2Hz timer F/F is set by 2Hz (500ms) signal. It is reset by setting "1" to 2Hz F/F of reset port. This bit can normally be used for clock counting.

Since the 2Hz timer F/F is reset only by 2Hz F/F of reset port, count error will occur and correct time can not be obtained unless resetting within 500ms cycles.



The 10Hz and 100Hz timers are outputted to 10Hz and 100Hz each by 50% duty pulse of 100ms and 10ms cycle. Whenever setting "1" to the timer bit of reset port, a counter lower than 1kHz will be reset.



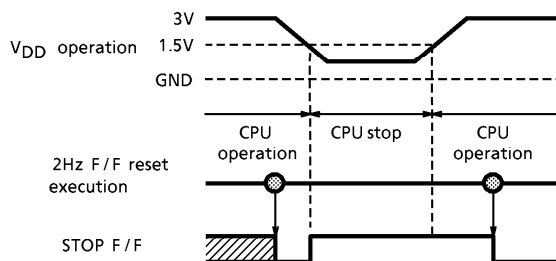
3. CPU stop function and STOP F/F bit

In order to prevent miss-function of CPU operation, the STOP F/F bit is set to "1" when V_{DD} voltage lower than 1.5V is supplied, and the CPU operation stops. The CPU operation stops program counter at a timing of which voltage lower than 1.5V is supplied to V_{DD} terminal, and the execution of instruction stops.

If voltage more than 1.5V is supplied to V_{DD} terminal again, the CPU operation will restart. Since the CPU operation, during this period, is not performed, the clock timing, etc. will be not correct. Whether such condition occurred can be judged by the contents of STOP F/F.

Initialization and clock correction should be done as necessary.

The STOP F/F bit will be reset to "0" whenever setting "1" to the 2Hz F/F of reset port.



(Note) The contents of timer port and STOP F/F will be reset to "0" after system reset or CKSTP instruction is executed.

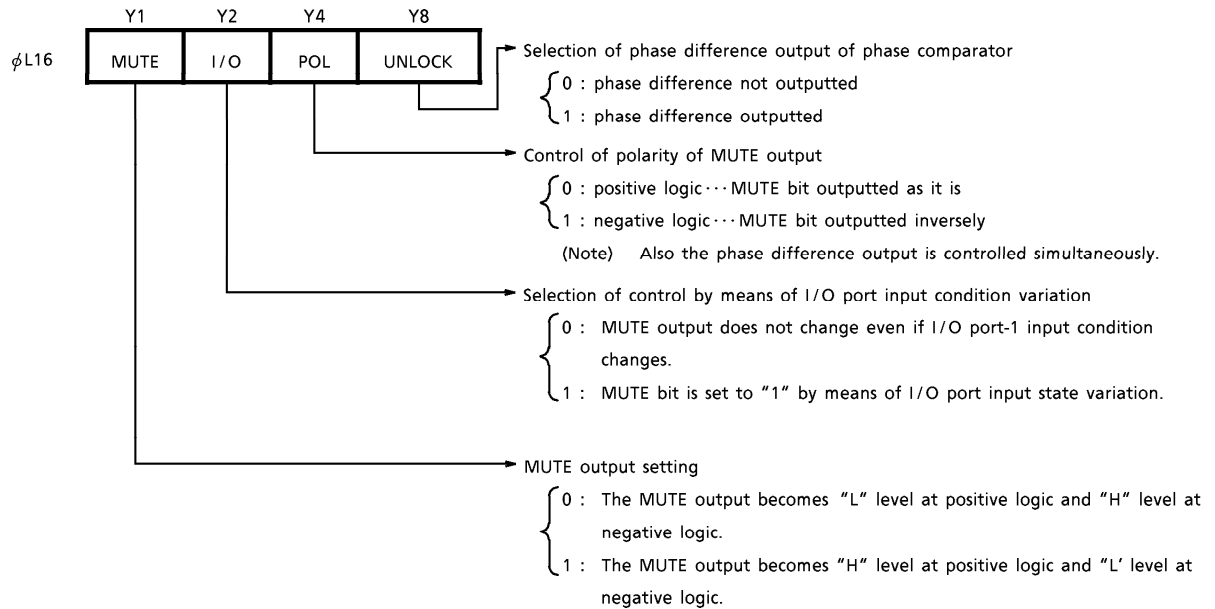
(Note) When clock stop mode setting, the CKSTP instruction will not be executed if V_{DD} voltage is below 1.5V. Execute the CKSTP instruction when V_{DD} voltage is above 1.5V at the timing of radio off, etc.

(Note) The key scan data just after CPU operation is restarted will be unknown.

○ MUTE output

It is a 1bit CMOS type output port exclusive for muting control.

1. MUTE port



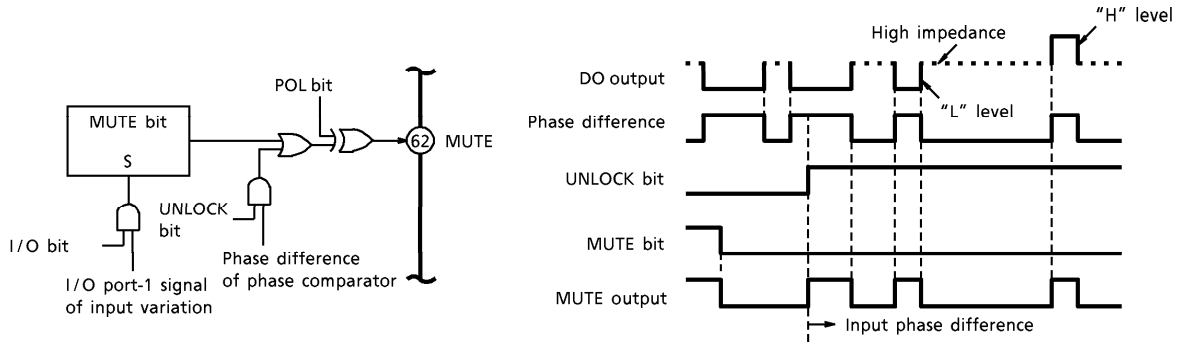
This port is accessed when OUT1 operation designated [C_N = 6H] in the operand is executed. The MUTE output is used for muting control. This has a function to set MUTE bit to "1" at band switching by means of I/O port-1 input, etc.

This function is to prevent noises which occur at the time of linear circuit switching, in case of band switching by I/O port-1 input with a slide switch, etc. This control is done by the contents of I/O bit.

The POL bit sets up the MUTE output logic.

The MUTE output is also capable of performing muting control by means of the phase difference output. The unlock state (when PLL system is not in lock state) is outputted as pulse. In this case, with an external low-pass filter this output is used for MUTE output. This selection can be done by UNLOCK bit.

2. MUTE output configuration and timing



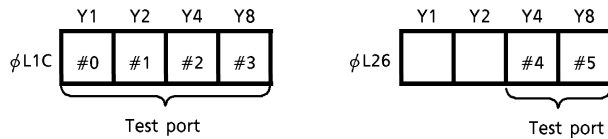
(Note) When POL bit = "0"

(Note) When using the phase difference output of phase comparator, MUTE output should be externally affixed with low-pass filter.

○ Test port

It is an internal port to test the function of a device.

It is accessed when OUT1 instruction designated [CN = CH] in the operand and OUT2 instruction designated [CN = 6H] in the operand are executed. In normal program it should be set to "0".



(Note) These contents will be reset to "0" after system reset.

○ Application for evaluator chip

If "H" level is supplied to TEST terminal (test mode), the device will operate as evaluator chip.

Three kinds of the test modes are prepared. The software development tool is configured by means of three devices.

By connecting this software development tool to a tuner IC, confirming the radio operation while proceeding software development can be done.

As to the development tool specifications, please refer to the specifications of TC9317F software development tool.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~4.0	V
Input Voltage	V _{IN}	-0.3~V _{DD} + 0.3	V
Power Dissipation	P _D	400	mW
Operating Temperature	T _{opr}	-10~60	°C
Storage Temperature	T _{stg}	-55~125	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta = 25°C, V_{DD} = 3.0V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Range of Operating Supply Voltage	V _{DD}	—	※	1.8	3.0	3.6	V
Range of Memory Retention Voltage	V _{HD}	—	Crystal oscillation stopped (CKSTP instruction executed) ※	1.0	~	3.6	
Operating Current	I _{DD1}	—	Under ordinary operation and PLL on operation, no output load	—	0.5	1.5	mA
	I _{DD2}	—	CPU only operating (PLL off, display lit)	—	50	100	
	I _{DD3}	—	In stand-by mode (PLL off, crystal oscillator only)	—	10	20	
Memory Retention Current	I _{HD}	—	Crystal oscillation stopped (CKSTP instruction executed)	—	0.1	1.0	
Crystal Oscillation Frequency	f _{XT}	—	※	—	75	—	kHz
Crystal Oscillation Startup Time	t _{ST}	—	Crystal oscillation f _{XT} = 75kHz	—	—	1.0	s

Voltage doubler circuit

Voltage Doubler Reference Voltage	V _{EE}	—	GND reference (V _{EE})	1.3	1.5	1.7	V
Constant Voltage Temperature Characteristics	D _V	—	GND reference (V _{EE})	—	-5	—	mV/°C
Voltage Doubler Boosting Voltage	V _{LCD}	—	GND reference (V _{LCD})	2.6	3.0	3.4	V

Operating frequency ranges for programmable counter and if counter

F _{MIN}	f _{FM}	—	Sine wave input when V _{IN} = 0.2V _{p-p} ※	0.5	~	2.5	MHz
A _{MIN}	f _{AM}	—	Sine wave input when V _{IN} = 0.2V _{p-p} ※	0.5	~	12	
I _{FIN}	f _{IF}	—	Sine wave input when V _{IN} = 0.2V _{p-p} ※	0.35	~	12	
Input Amplitude	V _{IN}	—	F _{MIN} , A _{MIN} , I _{FIN} input ※	0.2	~	V _{DD} - 0.5	V _{p-p}
F _{MIN} -PSC Transmission Delay Time	t _{pd}	—	PSC ※	—	—	400	ns

For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8~3.6V, Ta = 10~60°C.

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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LCD common output/segment output, general-purpose I/O ports
(COM1/P7-0~COM3/P7-2, S1/P7-3~S30/IN2)

Output Current	High Level	I_{OH1}	—	$V_{LCD} = 3V, V_{OH} = 2.7V$	-300	-600	—	μA
	Low Level	I_{OL1}	—	$V_{LCD} = 3V, V_{OL} = 0.3V$	300	600	—	
Output Voltage 1/2 Level		V_{BS}	—	No load	1.3	1.5	1.7	V
Input Leak Current		I_{LI}	—	$V_{IH} = V_{LCD}, V_{IL} = 0V$ (when I/O port or IN port)	—	—	± 1.0	μA
Input Voltage	High Level	V_{IH2}	—	(when I/O port or IN port)	$V_{LCD} \times 0.6$	~	V_{LCD}	V
	Low Level	V_{IL2}	—	(when I/O port or IN port)	0	~	$V_{LCD} \times 0.1$	

I/O port 1 (P1-0/KR12~P1-3/KR15)

Output Current	High Level	I_{OH2}	—	$V_{OH} = 2.7V$	-300	-600	—	μA
	Low Level	I_{OL2}	—	$V_{OL} = 0.3V$	300	600	—	
Input Leak Current		I_{LI}	—	$V_{IH} = 3.0V, V_{IL} = 0V$ (when I/O port)	—	—	± 1.0	μA
Input Voltage	High Level	V_{IH2}	—	(when I/O port)	2.4	~	3.0	V
	Low Level	V_{IL2}	—	(when I/O port)	0	~	0.6	
N-ch/P-ch Load Resistance		R_{ON}	—	$V_{OL} = 3.0V, V_{OH} = 0V$ (when key return output)	50	100	200	$k\Omega$

HOLD input port

Input Leak Current		I_{LI}	—	$V_{IH} = 3.0V, V_{IL} = 0V$	—	—	± 1.0	μA
Input Voltage	High Level	V_{IH3}	—	—	2.4	~	3.0	V
	Low Level	V_{IL3}	—	—	0	~	1.2	

A/D converter (A/D_{IN1}, A/D_{IN2}, DC-REF)

Analog Input Voltage Range		V_{AD}	—	AD _{IN1} , AD _{IN2}	0	~	V_{DD}	V
Analog Reference Voltage Range		V_{REF}	—	DC-REF, $V_{DD} = 2.0 \sim 3.6V$	1.0	~	$V_{DD} \times 0.9$	V
Resolution		V_{RES}	—	—	—	6	—	bit
Conversion Total Error		—	—	$V_{DD} = 2.0 \sim 3.6V$	—	± 1.0	± 4.0	LSB
Analog Input Leak		I_{LI}	—	$V_{IH} = 3.0V, V_{IL} = 0V$ (AD _{IN1} , AD _{IN2} , DC-REF)	—	—	± 1.0	μA

For conditions marked by an asterisk (*), guaranteed when $V_{DD} = 1.8 \sim 3.6V, T_a = 10 \sim 60^\circ C$.

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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Key input ports (K0~K3)

Key Input Voltage Range	V_{KI}	—	—	0	~	V_{DD}	V	
A/D Conversion Resolution	V_{RES}	—	—	—	3	—	bit	
A/D Conversion Combined Error	—	—	$V_{DD} = 1.8 \sim 2.0V$	—	—	± 1.5	LSB	
			$V_{DD} = 2.0 \sim 3.6V$	—	—	± 0.5		
N-ch / P-ch Input Resistance	R_{IN1}	—	—	50	100	200	k Ω	
Output Current	High Level	V_{IH1}	—	When WAIT instruction released			V	
	Low Level	V_{IL1}	—	When WAIT instruction released				
Input Leak Current	I_{LI}	—	When input resistance OFF, $V_{IH} = 3.0V$, $V_{IL} = 0V$			—	± 1.0	μA

DO1 / OT, DO2 output; MUTE, PSC output

Output current	High Level	I_{OH1}	—	$V_{OH} = 2.7V$			μA	
	Low Level	I_{OL1}	—	$V_{OL} = 0.3V$				
Output Off Leak Current	I_{TL}	—	$V_{TLH} = 3.0V$, $V_{TLL} = 0V$ (DO1, DO2)			—	± 100	nA

General-purpose I/O ports (P2-0~P6-3)

Output Current	High Level	I_{OH1}	—	$V_{OH} = 2.7V$			μA	
	Low Level	I_{OL1}	—	$V_{OL} = 0.3V$				
Input Leak Current	I_{LI}	—	$V_{IH} = 3.0V$, $V_{IL} = 0V$			—	± 1.0	
Input Voltage	High Level	V_{IH2}	—	—	2.4	~	3.0	V
	Low Level	V_{IL2}	—	—	0	~	0.6	

IN1 / SCIN, RESET input port

Input Leak Current	I_{LI}	—	$V_{IH} = 3.0V$, $V_{IL} = 0V$ (excluding SCIN input)			—	—	± 1.0	μA
Input Voltage	High Level	V_{IH2}	—	—	2.4	~	3.0	V	
	Low Level	V_{IL2}	—	—	0	~	0.6		

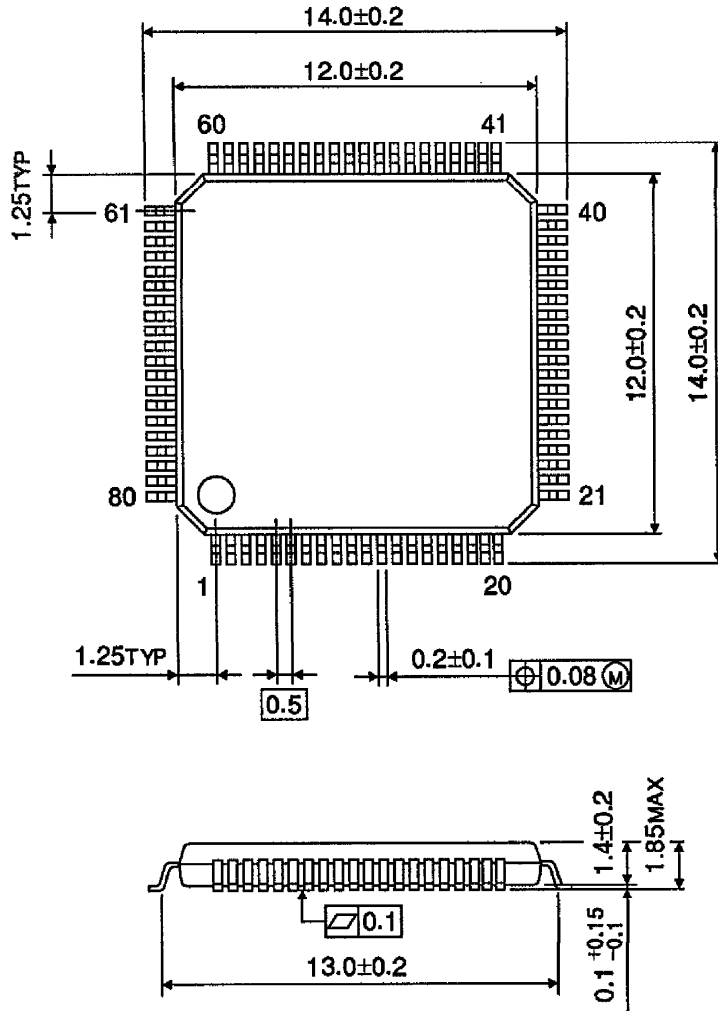
Others

Input Pull-Down Resistance	R_{IN2}	—	(TEST)	15	30	60	k Ω
XIN Amp Feedback Resistance	R_{fXT}	—	(XIN-XOUT)	—	20	—	M Ω
XOUT Output Resistance	R_{OUT}	—	(XOUT)	—	4	—	k Ω
Input Amp Feedback Resistance	R_{fIN1}	—	(FM _{IN} , AM _{IN} , IF _{IN} / SCIN)	500	1000	2000	k Ω
Voltage Used to Detect Supply Voltage Drop	V_{STP}	—	(V_{DD})	1.35	1.5	1.6	V
Supply Voltage Drop Detection Temperature Characteristics	D_S	—	(V_{DD})	—	-3	—	mV/ $^{\circ}C$

For conditions marked by an asterisk (*), guaranteed when $V_{DD} = 1.8 \sim 3.6V$, $T_a = 10 \sim 60^{\circ}C$.

PACKAGE DIMENSIONS
LQFP80-P-1212-0.50A

Unit : mm



Weight : 0.45g (Typ.)

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000707EBA

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