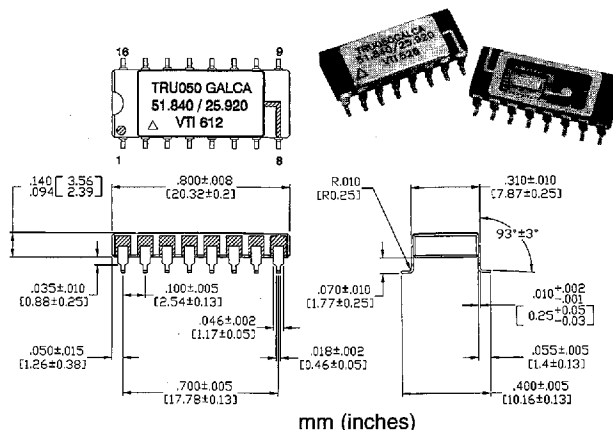


Crystal Based Clock and Data Recovery Products

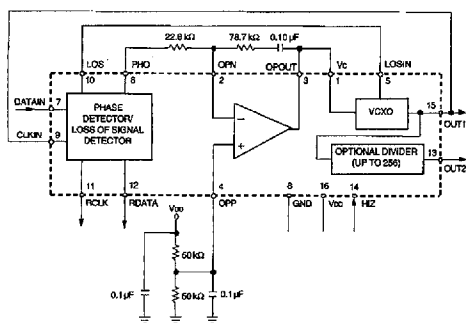
TRU-050 Timing Based Recovery Unit

Features

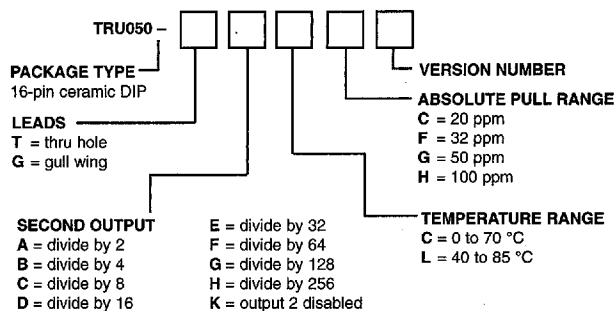
- Frequency translator
- Compact phase-locked loop (PLL) saves board space
- Quartz crystal stabilized by internal VCXO
- User-defined loop filter for tailoring performance
- Input data and clock rates from 8 kb/s to 52 Mb/s
- NRZ data compatible
- Low transition density capability
- Superior jitter performance
- TTL output compatible
- 3-state clock and data output
- Loss of signal indicator



Typical NRZ Data Retiming Application

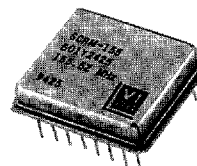
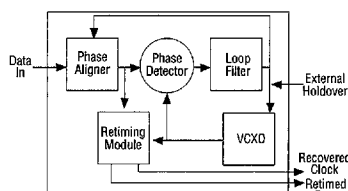


Ordering Information



Sonet Clock Recovery Module SCRM-155 (155.52 MHz)

- Clock Recovery and Data Retiming (with VCXO). Meets CCITT Type A or B interfaces with either type
- Holdover feature offers ± 20 ppm clock accuracy with no data
- Acquires lock quickly (40 bit periods)
- Eliminates pattern (systematic) jitter
- Virtually unlimited cascades



Acquisition Time	Input Density = 50%	40 bit periods (260 nanosec)
Phase Drift due to input data		
	20 non-transitions	<0.002 UI
	60 non-transitions	<0.006 UI
Jitter Tolerance	10 Hz	>40 UI
(Exceeds requirements	300 Hz	>10 UI
of TR-NWT-000253	6.5 kHz	> 2 UI
and CCITT G.958)	65 kHz	> 2 UI
Jitter Transfer	Peaking	0 dBm.
	Bandwidth	15.5 kHz typical
	Residual Jitter	<2° rms for input density of 50%
		<2°rms for 2 ⁷ -1 PRB Sequence
		<2°rms for 2 ²³ -1 PRB Sequence
Free Running Temperature Stability		
0°C to +70°C or -40°C to +85°C		±20 ppm over temperature
Tuning Range	0 to -5V (ECL)	±50 ppm
	0 to +5V (PECL)	±50 ppm
Signal levels		10 KH ECL/PECL compatible, differential input, complementary output
Supply		-5.2 Vdc ±5% at 85 mA (ECL) +5.0 Vdc ±5% at 85 mA (PECL)
How to Order	<u>Temp Range</u>	<u>Output</u>
	0°C to +70°C	ECL
	0°C to +70°C	PECL
	-40°C to +85°C	ECL
	-40°C to +85°C	PECL
		<u>SCRM-155</u>
		601Y2425
		601Y2425-1
		601Y2425-2
		601Y2425-3