



# VNQ500PEP

## QUAD CHANNEL HIGH SIDE DRIVER

### TARGET SPECIFICATION

TYPE	R <sub>DS(on)</sub>	I <sub>OUT</sub>	V <sub>CC</sub>
VNQ500PEP	500 mΩ	0.35 A	36V

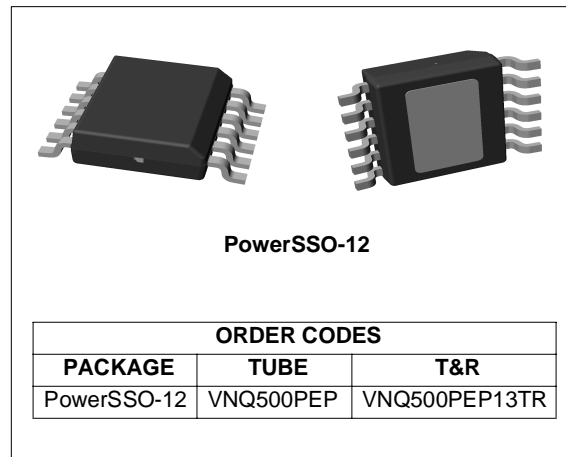
- CMOS COMPATIBLE I/O's
- CHIP ENABLE
- JUNCTION OVERTEMPERATURE PROTECTION
- CURRENT LIMITATION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT

### DESCRIPTION

The VNQ500PEP is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active current limitation combined with latched thermal shutdown, protect the device against overload.

Device automatically turns off in case of ground pin disconnection.



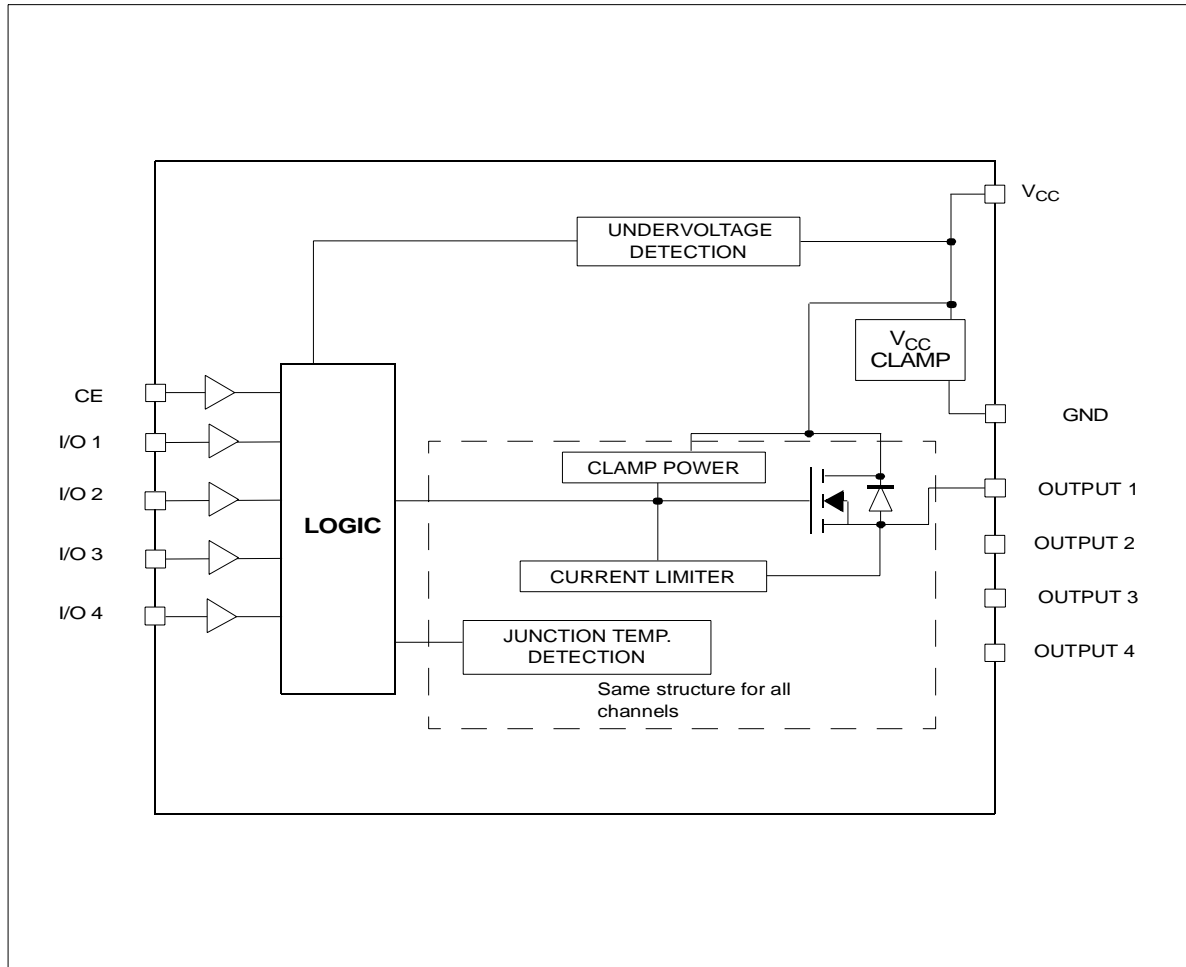
### APPLICATION

- Relay Driver
- LED Driver

### ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply voltage	41	V
-V <sub>CC</sub>	Reverse supply voltage	-0.3	V
-I <sub>GND</sub>	DC Ground pin reverse current	- 250	mA
I <sub>OUT</sub>	DC Output current	Internally Limited	A
-I <sub>OUT</sub>	Reverse DC output current	-1	A
I <sub>IN</sub>	DC Input current	+/- 10	mA
V <sub>ESD</sub>	Electrostatic discharge (R=1.5KΩ; C=100pF)		
	- I/On	4000	V
	- OUTn & Vcc	5000	V
T <sub>j</sub>	Junction operating temperature	Internally Limited	°C
T <sub>stg</sub>	Storage temperature	- 55 to 150	°C

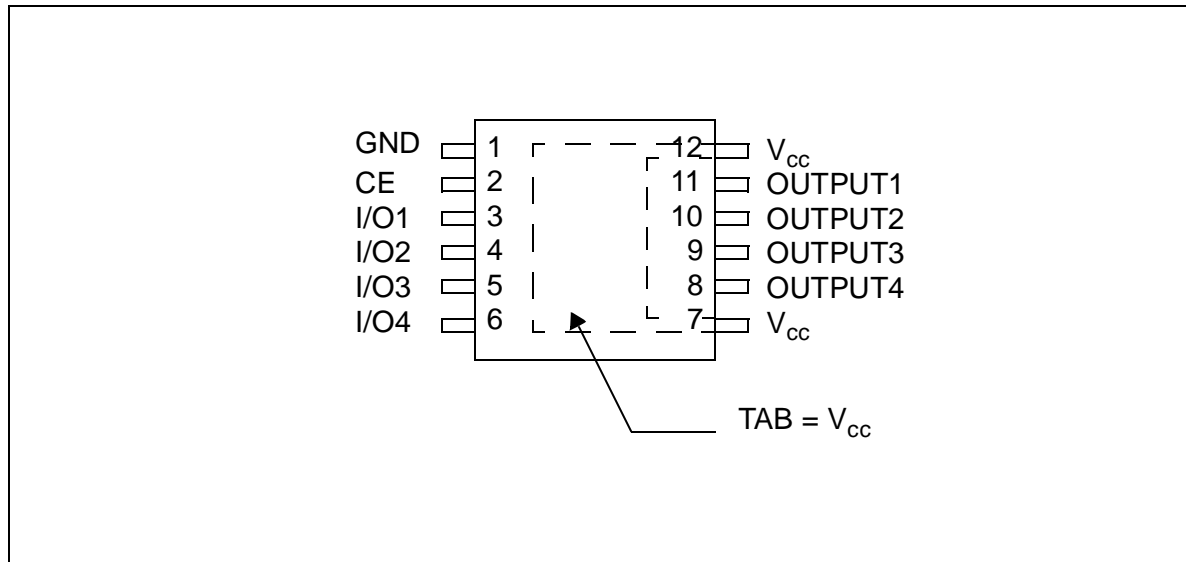
**BLOCK DIAGRAM**



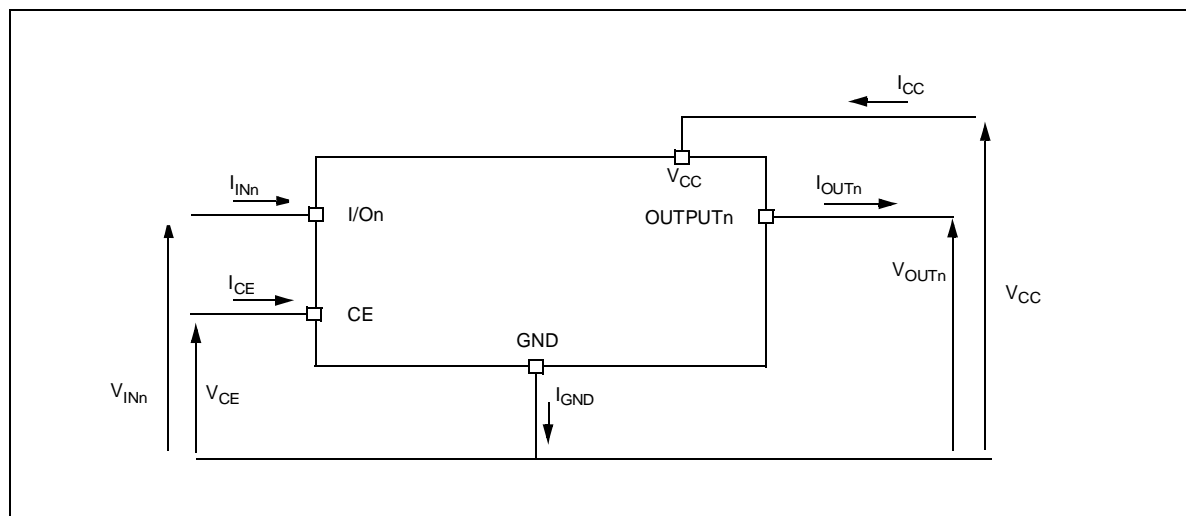
**PIN DEFINITIONS AND FUNCTIONS**

Pin No	Symbol	Function
TAB	V <sub>CC</sub>	Positive power supply voltage
7,12	V <sub>CC</sub>	Positive power supply voltage
1	GND	Logic ground
2	CE	Chip Enable
3	I/O 1	Input/Output of channel 1
4	I/O 2	Input/Output of channel 2
5	I/O 3	Input/Output of channel 3
6	I/O 4	Input/Output of channel 4
8	OUTPUT 4	High-Side output of channel 4
9	OUTPUT 3	High-Side output of channel 3
10	OUTPUT 2	High-Side output of channel 2
11	OUTPUT 1	High-Side output of channel 1

## CONNECTION DIAGRAM (TOP VIEW)



## CURRENT AND VOLTAGE CONVENTIONS



## VNQ500PEP

### THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	Max	4.6
$R_{thj-amb}$	Thermal resistance junction-ambient (*)	Max	60

(\*) When mounted on FR4 printed circuit board with 0.5 cm<sup>2</sup> of copper area (at least 35μ thick) connected to all TAB pins.

### ELECTRICAL CHARACTERISTICS (8V < V<sub>CC</sub> < 36V; -40°C < T<sub>j</sub> < 150°C, unless otherwise specified)

#### POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>CC</sub> (**)	Operating supply voltage		5.5	13	36	V
V <sub>USD</sub> (**)	Undervoltage shut-down		3	4	5.5	V
V <sub>OV</sub> (**)	Overshoot shutdown		36			V
R <sub>ON</sub>	On state resistance	I <sub>OUTn</sub> =0.25A; T <sub>j</sub> =25°C I <sub>OUTn</sub> =0.25A			500 1000	mΩ mΩ
I <sub>S</sub>	Supply current	V <sub>CE</sub> =V <sub>I/On</sub> =0V; V <sub>CC</sub> =13V; T <sub>case</sub> =25°C On state (all channels ON); V <sub>CC</sub> =13V			20 8	μA mA
I <sub>LGND</sub> (**)	Output current at turn-off	V <sub>CC</sub> =V <sub>CE</sub> =V <sub>I/On</sub> =V <sub>GND</sub> =13V V <sub>OUTn</sub> =0V			1	mA
I <sub>L(off)</sub> (**)	Off state output current	V <sub>I/On</sub> =V <sub>OUTn</sub> =0V	0		5	μA
I <sub>Loff2</sub> (**)	Off state output current	V <sub>I/On</sub> =0V, V <sub>OUTn</sub> =0V, V <sub>CC</sub> =13V; T <sub>case</sub> =25°C			1	μA

(\*\*) Per channel

#### SWITCHING (V<sub>CC</sub>=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t <sub>on</sub>	Turn-on time	R <sub>L</sub> =52Ω from 80% V <sub>OUT</sub> (*)		50		μs
t <sub>off</sub>	Turn-off time	R <sub>L</sub> =52Ω to 10% V <sub>OUT</sub> (*)		75		μs
dV <sub>OUT</sub> /dt <sub>(on)</sub>	Turn-on voltage slope	R <sub>L</sub> =52Ω from V <sub>OUT</sub> =1.3V to V <sub>OUT</sub> =10.4V (*)		0.3		V/μs
dV <sub>OUT</sub> /dt <sub>(off)</sub>	Turn-off voltage slope	R <sub>L</sub> =52Ω from V <sub>OUT</sub> =11.7V to V <sub>OUT</sub> =1.3V (*)		0.3		V/μs

(\*) see fig. 1a : switching time waveforms

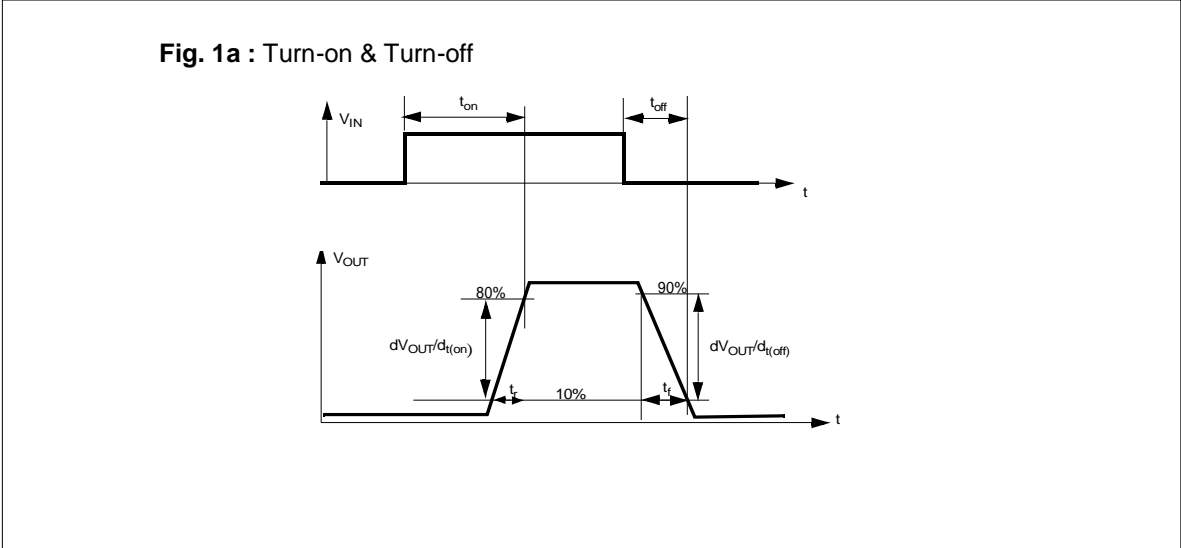
#### INPUT & CE PINS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>INL</sub>	I/O low level				1.25	V
I <sub>INL</sub>	Low level I/O current	V <sub>IN</sub> =1.25V	1			μA
V <sub>INH</sub>	I/O high level		3.25			V
I <sub>INH</sub>	High level I/O current	V <sub>IN</sub> =3.25V			10	μA
V <sub>I(hyst)</sub>	I/O hysteresis voltage		0.5			V
V <sub>ICL</sub>	I/O clamp voltage	I <sub>IN</sub> =1mA I <sub>IN</sub> =-1mA	6	6.8 -0.7	8	V V
V <sub>OL</sub>	I/O low level default detection	I <sub>IN</sub> =1mA, latched thermal shutdown			0.5	V

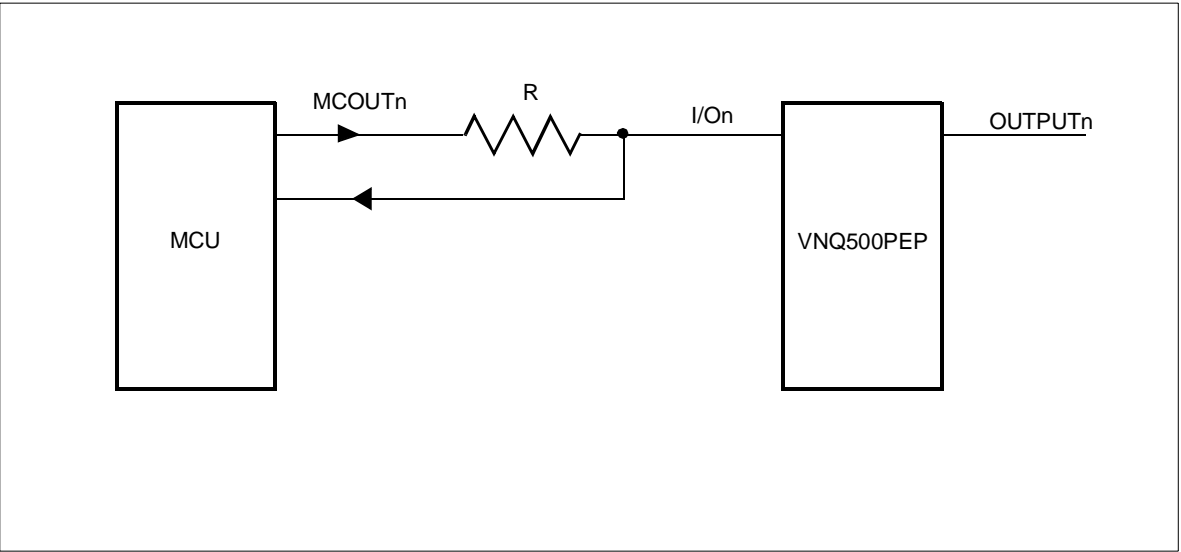
**ELECTRICAL CHARACTERISTICS (continued)****PROTECTIONS**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{TSD}$	Junction shut-down temperature		150	175	200	°C
$I_{lim}$	DC Short circuit current	$V_{CC}=13V$ ; $R_{LOAD}=10m\Omega$	0.35		0.7	A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT}=0.25$ A; $L=20mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V
$t_{reset}$	Thermal latch reset time	$T_J < T_{TSD}$ (see figure 3 in waveforms)			10	$\mu s$

Switching Time Waveforms



Driving circuit



## TRUTH TABLE

CONDITIONS	MCOUTn	CE	I/On	OUTPUTn
Normal operation	L	H	L	L
	H	H	H	H
Current limitation	L	H	L	L
	H	H	H	H
Overtemperature	L	H	L	L
	H	H	L (latched)	L
Undervoltage	L	H	L	L
	H	H	H	L
Stand-by	X	L	X	L

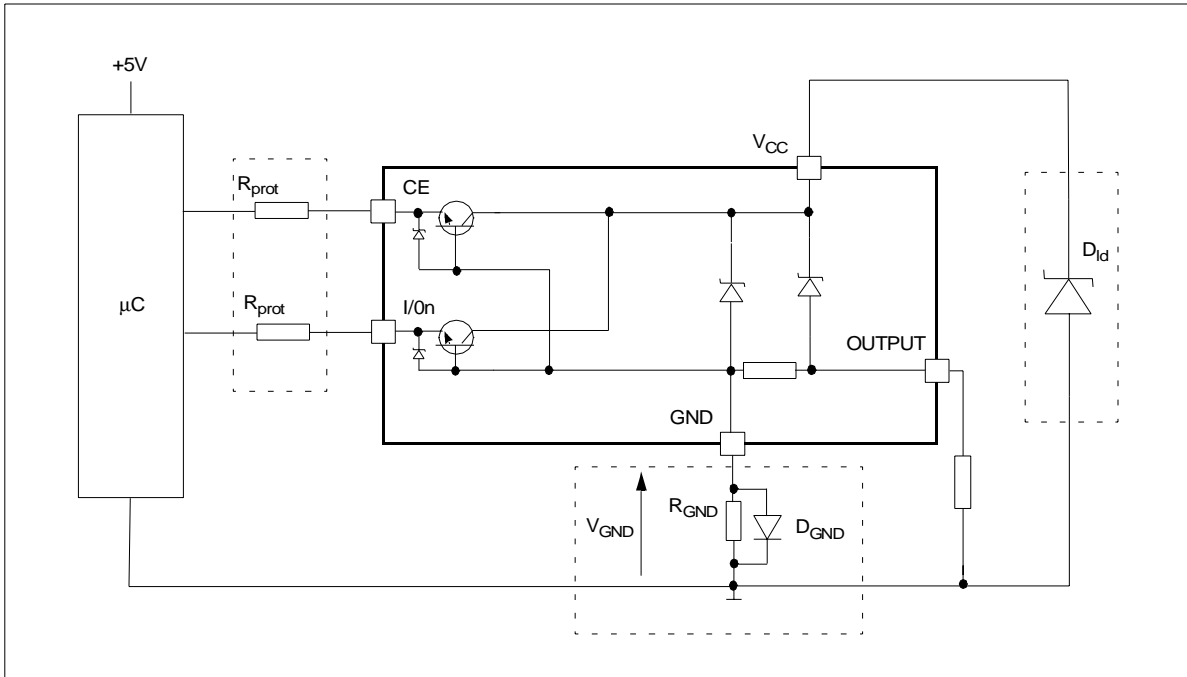
## ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 $\Omega$
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 $\Omega$
3a	-25 V	-50 V	-100 V	-150 V	0.1 $\mu$ s 50 $\Omega$
3b	+25 V	+50 V	+75 V	+100 V	0.1 $\mu$ s 50 $\Omega$
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 $\Omega$
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 $\Omega$

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

APPLICATION SCHEMATIC



**GND PROTECTION NETWORK AGAINST REVERSE BATTERY**

**Solution 1:** Resistor in the ground line ( $R_{GND}$  only). This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

- 1)  $R_{GND} \leq 600mV / (I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the of the device's datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggest to utilize Solution 2 (see below).

**Solution 2:** A diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND} = 1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\approx 600mV$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

**LOAD DUMP PROTECTION**

$D_{id}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds  $V_{CC}$  max DC rating. The same applies if the device will be subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

**µC I/Os PROTECTION:**

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

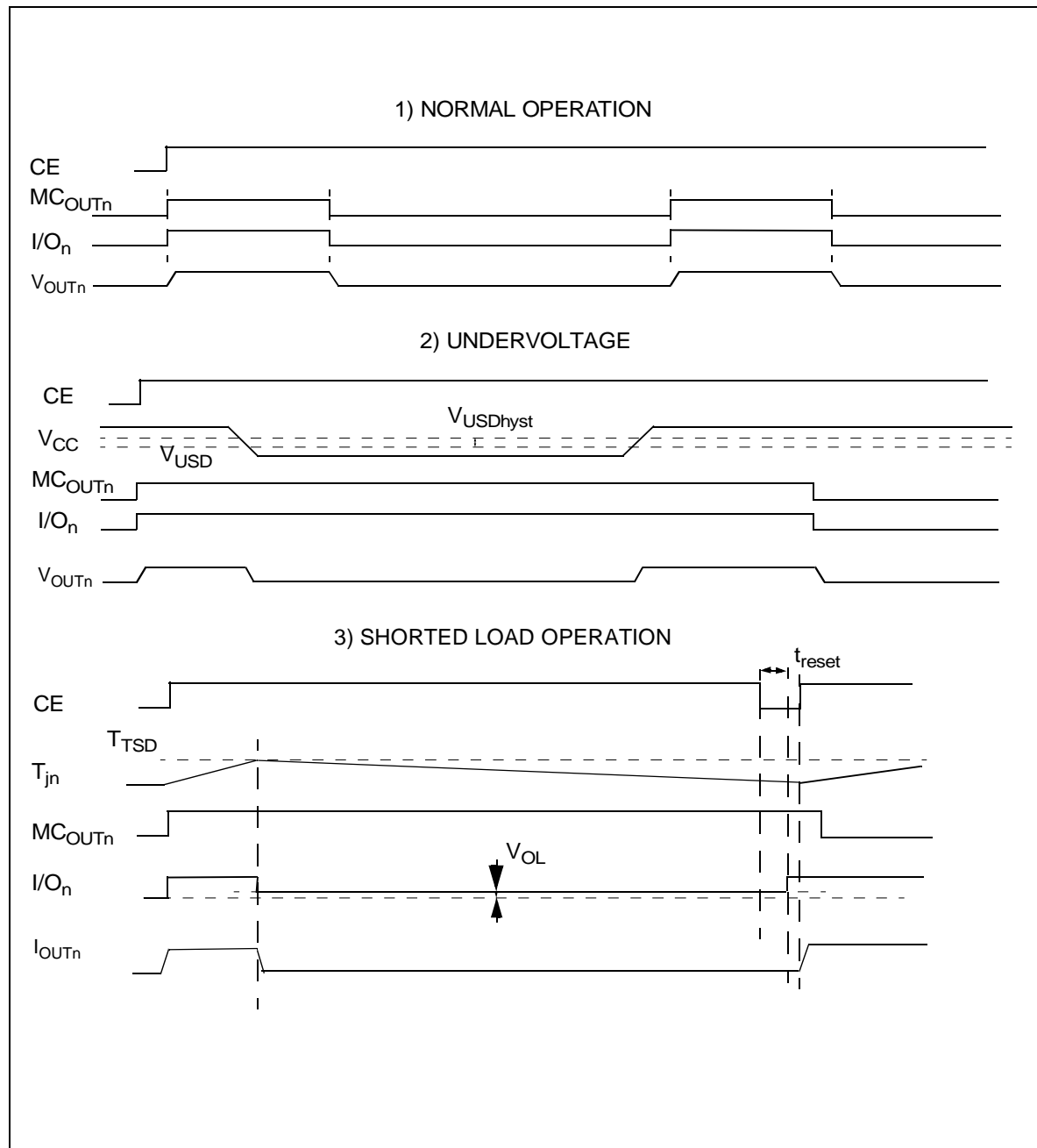
For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended  $R_{prot}$  value is  $10k\Omega$ .

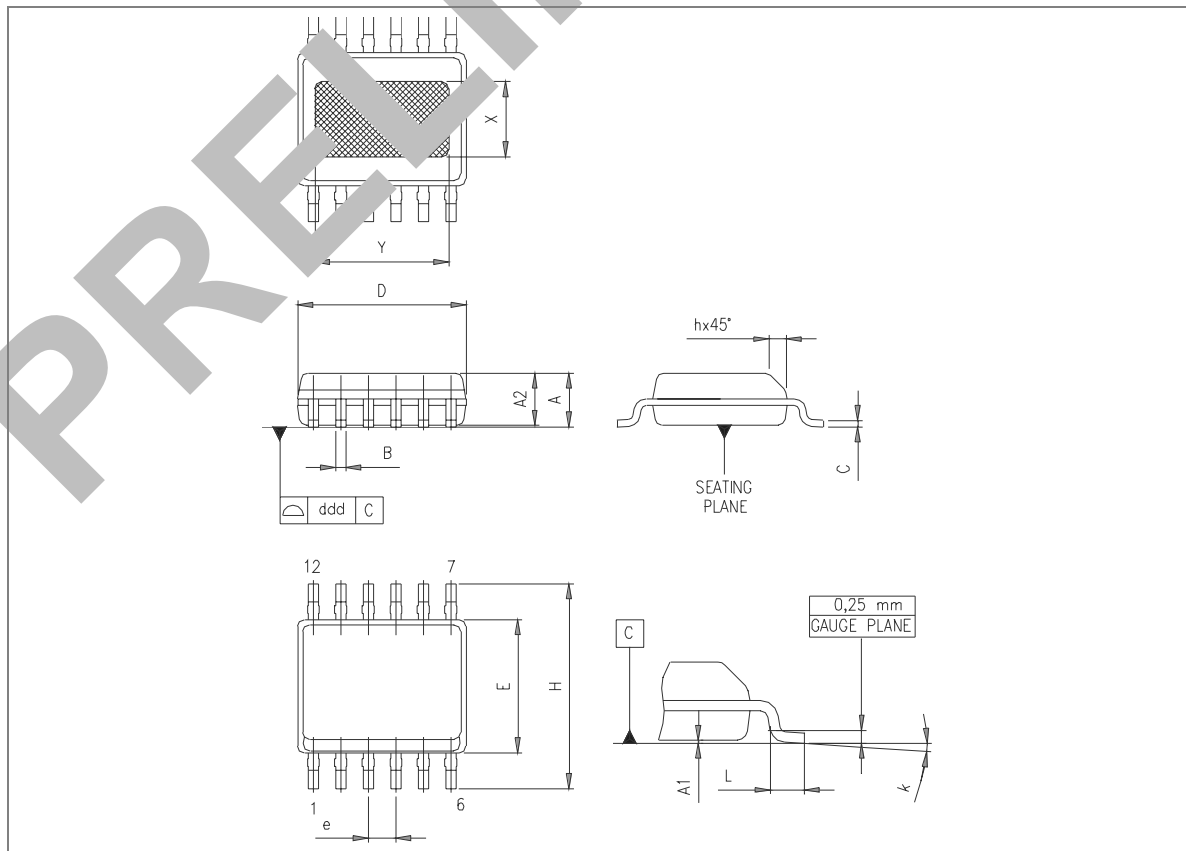


## Waveforms



**PowerSSO-12™ MECHANICAL DATA**

DIM.	mm.		
	MIN.	TYP	MAX.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100



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