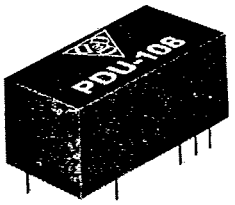
Programmable Delay Units

SERIES: PDU-108

ECL Interfaced (3 BIT)

data delay devices, inc.



Features:

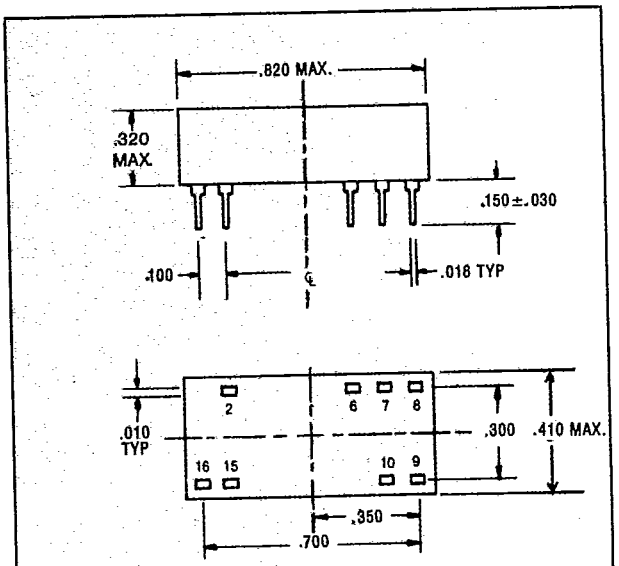
- Digitally programmable in 8 delay steps.
- Delay increments of 1/2 ns thru 50 ns.
- Fits standard 16 pins DIP socket.
- Output ECL interfaced.

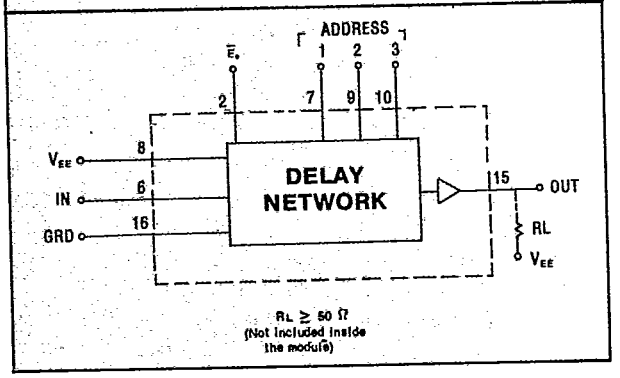
Specifications:

- Logic 1 input voltage: −.980 V.
- Logic 1 input current: 10 ma.
- Logic 0 input voltage: −1.65 V.
- Logic 0 input current: −20 ma.
- Logic 1 output voltage: −.96 V.
- Logic 0 output voltage: −1.65 V.
- Operating temperature: 0° to 70°C.
- Storage temperature: −55° to + 125°C.
- Power dissipation: −290 mw typ. (no load).
- Temperature coefficient: 100 PPM/°C.
- Delay variation: Monotonic in one direction.
- Total delay tolerance: ± 5% or 1 ns whichever is greater.
- Inherent delay (T_{DO}): 5 ns typ.
- Propagation delay:
  Address to output (T_{SUA}): = 5 ns typ.
  Enable to output (T_{SUE}): = 2 ns typ.

Test Conditions:

- Input pulse-width: 150% of total delay.
- Input pulse rise-time: ≤6 ns.
- Input pulse voltage: −1.5 V.
- V_{EE} supply voltage: −5 V.
- V_{EE} supply current: 56 ma typ.
- Operating temperature: 25°C.





TRUTH TABLE

Enable ($\overline{E_0}$)	Address (Bit No.) 3	2	1	Delay Out
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	1	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1	ϕ	ϕ	ϕ	0

1 = High
0 = Low
ϕ = Don't care
T_0 = Reference or inherent delay of circuit.
T_1 to T_7 = Multiplier of incremental delay.

Part No.**	Min. Delay Increment (ns)	Total Delay* Change (ns)
PDU-108-.5	.5 ± .3	3.5
PDU-108-1	1 ± .4	7
PDU-108-2	2 ± .4	14
PDU-108-3	3 ± .5	21
PDU-108-5	5 ± .6	35
PDU-108-10	10 ± 1	70
PDU-108-20	20 ± 1.5	140
PDU-108-40	40 ± 2	280
PDU-108-50	50 ± 2.5	350

*This delay value does not include the T_0 delay.
**Other delay increments available on request.

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