1.1 Scope.

This specification covers the detail requirements for a hybrid, fast, 16-bit successive approximation analog-to-digital converter including internal clock, reference and comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD1378SD/883B
−2	AD1378TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32E.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage	±18 V
Logic Supply Voltage	+7 V
Analog Inputs (Pins 24 & 25)	±25 V
Digital Inputs	−0.3 V to V_L +0.3 V
Junction Temperature	+175°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 12°C/W
θ_{JA} = 38°C/W

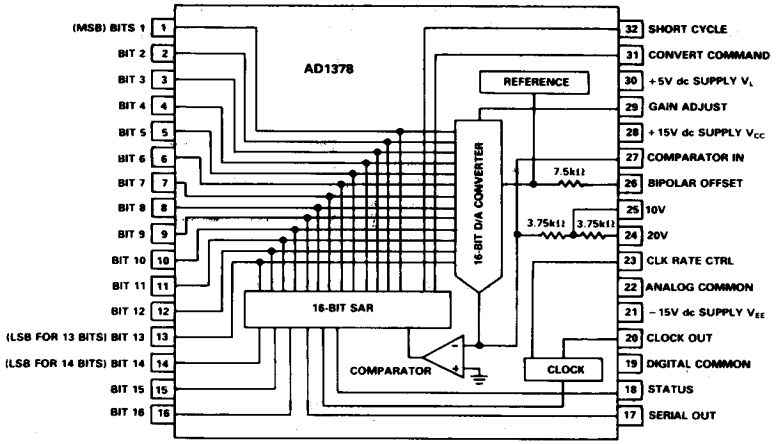
AD1378—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Conditions[1]	Units
Analog Input Voltage Ranges Bipolar Unipolar	V_{IN}	−1, 2	±2.5 ±5, ±10 0 to +5 0 to +10 0 to +20					V
Input Impedance 0 to +5 V, ±2.5 V 0 to +10 V, ±5 V 0 to +20 V, ±10 V	R_{IN}	−1, 2	1.88 3.75 7.50					kΩ typ[2]
Gain Error	V_{GE}	−1, 2	0.1	0.1			10 V Unipolar 20 V Bipolar	±% of FSR max
Gain Drift	V_{GD}	−1, 2	15		15		10 V Unipolar 20 V Bipolar	±ppm/°C max
Unipolar Offset Error	V_{OSE}	−1, 2	0.1	0.1			10 V Unipolar	±% of FSR max
Unipolar Offset Drift	V_{OSD}	−1, 2	4		4		10 V Unipolar	±ppm/°C max
Bipolar Offset Error	V_{OSE}	−1, 2	0.2	0.2			20 V Bipolar	±% of FSR max
Bipolar Offset Drift	V_{OSD}	−1, 2	10		10		20 V Bipolar	±ppm/°C max
Linearity Error	RA	−1	0.006			0.006	10 V Unipolar 20 V Bipolar	±% of FSR max
		−2, 3	0.003			0.003	10 V Unipolar 20 V Bipolar	
Differential Linearity Error	DNL	−1, 2	2	2	2	2	10 V Unipolar 20 V Bipolar	$\pm LSB_{14}$ max
Resolution, No Missing Codes	L_{NMC}	−1, 2		13	13			Bits min
+5 V Power Supply Sensitivity	PSRR	−1, 2		0.005	0.005		±5%	±% of FSR/% Δ V_S max
±15 V Power Supply Sensitivity	PSRR	−1, 2		0.003	0.003		±5%	±% of FSR/% Δ V_S max
Digital Output High Drive	V_{OH}	−1, 2		2.7	2.7		@ −100 μA	V min
Digital Output Low Drive	V_{OL}	−1, 2		0.4	0.4		@ 2.0 mA	V max
Digital Input Current Low Level Endpoint	I_{INL}	−1, 2		−0.4 −0.8	−0.4		V_{INL} = 0.4 V	mA max
Digital Input Current High Level	I_{INH}	−1, 2		0.02	0.02		V_{INH} = 2.7 V	mA max
Conversion Speed	t_C	−1, 2		17 15	17 15		16 Bit 14 Bit	μs max
+5 V Supply Drain	$+I_{DD}$	−1, 2		25	25			mA max
+15 V Supply Drain	$+I_{CC}$	−1, 2		25	25			mA max
−15 V Supply Drain	$-I_{CC}$	−1, 2		−40	−40			mA max
Power Dissipation	P_D	−1, 2		800	800			mW max
Power Supply Range	$+V_{DD}$ $\pm V_{CC}$	−1, 2	+5 ±15				±5% ±5%	V

NOTES
[1]V_{CC} = ±15 V, V_{DD} = +5 V, T_A = +25°C unless otherwise noted.
[2]Tolerance ±20%.
[3]Guaranteed no missing codes, −55°C to +85°C.

3.2.1 Functional Block Diagram and Terminal Assignments.

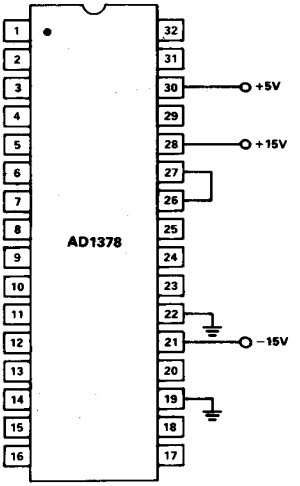


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



6.0 Gain and Offset Adjustment.

Gain Adjustment

The gain adjust circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300 kΩ resistor to the gain adjust Pin 29 as shown in Figure 1.

If no external trim adjustment is desired, Pin 29 (GAIN ADJ) may be left open.

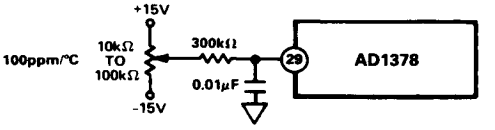


Figure 1. Gain Adjustment Circuit (±0.15% FSR)

Offset Adjustment

The zero adjust circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8 MΩ resistor to Comparator Input Pin 27 for all ranges. As shown in Figure 2, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200 ppm/°C tempco contributes a worst-case offset tempco of 32 $LSB_{14} \times 61$ ppm/$LSB_{14} \times 1200$ ppm/°C = 2.3 ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±16 LSB_{14}, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset tempco.

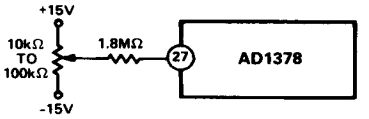


Figure 2. Offset Adjustment Circuit (±0.3% FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 3.

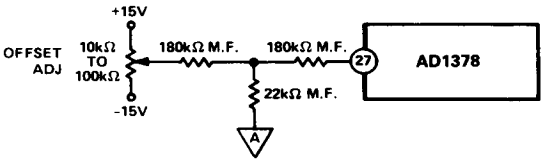


Figure 3. Low Tempco Zero Adjustment Circuit

In either adjust circuit, the fixed resistor connected to Pin 27 should be located close to this pin to keep the pin connection runs short. (Comparator Input Pin 27 is quite sensitive to external noise pickup and should be guarded by analog common.) If no external trim adjustment is desired, Pin 27 (OFFSET ADJ) may be left open.

6.1 Input Scaling.

The AD1378 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table 2. See Figure 4 for circuit details.

Table 2. AD1378 Input Scaling Connections

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	Connect Input Signal to
±10 V	COB	27	Input Signal	24
±5 V	COB	27	Open	25
±2.5 V	COB	27	Pin 27	25
0 V to +5 V	CSB	22	Pin 27	25
0 V to +10 V	CSB	22	Open	25
0 V to +20 V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and should be guarded by analog common.

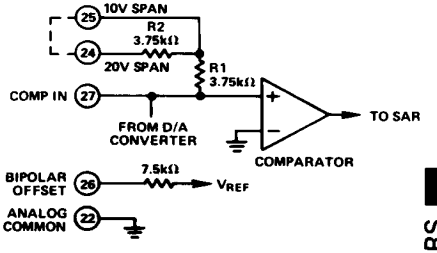


Figure 4. AD1378 Input Scaling Circuit

6.2 Digital Output Data.

Parallel data from TTL storage registers is in negative true form (Logic "1"=0 V and Logic "0"=2.4 V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data outputs change state on positive-going clock edges.

Table 3. Input Voltage Range and LSB Values

Analog Input Voltage Range		±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V
Code Designation		COB* or CTC**	COB* or CTC**	COB or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$
	n=8	78.13 mV	39.06 mV	19.53 mV	39.06 mV	19.53 mV
	n=10	19.53 mV	9.77 mV	4.88 mV	9.77 mV	4.88 mV
	n=12	4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV
	n=13	2.44 mV	1.22 mV	0.61 mV	1.22 mV	0.61 mV
	n=14	1.22 mV	0.61 mV	0.31 mV	0.61 mV	0.31 mV
	n=15	0.61 mV	0.31 mV	0.15 mV	0.31 mV	0.15 mV

NOTES
*COB=Complementary Offset Binary.
**CTC=Complementary Twos Complement – achieved by using an inverter to complement the most significant bit to produce ($\overline{MSB}$).
***CSB=Complementary Straight Binary.

6.3 Clock Rate Control.

The AD1378 may be operated at faster conversion times by connecting the Clock Rate Control (Pin 23) to an external multiturn trim potentiometer (TCR <100 ppm/°C) as shown in Figure 5. The integral linearity and differential linearity errors will vary with speed.

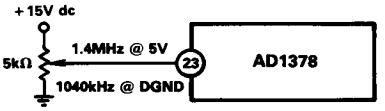


Figure 5. Clock Rate Control Circuit

6.3.1 Short Cycle Input.

A Short Cycle Input, Pin 32, permits the timing cycle shown in Figure 6 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, Pin 32 is connected to Bit 11 output Pin 11. The conversion cycle then terminates and the STATUS flat resets after the Bit 10 decision (timing diagram of Figure 6). Short cycle connections and associated 8-, 10-, 12-, 13-, 14- and 15-bit conversion times are summarized in Table 4, for a 1040 kHz clock.

Table 4. Short Cycle Connections

Resolution Bits	(% FSR)	Maximum Conversion Time (μs)	Status Flag Reset	Connect Short Cycle Pin 32 to Pin:
16	0.0015	16.4	t_{16}	N/C (Open)
15	0.003	15.4	t_{15}	16
14	0.006	14.4	t_{14}	15
13	0.012	13.5	t_{13}	14
12	0.024	12.5	t_{12}	13
10	0.100	10.6	t_{10}	11
8	0.390	8.7	t_8	9

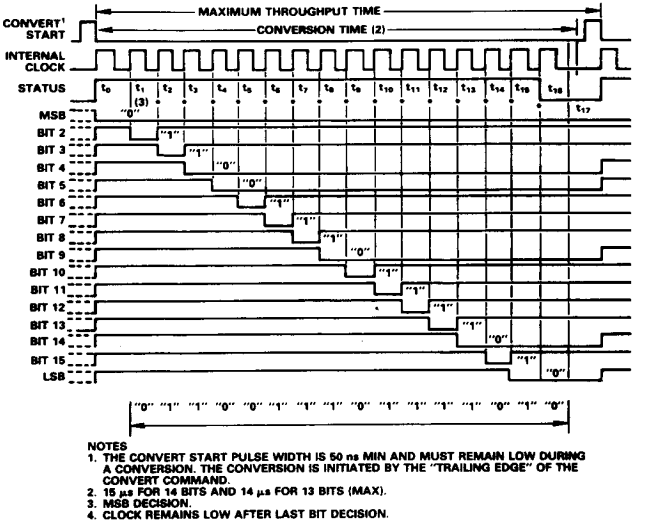


Figure 6. Timing Diagram (Binary Code 0110011101111010)