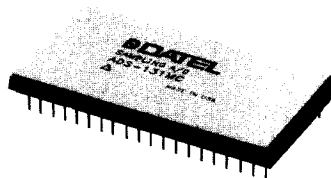


FEATURES

- 12-bit resolution
- Internal Sample/Hold amplifier
- 5.0 MHz minimum throughput
- Samples up to Nyquist
- Functionally complete
- Small 40-pin DIP
- Low-power, 3.65 Watts
- Three-state output buffers
- High input bandwidth
- Overflow pin
- No missing codes



GENERAL DESCRIPTION

DATEL's ADS-131 is a 12-bit, functionally complete, sampling A/D converter packaged in a small 40-pin DIP. A 5.0 MHz minimum throughput rate in digitizing sinusoidal signals is achieved while only dissipating 3.65 Watts.

APPLICATIONS

- Spectrum analysis
- Imaging
- Radar
- Medical instrumentation
- High-speed data acquisition systems

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V	40	DIGITAL GROUND
2	-15V	39	COMP BIN
3	ANALOG GROUND	38	ENABLE
4	ANALOG -5V	37	DATA READY
5	ANALOG +5V	36	DIGITAL +5V
6	ANALOG INPUT	35	START CONVERT
7	S/H OUT	34	OVERFLOW
8	DIGITAL +5V	33	BIT 1 (MSB)
9	DIGITAL GROUND	32	BIT 2 OUT
10	DIGITAL -5V	31	BIT 3 OUT
11	OFFSET ADJUST	30	BIT 4 OUT
12	ANALOG +5V	29	BIT 5 OUT
13	ANALOG GROUND	28	BIT 6 OUT
14	ANALOG -5V	27	DIGITAL GROUND
15	GAIN ADJUST	26	BIT 7 OUT
16	+10V REFERENCE	25	BIT 8 OUT
17	+15V SUPPLY	24	BIT 9 OUT
18	ANALOG -5V	23	BIT 10 OUT
19	ANALOG GROUND	22	BIT 11 OUT
20	ANALOG +5V	21	BIT 12 OUT (LSB)

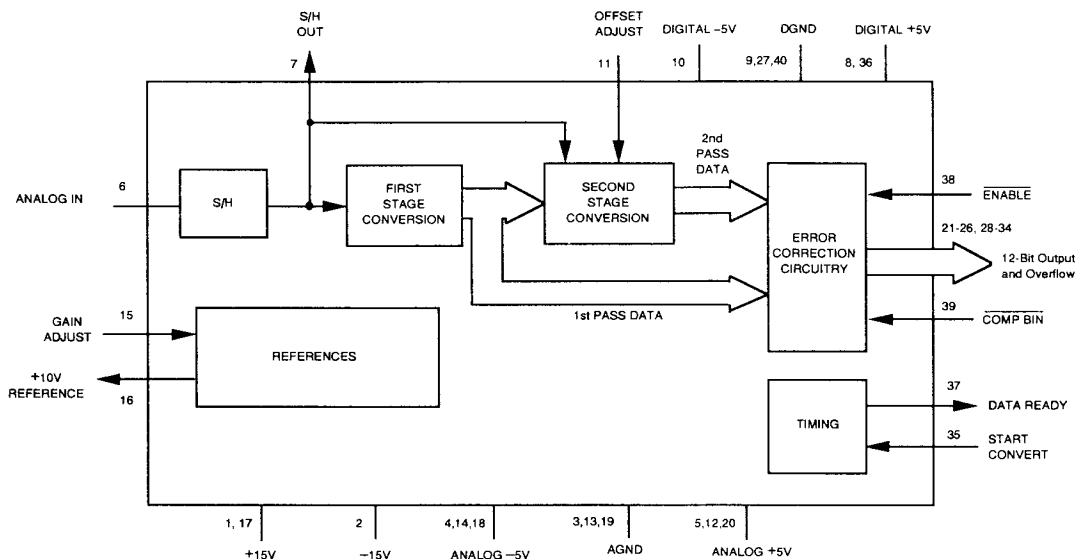


Figure 1. ADS-131 Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 1,17)	0 to +18	Volts dc
-15V Supply (Pin 2)	0 to -18	Volts dc
+5V Supply (Pin 5, 8,12,20,36)	-0.5 to +7.0	Volts dc
-5V Supply (Pin 4,10,14,18)	+0.5 to -7.0	Volts dc
Digital Inputs (Pins 35,38,39)	-0.3 to +5.5	Volts dc
Analog Input (Pin 6)	±5	Volts dc
Lead Temp.(10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and ±5V dc unless otherwise specified.

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog				
Input Voltage Range	—	±1.25	—	V dc
Input Impedance	50	160	—	kOhm
Input Capacitance	—	2.5	10	pF
Digital				
Logic Levels				
Logic "1"	2.0	—	—	V dc
Logic "0"	—	—	0.8	V dc
Logic Loading "1"	—	—	5.0	μA
Logic Loading "0"	—	—	-200	μA
OUTPUTS				
Resolution	12 Bits			
Output Coding (Pin 39 High) (Pin 39 Low)	Offset Binary Complementary Offset Binary			
Logic Levels				
Logic "1"	2.4	—	—	V dc
Logic "0"	—	—	0.4	V dc
Logic Loading "1"	—	—	-160	μA
Logic Loading "0"	—	—	6.4	mA
Internal Reference Voltage, (pin 16)				
0 to +70 °C	9.9	10.0	10.1	V dc
Drift	—	±3	±8.5	ppm/ °C
External Current	—	—	2	mA
PERFORMANCE				
Int. Non-Linear., $f_{IN} = 2.5\text{MHz}$	—	—	±2	LSB
Diff. Non-Linear., $f_{IN} = 2.5\text{MHz}$	—	—	±1.5	LSB
Full Scale Absolute Accuracy (Refer to Tech. note 1)	—	±0.4	±0.8	%FSR
Bipolar Zero Error, (Refer to Tech. note 1)	—	±0.2	±0.4	%FSR
Bipolar Offset Error, (Refer to Tech. note 1)	—	±0.2	±0.4	%FSR
Gain Error (Refer to Tech. note 1)	—	±0.2	±0.4	%FSR

DYNAMIC PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Conversion Rate	5.0	—	—	MHz
Total Harm. Distort.(-0.5 dB)				
DC to 500 kHz	—	-70	-66	FS, -dB
500 kHz to 2.5 MHz	—	-67	-62	FS, -dB
Signal-to-Noise Ratio (w/o distortion, -0.5 dB)				
DC to 500 kHz	65	70	—	FS, -dB
500 kHz to 2.5 MHz	62	69	—	FS, -dB
Signal-to-Noise Ratio and Distortion (-0.5 dB)				
DC to 500 kHz	63	66	—	FS, -dB
500 kHz to 2.5 MHz	60.5	65	—	FS, -dB
Spurious Free Dyn. Range ①				
DC to 500 kHz	66	70	—	FS, -dB
500 kHz to 2.5 MHz	63	67	—	FS, -dB
Effective Bits				
DC to 500 kHz	—	11.0	—	Bits
500 kHz to 2.5 MHz	9.8	10.5	—	Bits
Two-tone Intermodulation Distortion ($f_{IN} = 2.2\text{ MHz}$, 2.3 MHz, $f_s = 5\text{ MHz}$)	—	-75	—	dB
Input Bandwidth				
Small Signal (-20 dB)	50	65	—	MHz
Large Signal (-3 dB)	30	40	—	MHz
Slew Rate	75	100	—	V/μSec
Aperture Delay Time	—	5	7	nSec
Aperture Uncertainty	—	5	7	psec
S/H Acquisition Time to 0.01% FS (2.5V step)	—	50	70	nSec
Feedthrough Rejection 2.5V step	—	-66	-62	dB
Overvoltage Recovery, ±2.5 V	—	100	200	nSec
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply (Vcc)	14.25	15.0	15.75	V dc
-15V dc Supply (VEE)	-14.25	-15.0	-15.75	V dc
+5V dc Supply (VDD)	4.75	5.0	5.25	V dc
-5V dc Supply (VSS)	-4.75	-5.0	-5.25	V dc
Power Supply Current				
+15V dc Supply	—	25	28	mA
-15V dc Supply	—	-30	-33	mA
+5V dc Supply ②	—	310	342	mA
-5V dc Supply	—	-250	-275	mA
Power Dissipation	—	3.65	4.00	Watts
Power Supply Rejection	—	0.05	0.1	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, case				
-MC	0	—	70	°C
Thermal Resistance				
Junction-to-Case	—	3.9	—	°C/W
Case-to-Ambient	—	9.1	—	°C/W
Storage Temperature Range	-65	—	150	°C
Weight	0.56 oz. (16 grams) Max.			
Package Type	40-pin ceramic TDIP			

① The same specifications apply to Inband Harmonics.

② +5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or to reduce the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 15 (tie pin 15 to ANALOG GROUND for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 11 for zero/offset adjustment (tie pin 11 to ANALOG GROUND for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter.

In most cases, users will use a single +5V supply for both analog +5V and digital +5V (applicable for the -5V supply also). Should users have separate supplies, the difference between the analog and digital supply should be within ± 100 mV to avoid performance degradation.

Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital power supply pins with a 2.2 μ F, 25V tantalum electrolytic capacitor in parallel with a 0.1 μ F ceramic capacitor to their respective analog and digital grounds. Use of chip capacitors is recommended.

4. Obtain offset binary output coding by tying COMP BIN (pin 39) to +5V dc. To obtain complementary offset binary output coding, tie pin 39 to ground. The pin 39 signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To obtain three-state outputs, connect ENABLE (pin 38) to a logic "1" (high). Otherwise, connect pin 38 to a logic "0" (low).

6. The ADS-131 guarantees its specified throughput rate over the temperature range when the START CONVERT pulse of 10 nanoseconds minimum, 190 nanoseconds maximum is provided at the specified rate. START CONVERT pulses greater than 190 nanoseconds will result in slower throughput rates.

7. The ADS-131 is capable of digitizing sinusoidal input frequencies up to the Nyquist frequency. The acquisition time for pulse or dc level signals is 70 nanoseconds maximum over the 0 to +70 °C temperature range.

8. The specifications listed in Figure 3 (timing diagram) apply over the full operating temperature range unless otherwise specified.

9. The OVERFLOW pin (pin 34) goes high for signals greater than +full scale (no overflow flag given for signals greater than -FS). The OVERFLOW pin is a three-state output and is enabled by the ENABLE line (pin 38).

10. The ADS-131 has a one pipeline delay in obtaining output data. Refer to the Timing Diagram in Figure 3.

11. ADS-131 goes into the hold mode on the rising edge of the START CONVERT pulse.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 2.

Apply a pulse of 10 nanoseconds typical to the START CONVERT input (pin 35) at a rate of 500 kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments

Apply a precision voltage reference source between the analog input (pin 6) and analog ground. Adjust the output of the reference source per Table 2 for the bipolar zero adjustment (zero $+1/2$ LSB). Adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN (pin 39 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 39 tied low (complementary offset binary).

3. Full-Scale Adjustment

Set the output of the voltage reference used in step 2 to the value shown in Table 2 for the bipolar gain adjustment (+FS -1 $1/2$ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 with COMP BIN (pin 39) tied high or between 0000 0000 0000 and 0000 0000 0001 with pin 39 tied low.

To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

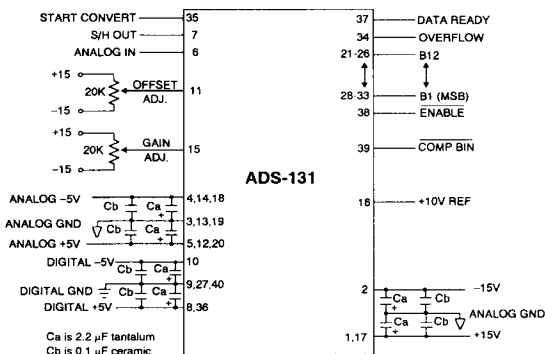


Figure 2. Typical ADS-131 Connections

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST 0 + $1/2$ LSB	GAIN ADJUST +FS - $1/2$ LSB
± 1.25 Vdc	+305 μ V dc	+1.249085V dc.

Table 3. Output Coding

BIPOLAR SCALE	INPUT RANGE (Volts dc) $\pm 1.25V$	OUTPUT CODING			
		OFFSET BINARY		COMP OFF. BINARY	
		MSB	LSB	MSB	LSB
+FS -1 LSB	+1.24939V	1111	1111 1111	0000	0000 0000
+3/4 FS	+0.9375V	1110	0000 0000	0001	1111 1111
+1/2 FS	+0.625V	1100	0000 0000	0011	1111 1111
0	0.0000V	1000	0000 0000	0111	1111 1111
-1/2 FS	-0.625V	0100	0000 0000	1011	1111 1111
-3/4 FS	-0.9375V	0010	0000 0000	1101	1111 1111
-FS +1 LSB	-1.24939V	0000	0000 0001	1111	1111 1110
-FS	-1.2500V	0000	0000 0000	1111	1111 1111

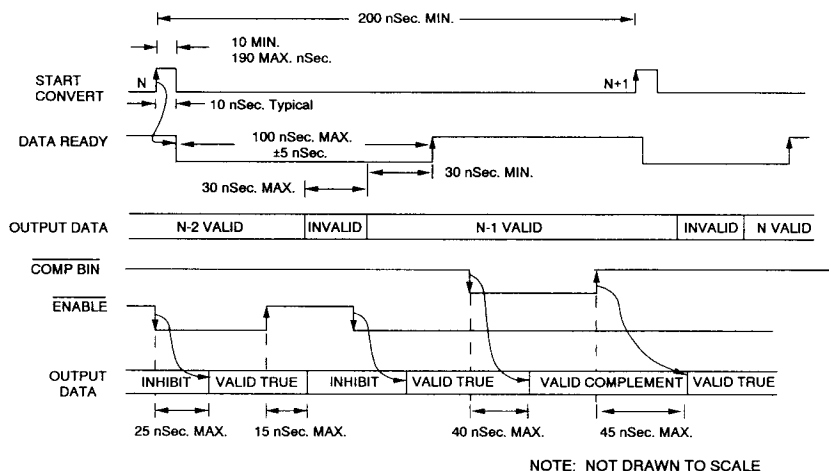
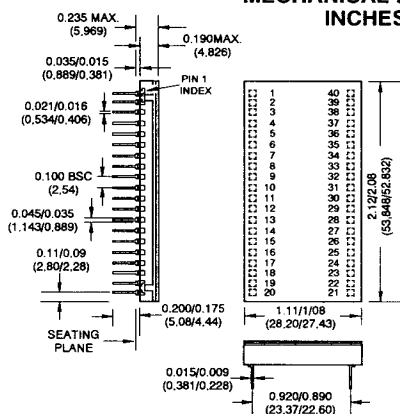


Figure 3. ADS-131 Output Data Timing

MECHANICAL DIMENSIONS
INCHES (mm)

ORDERING INFORMATION

MODEL
NUMBEROPERATING
TEMP. RANGE

ADS-131MC

0 to +70 °C

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 40 required.

For availability of extended temperature versions, contact DATEL.

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DATEL, Inc.
INTERNATIONAL:

11 CABOT BOULEVARD, MANSFIELD, MA 02048-1194 TEL. (508) 339-3000 / FAX (508) 339-6356
DATEL (UNITED KINGDOM) Basingstoke Tel. (256) 469-085 • DATEL (FRANCE) Tel. (1) 3460.0101
DATEL (GERMANY) Tel. (89) 53-0741 • DATEL (JAPAN) Tokyo Tel. (3) 779-1031 • Osaka Tel. (6) 354-2025