7.0 DC ELECTRICAL SPECIFICATIONS

7.1 OPERATING CONDITIONS

OPERATING CONDITIONS					
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**	**NOTES**
Vdd	Supply voltage	4.75	5.25	V	
Idd	Supply current (active)		372	mA	1
Idd	Supply current (standby)		26	mA	2
Idd	Supply current (low power)		100	µA	3
Ta	Ambient temperature	0	50@still air 70@air flow	°C	6
Vil	Input low voltage	Vss-0.5	0.8	V	
Vih	Input high voltage	2.0	Vdd+0.5	V	
Ii	Input leakage current	-10	10	µA	
Vol	Output low voltage (Iol=-4mA)		0.4	V	5
Voh	Output high voltage (Ioh=4mA)	2.4		V	5
Voh	Output high voltage (Ioh=100µA)	Vdd-0.8		V	5
Iol	Output low current		4	mA	
Ioh	Output high current		-4	mA	
Ioz	Output leakage current	-10	10	µA	
Ioz	High impedance leakage current	-10	10	µA	
Cin	Input capacitance		5	pF	
Cout	Output capacitance		7	pF	
Cio	Input/Output capacitance		7	pF	
Comax	Maximum capacitance load for all signals (including self loading)		50	pF	4

Notes:

1) Dynamic current (Iout=0mA) - see Figure 24
2) Dynamic current; no data transfers
3) Static current (clock high)
4) Timings referenced to this load
5) Output AC timings referenced to Vol for high to low transitions and Voh for low to high transitions.
6) For ambient temperature with regard to air flow see graph in Figure 25

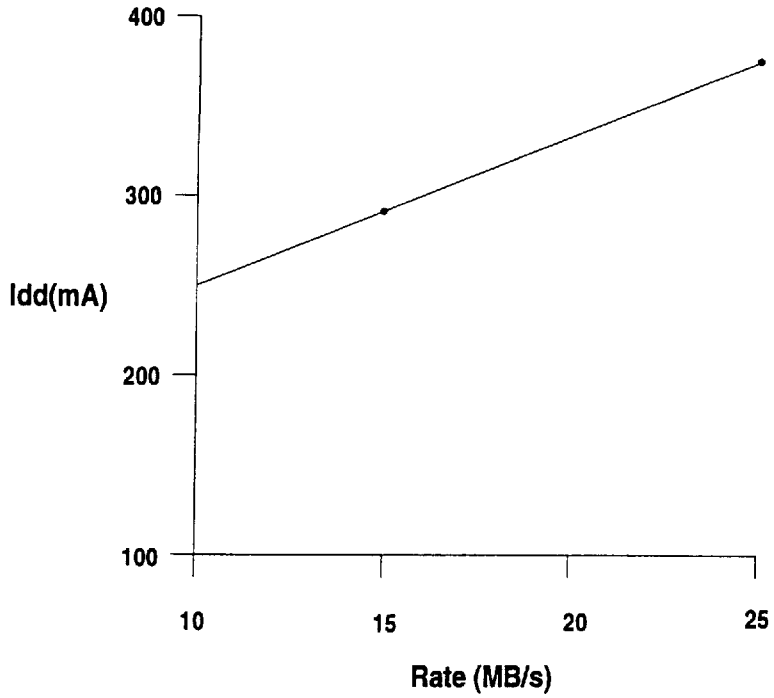
7.2 ABSOLUTE MAXIMUM STRESS RATINGS

ABSOLUTE MAXIMUM STRESS RATINGS					
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**	**NOTES**
Tstg	Storage temperature	-50	150	°C	
Vdd	Supply voltage	-0.5	7	V	
Vin	Input voltage	Vss-0.5	Vdd+0.5	V	
Ilp	Latch-up current		100	mA	
ESD	Electro-static discharge	-2,000	+2,000	V	1

Notes:

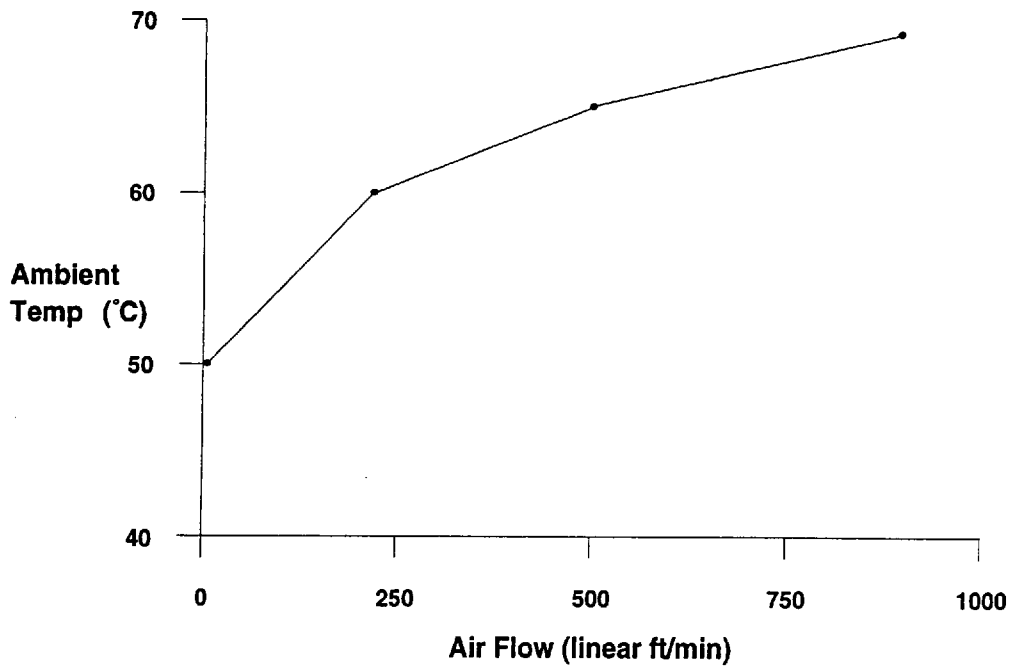
1) Human body model

Figure 17: Power vs. Data Rate at 25 MHz Operation



Note: Power scales linearly with frequency at a given data rate.

Figure 18: Ambient Temperature vs. Air Flow (25 MB/s)



8.0 AC ELECTRICAL SPECIFICATIONS

Figure 19: Data Interface Timing

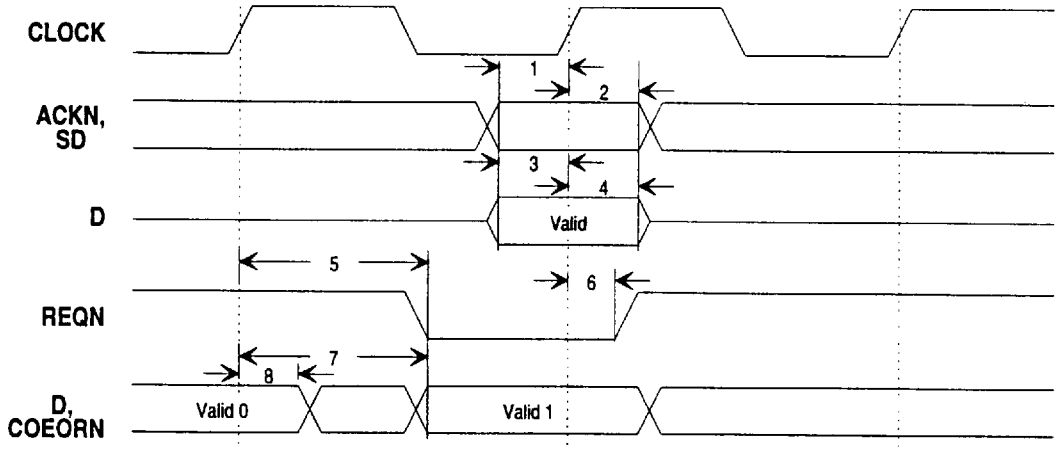


Table 6: Data Port Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	CIACKN, DIACKN, COACKN, DOACKN and SD setup time	15		ns	
2	CIACKN, DIACKN, COACKN, DOACKN and SD hold time	3.5		ns	2
3	D-bus input setup time	10		ns	
4	D-bus input hold time	3		ns	
5	REQN delay (non-EOR case)		18	ns	1
6	REQN hold (non-EOR case)	3		ns	
7	D-bus, COEORN output delay		23	ns	
8	D-bus, COEORN output hold	4		ns	

Notes:

1) Production test condition is 50 pF. Delay is decreased 2 ns with 25 pF load guaranteed by design or characterization.

2) Input timings are referenced to 1.4 volts.

Figure 20: Request Deasserts at EOR, Strobe Condition of DSC=0-3, 6-15; ERC=0

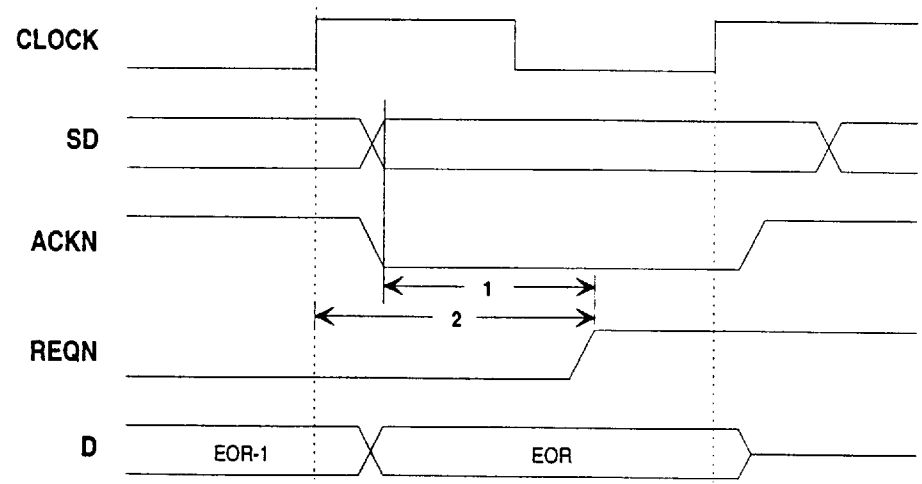


Figure 21: Request Deasserts at EOR, Strobe Condition of DSC=0-3, 6-15; ERC=1

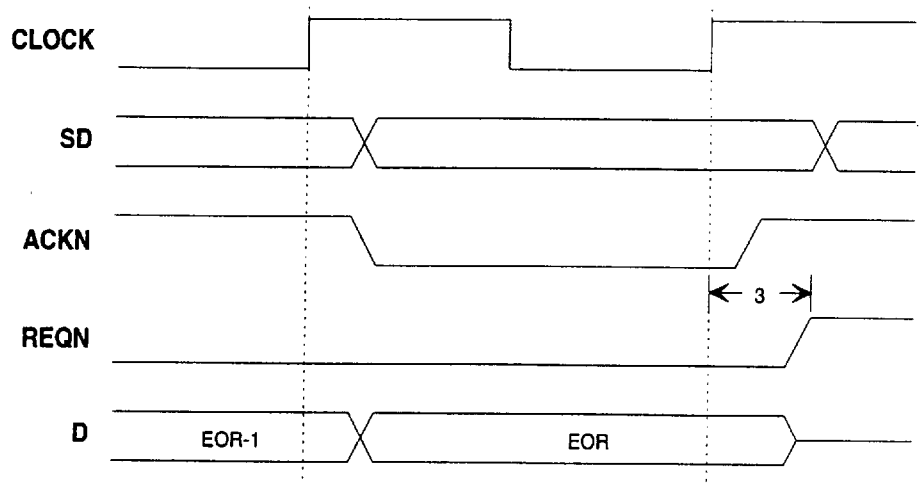


Figure 22: Request Deasserts at EOR, Strobe Condition of DSC=4 or 5; ERC=0

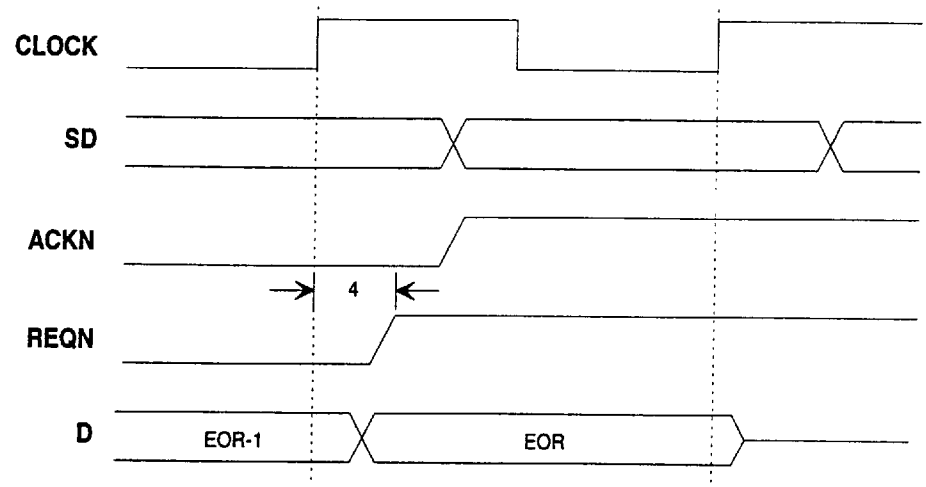


Figure 23: Request Deasserts at EOR, Strobe Condition of DSC=4 or 5; ERC=1

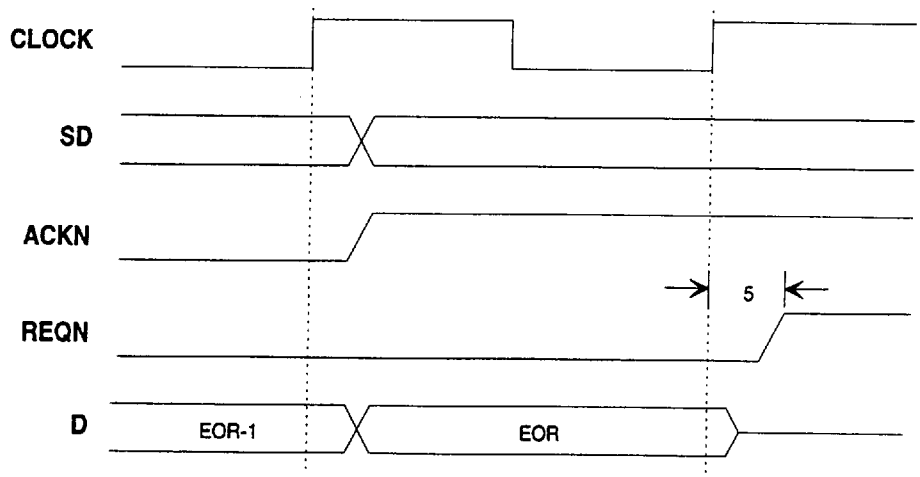


Table 7: Request vs. EOR Timing

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	ACKN, SD to REQN DSC=0-15; ERC=0		20	ns	1
2	CLOCK to REQN DSC=0-3, 6-9; ERC=0		21	ns	1
	CLOCK to REQN DSC=10-15; ERC=0		23	ns	1
3	CLOCK to REQN DSC=0-3, 6-15; ERC=1		18	ns	1
4	CLOCK to REQN DSC=4, 5; ERC=0		21	ns	1
5	CLOCK to REQN DSC=4, 5; ERC=1		18	ns	1

Notes:

1) Production test condition is 50 pF. Delay is decreased 2 ns with 25 pF load guaranteed by design or characterization.

Figure 24: Output Enable Timing

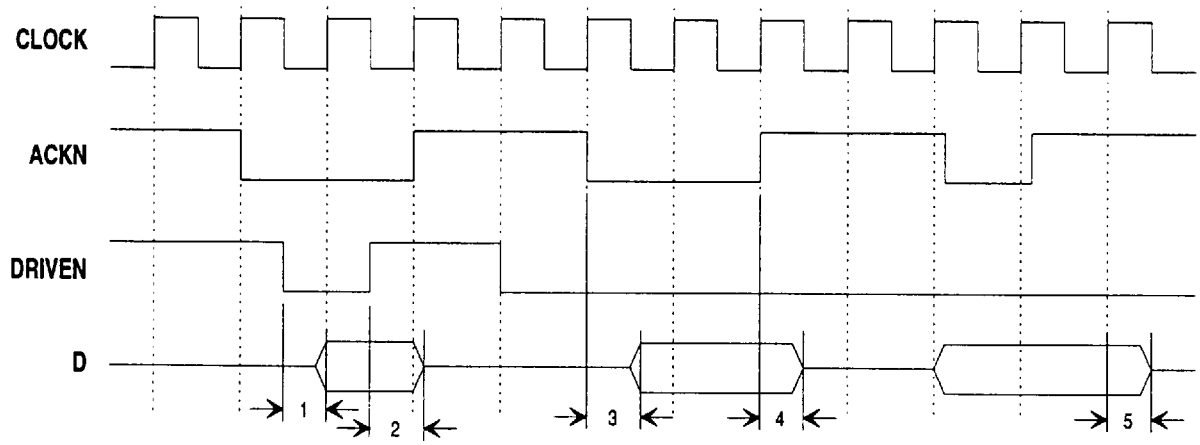


Table 8: Output Enable Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	DRIVEN to D valid		20	ns	
2	DRIVEN to D tristate		10	ns	
3	Signal to D valid		20	ns	
4	Signal to D tristate		10	ns	
5	CLOCK to D tristate (DSC=0100, 0101)		15	ns	

Figure 25: Video Input Port Timing

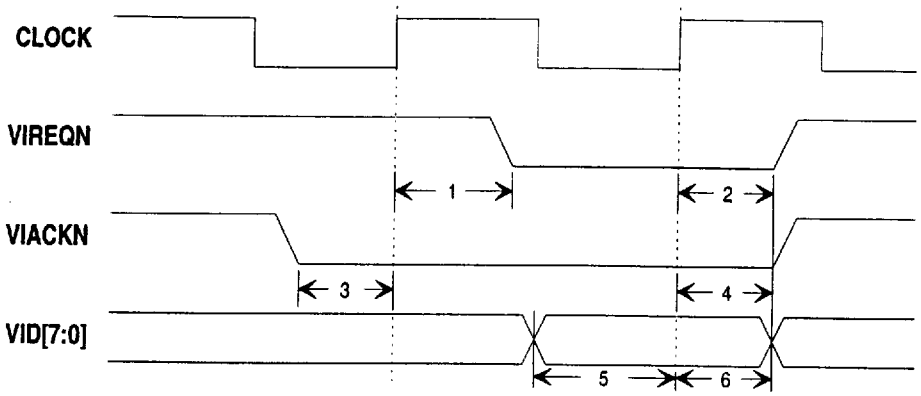


Table 9: Video Input Port Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	VIREQN delay		16	ns	
2	VIREQN hold	3.6		ns	
3	VIACKN setup	8		ns	
4	VIACKN hold	3		ns	
5	VID setup	15		ns	
6	VID hold	3		ns	

Figure 26: Video Output Port Timing

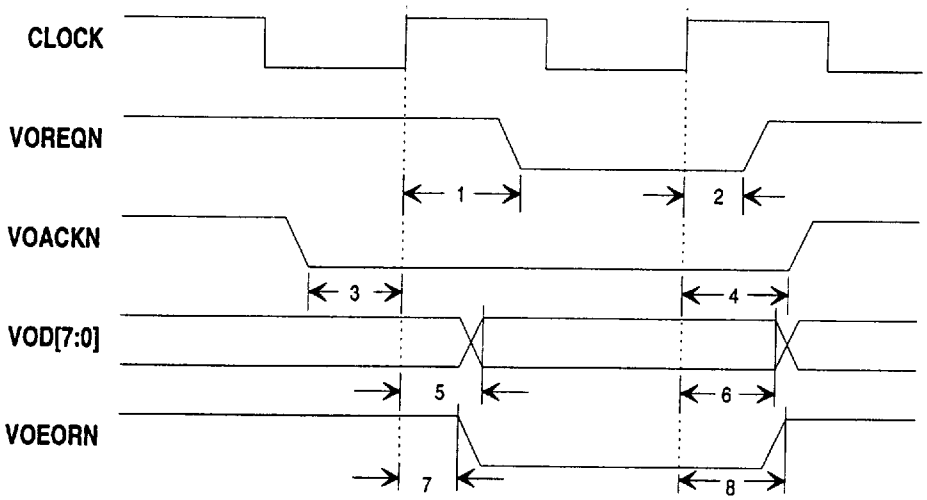


Table 10: Video Output Port Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	VOREQN delay		19	ns	1
2	VOREQN hold	4		ns	
3	VOACKN setup	8		ns	
4	VOACKN hold	3		ns	
5	VOD delay		21	ns	1
6	VOD hold	3.7		ns	
7	VOEORN hold	3.7		ns	
8	VOEORN delay		21	ns	1

Notes:

1) Production test condition is 50 pF. Delay is decreased 2 ns with 25 pF load guaranteed by design or characterization.

Figure 27: Microprocessor Interface Timing (PROCMODE[1]=0)

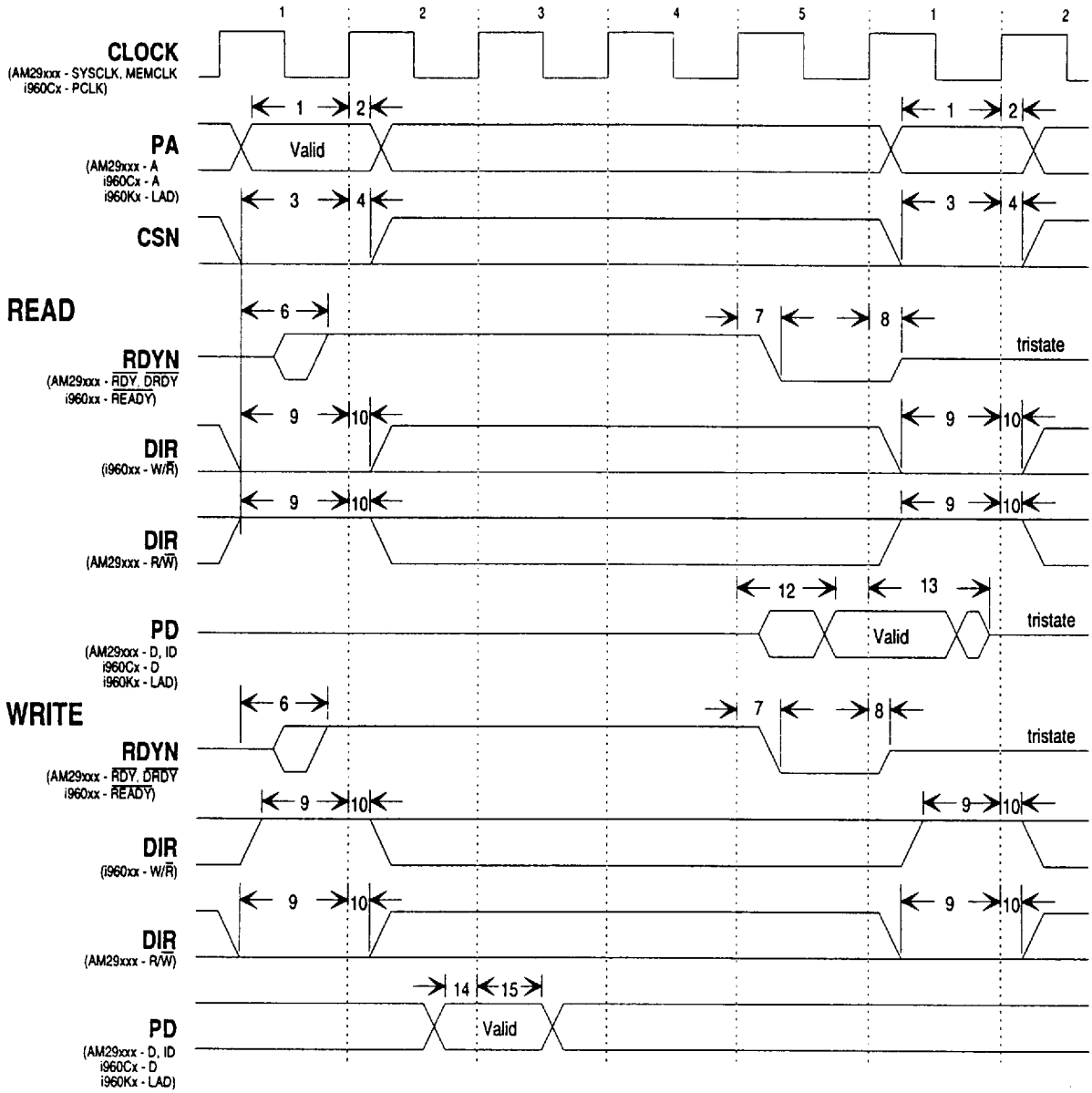


Figure 28: Microprocessor Interface Timing (PROCMODE[1]=1)

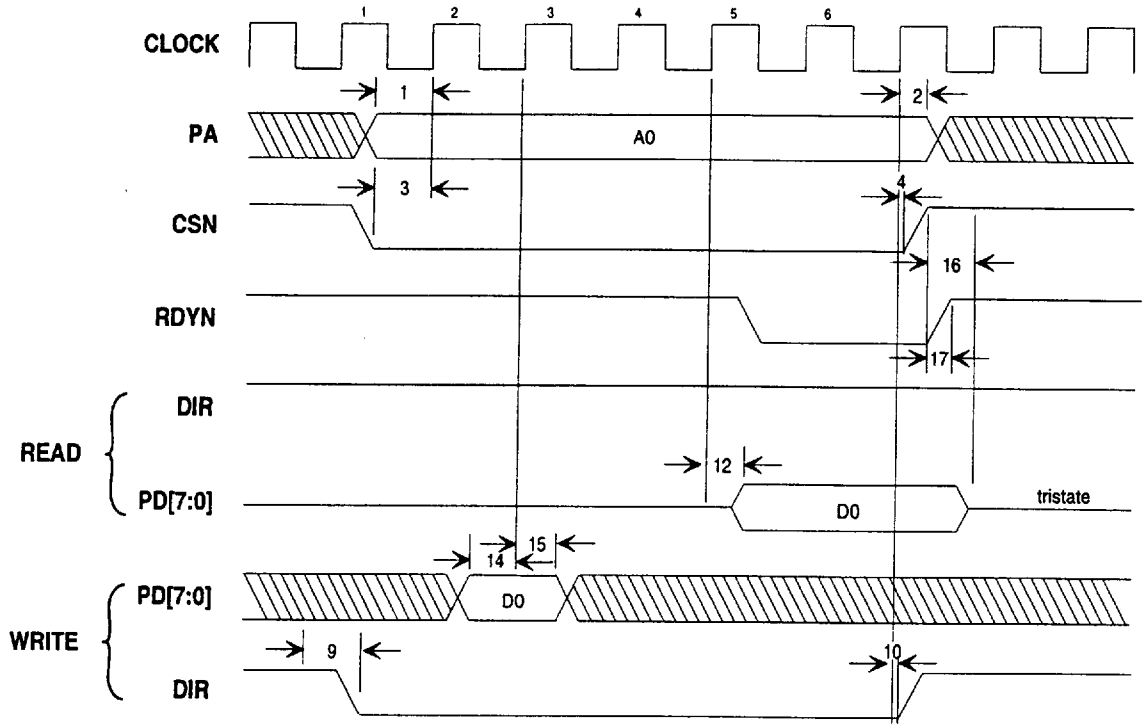


Table 11: Microprocessor Interface Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	PA setup time	10		ns	
2	PA hold time	3		ns	
3	CSN setup time	10		ns	
4	CSN hold time	3		ns	
6	CSN to valid RDYN		15	ns	
7	RDYN valid delay		20	ns	
8	RDYN drive disable		10	ns	
9	DIR setup time	10		ns	
10	DIR hold time	3		ns	
12	PD valid delay		20	ns	
13	PD drive disable		12	ns	
14	PD setup time	10		ns	
15	PD hold time	3		ns	
16	CSN high to PD tristate		10	ns	
17	CSN high to RDYN high		15	ns	

Figure 29: Interrupt Timing

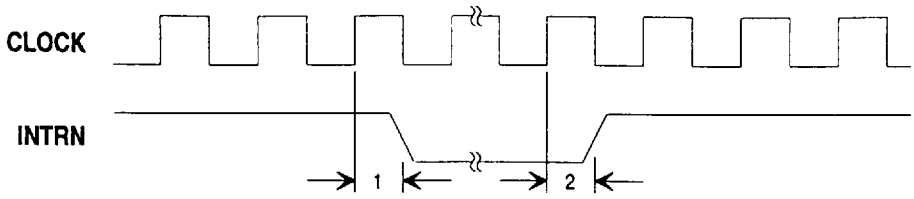


Table 12: Interrupt Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	INTRN delay time		15	ns	
2	INTRN hold time	3		ns	

Figure 30: Clock Timing

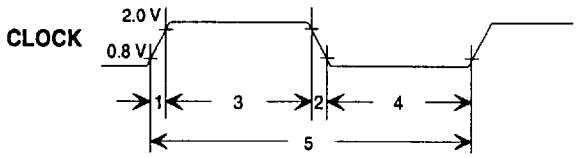


Table 13: Clock Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	CLOCK rise time		5	ns	
2	CLOCK fall time		5	ns	
3	CLOCK high time	15		ns	
4	CLOCK low time	16		ns	
5	CLOCK period	40	∞	ns	

Figure 31: Power On Reset Timing

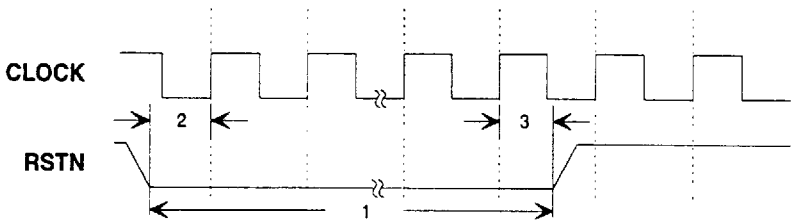


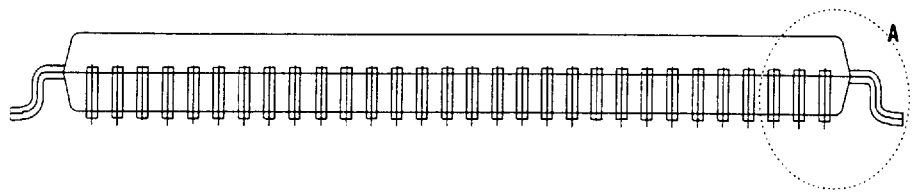
Table 14: Power On Reset Timing Requirements

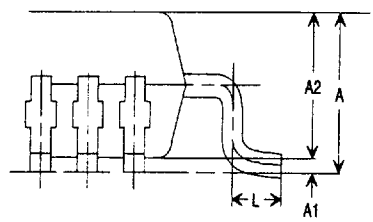
NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	RSTN low pulsewidth	10		clocks	
2	RSTN setup to CLOCK rise	15		ns	1
3	RSTN hold time	2		ns	1

Notes:

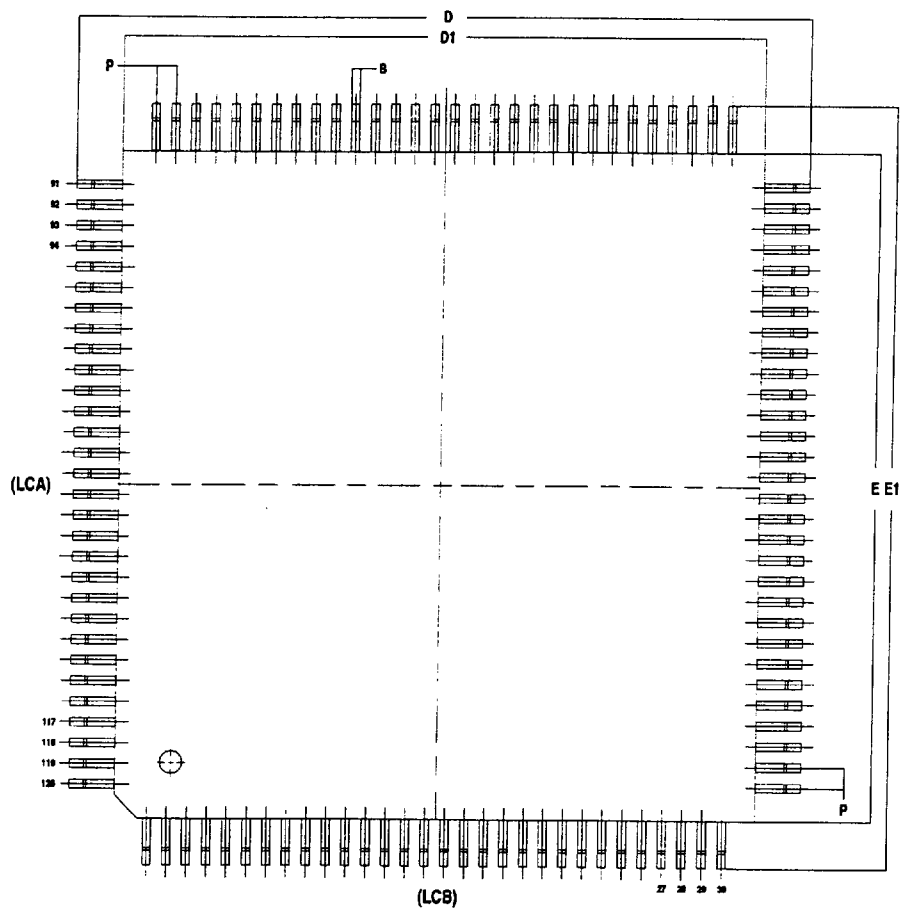
1) RSTN signal can be asynchronous to the CLOCK signal. It is internally synchronized to the rising edge of CLOCK.

9.0 PACKAGE SPECIFICATIONS





DETAIL A



PLASTIC QUAD FLAT PACK PACKAGE DIMENSIONS
(All dimensions are in mm)

SYMBOL	NUMBER OF PIN AND SPECIFICATION DIMENSION		
	120		
	SB		
	MIN	NOM	MAX
(LCA)		30	
(LCB)		30	
A	3.22	3.57	3.97
A1	0.05	0.25	0.50
A2	3.17	3.32	3.47
D	31.65	31.90	32.15
D1	27.90	28.00	28.10
E	31.65	31.90	32.15
E1	27.90	28.00	28.10
L	0.65	0.75	0.95
P		0.80	
B	0.25	0.35	0.45

10.0 ORDERING INFORMATION

10.1 AVAILABLE PARTS

PART NUMBER	DESCRIPTION
AHA3410A-025 PQC	25 MBytes/sec Simultaneous Lossless Data Compression/Decompression Coprocessor IC

10.2 PART NUMBERING

AHA	3410	A-	025	P	Q	C
Manufacturer	Device Number	Revision Level	Speed Designation	Package Material	Package Type	Test Specification

Device Number:
3410

Revision Letter:
A

Package Material Codes:
P Plastic

Package Type Codes:
Q Quad Flat Pack

Test Specifications:
C Commercial 0°C to +70°C

11.0 RELATED PUBLICATIONS

11.1 AHA TECHNICAL PUBLICATIONS

DOCUMENT #	DESCRIPTION
ANDC12	AHA Application Note - AHA3410 StarLite™ Designer's Guide
ANDC13	AHA Application Note - Compression Performance: StarLite™: ENCODEB2 on Bitonal Images
ANDC14	AHA Application Note - StarLite™ Evaluation Software
GLGEN1	General Glossary of Terms
STARSW	StarLite™ Evaluation Software (Windows™)*
PCTP127	T. Summers, "Applying Compression/Decompression in High-Performance Printers and Copiers", Conference Proceeding: *The 1995 Silicon Valley Personal Computer Design Conference and Exposition*
	T. Summers, "Compression Technologies in Printers", A paper presentation at Seybold Conference, 1995

** Evaluation Software is also available for UNIX operating system, upon request.*

11.2 OTHER TECHNICAL PUBLICATIONSS

DOCUMENT #	DESCRIPTION
7th Edition, 1995	AMD's Fusion29K® Catalog
6th Edition, 1995	Intel's Solutions 960® Catalog
1996 Edition	Motorola's 68K & ColdFIRE® Source Book: High Performance Embedded Systems