T-46-13-25

Am27X040

4 Megabit (524,288 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time—120 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**

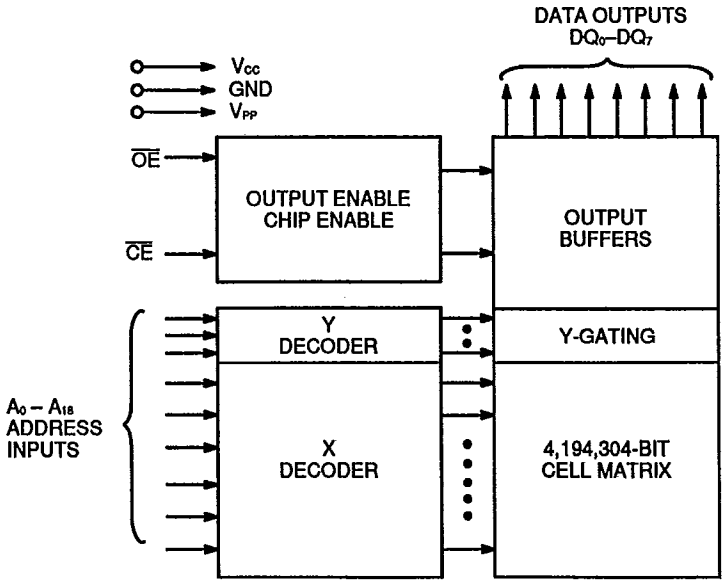
GENERAL DESCRIPTION

The Am27X040 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 524,288 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 120 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X040 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

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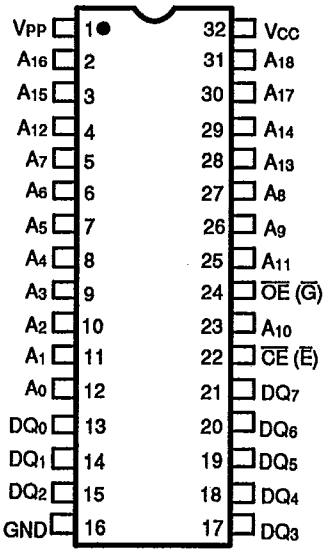
Family Part No.	Am27X040			
Ordering part No:				
±5% VCC Tolerance	-125	-155		
±10% VCC Tolerance	—	-150	-200	-250
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	65	75	100

CONNECTION DIAGRAMS

Top View

PLASTIC DIP



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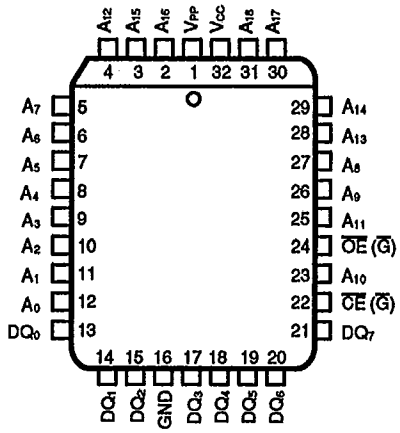
PLCC



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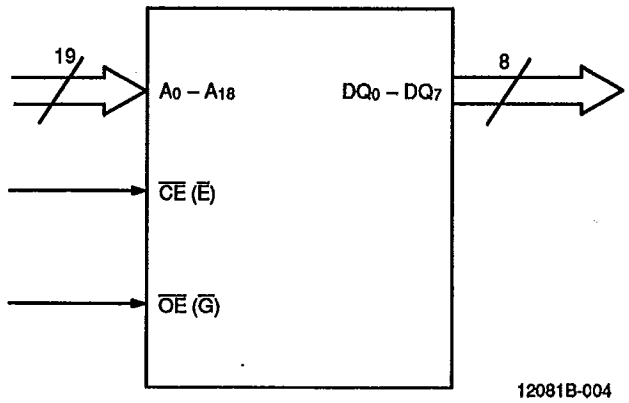
Note: 1. JEDEC nomenclature is in parentheses.
2. The 32-Pin DIP to 32-Pin PLCC configuration varies from the JEDEC 28-Pin DIP to 32-Pin PLCC configuration.

LOGIC SYMBOL



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PIN DESCRIPTION

A0 – A18	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0 – DQ7	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
VPP	=	Vcc Supply Voltage
Vcc	=	Vcc Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

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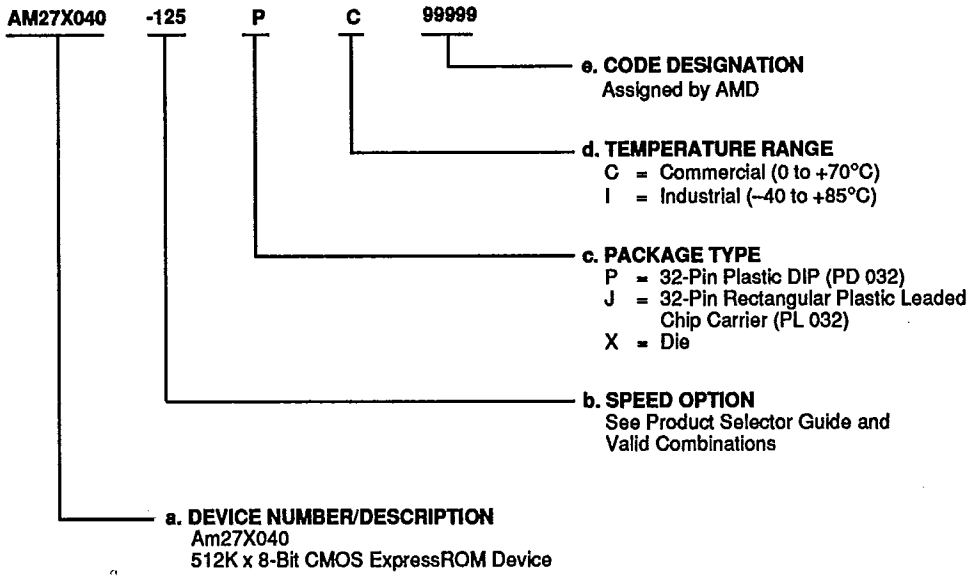
AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
AM27X040-125 AM27X040-150 AM27X040-155 AM27X040-200 AM27X040-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X040 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X040 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X040 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Pins / Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	High Z
Standby (TTL)	V_{IH}	X	X	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except Vcc	–0.6 to Vcc + 0.6 V
Vcc	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to Vcc +2.0 V for periods of up to 20 ns.

OPERATING RANGES

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Commercial (C) Devices

Case Temperature (Tc)	0 to +70°C

Industrial (I) Devices

Case Temperature (Tc)	–40 to +85°C

Supply Read Voltages:

Vcc for Am27X040–XX5	+4.75 to +5.25 V
Vcc for Am27X040–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

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Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		40	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	$V_{CC} - 0.8$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		0.7 V_{CC}	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		40	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

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CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	PD032 Typ.	PD032 Max.	PL032 Typ.	PL032 Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X040 must not be removed from, or inserted into, a socket or board when Vcc is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to Vcc + 2.0 V for periods of up to 20 ns.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol JEDEC	Parameter Symbol Standard	Parameter Description	Test Conditions		-125	-155 -150	-200	-250	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.					ns
				Max.	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.					ns
				Max.	40	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	ns
				Max.					

Notes:

1. Vcc must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X040 must not be removed from, or inserted into, a socket or board when Vcc is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

SWITCHING TEST CIRCUIT

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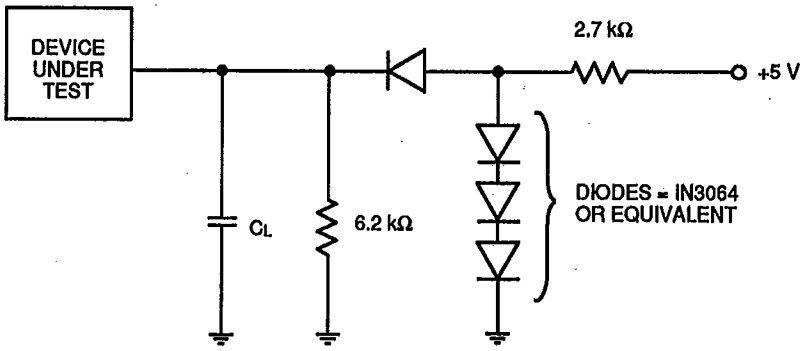

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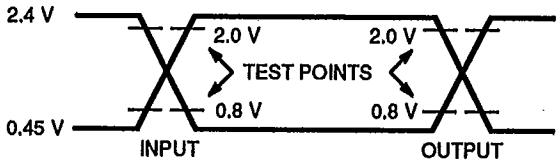
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



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AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

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WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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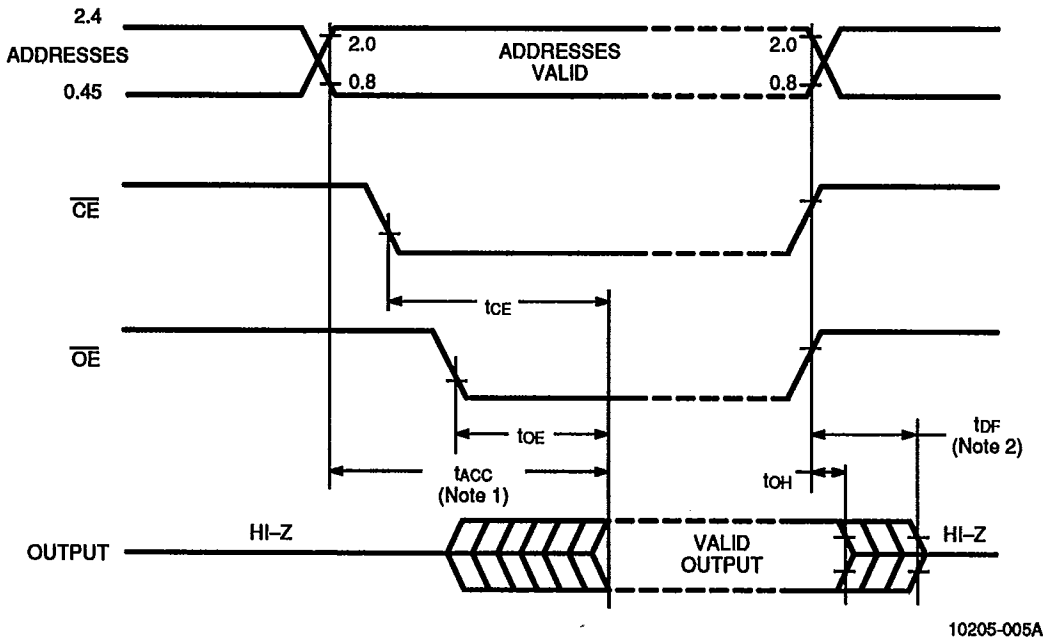
SWITCHING WAVEFORMS



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Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.