ADVANCE INFORMATION

Am53CF94LV

Low-Voltage Fast SCSI-2 Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Functionally compatible with Emulex FAS216 and NCR 53CF94
- Supports Low-Voltage operation at 3.3 V. Conforms to JEDEC baseline specifications
- AMD patented GLITCH EATER™ circuitry
- 10 MB per second SCSI transfer rate
- 20 MB per second DMA transfer rate
- 16-bit DMA Interface plus 2 bits of parity
- Flexible bus architecture, supports a three bus architecture
- Supports single ended SCSI bus
- Selection of multiplexed or non-multiplexed address and data bus
- High current drivers (48 mA) for direct connection to the single ended SCSI bus
- Supports Disconnect and Reselect commands
- Supports burst mode DMA operation with a threshold of 8
- Supports 3 byte tagged queuing as per the SCSI-2 specification
- Supports group 2 and 5 command recognition as per the SCSI-2 specification
- Advanced CMOS process for low power consumption
- Am53CF94LV available in 100-pin PQFP package

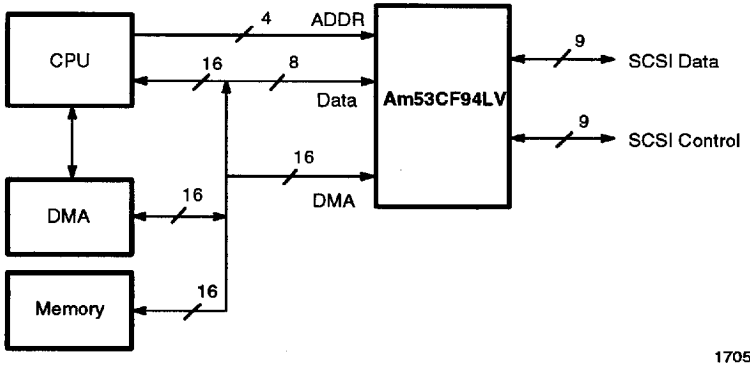
GENERAL DESCRIPTION

The Low Voltage Fast SCSI-2 Controller (LVFSC) has a flexible three bus architecture. The LVFSC has a 16 bit DMA interface, an 8 bit host data interface and an 8 bit SCSI data interface. The LVFSC is designed to minimize host intervention by implementing common SCSI sequences in hardware. An on-chip state machine reduces protocol overheads by performing the required sequences in response to a single command from the host. Selection, Reselection, Information Transfer and Disconnection commands are directly supported.

The 16 byte internal FIFO further assists in minimizing host involvement. The FIFO provides a temporary storage for all command, data, status and message bytes as they are transferred between the 16 bit host data bus and the 8 bit SCSI data bus. During DMA operations the FIFO acts as a buffer to allow greater latency in the DMA channel. This permits the DMA channel to be suspended for higher priority operations such as DRAM refresh or reception of an ISDN packet.

Parity on the DMA bus is optional. Parity can either be generated and checked or it can be simply passed through.

SYSTEM BLOCK DIAGRAM



17059A-001A

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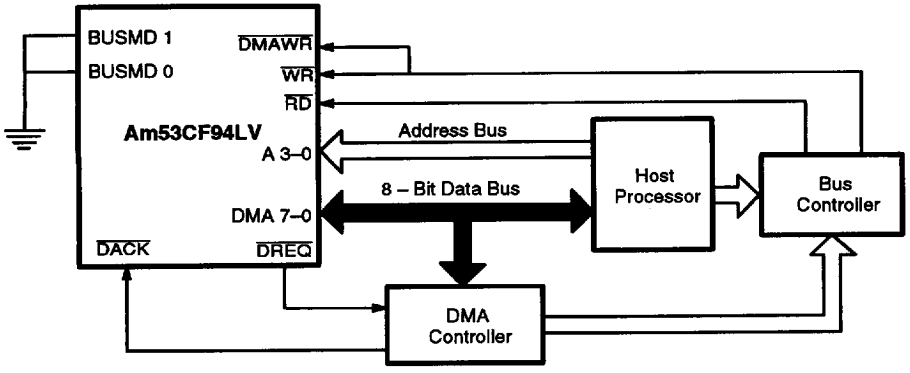
SYSTEM BUS MODE DIAGRAMS



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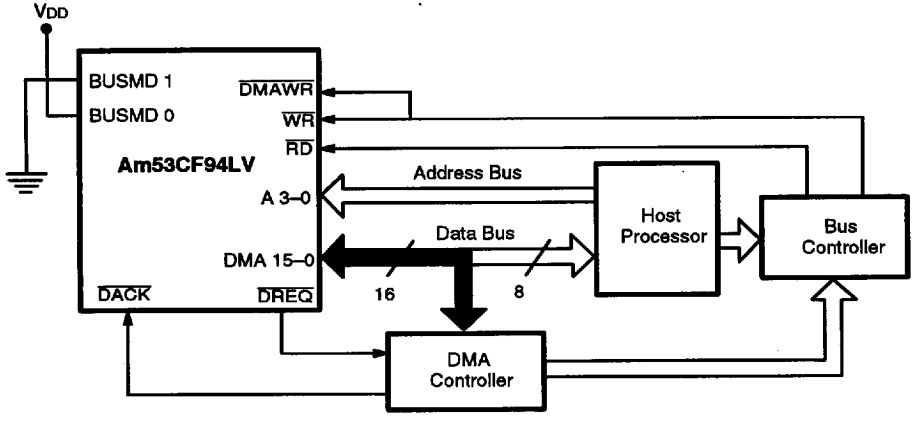
Bus Mode 0



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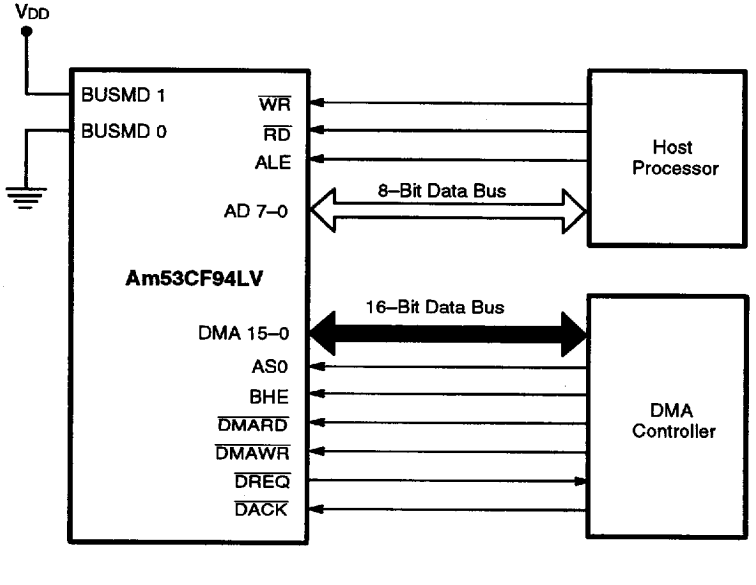
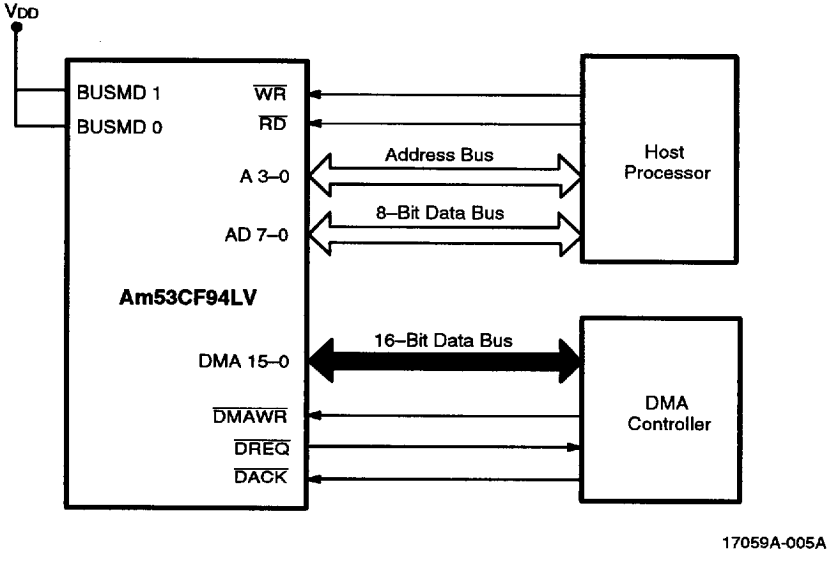
Bus Mode 1

SYSTEM BUS MODE DIAGRAMS

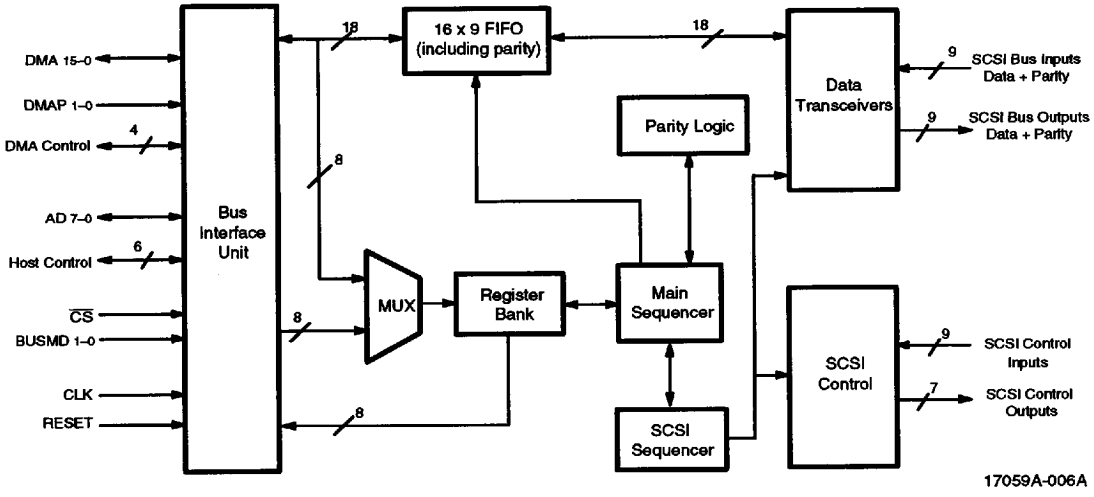


Bus Mode 2



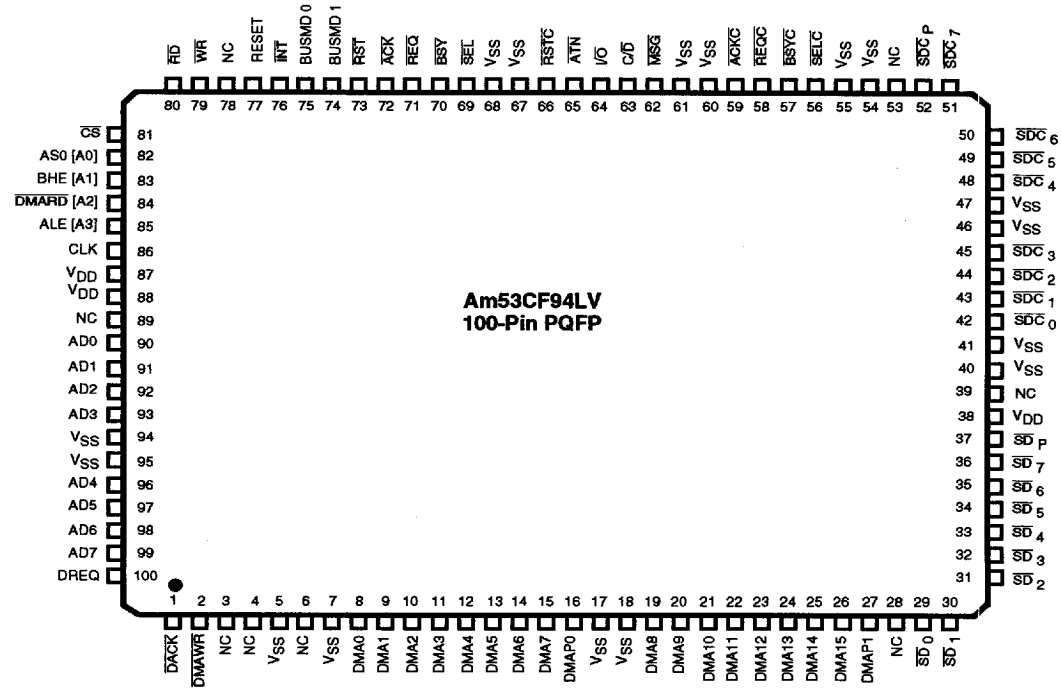
Bus Mode 3

BLOCK DIAGRAM



CONNECTION DIAGRAM
Am53CF94LV (Top View)

PQFP

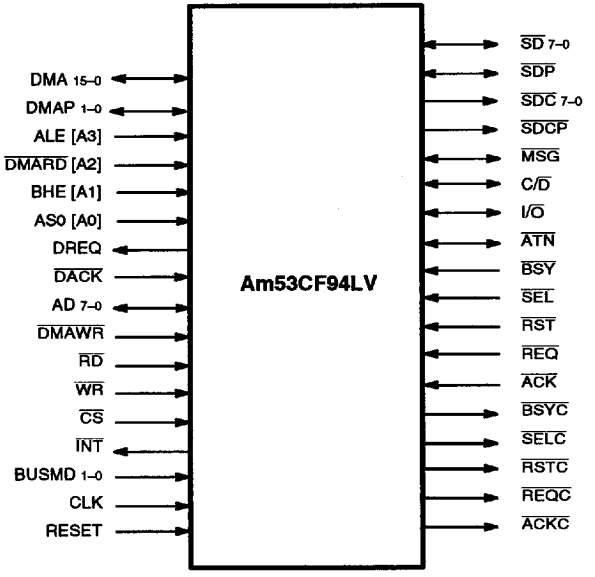


17059A-007A

RELATED AMD PRODUCTS

Part Number	Description
Am53C80A	4 MBytes/sec Asynchronous CMOS SCSI Controller
Am33C93A	5 MBytes/sec Async/Synchronous CMOS SCSI Controller
Am85C80	Combination SCSI Controller (Am53C80A) and ESCC (Am85C30)
Am85C30	Enhanced Serial Communications Controller (ESCC)
Am53C94	High-Performance CMOS SCSI Controller (Single-Ended)
Am53C96	High-Performance CMOS SCSI Controller (Single-Ended and Differential)
Am53C94LV	Low-Voltage High-Performance SCSI Controller
Am53CF94	CMOS Fast SCSI-2 Controller (Single-Ended)
Am53CF96	CMOS Fast SCSI-2 Controller (Single-Ended and Differential)

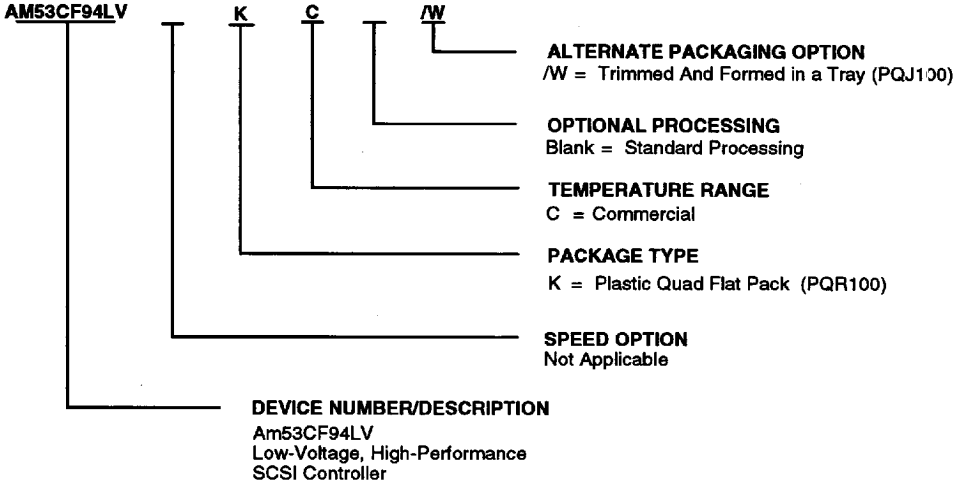
LOGIC SYMBOL



17059A-008A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM53CF94LV	KC, KC/W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Host Interface Signals

DMA 15-0
Data/DMA Bus (Input/Output, Active High, Internal Pullup)

The configuration of this bus depends on the Bus Mode 1-0 (BUSMD 1-0) inputs. When the device is configured for single bus operation, the host can access the internal register set on the lower eight lines and the DMA accesses can be made to the FIFO using the entire bus. When using the Byte Mode via the BHE and A0 inputs the data can be transferred on either the upper or lower half of the DMA 15-0 bus.

DMAP 1-0
Data/DMA Parity Bus (Input/Output, Active High, Internal Pullup)

These lines are odd parity for the DMA 15-0 bus. DMAP 1 is the parity for the upper half of the bus (DMA 15-8) and DMAP 0 is the parity for the lower half of the bus (DMA 7-0).

ALE [A3]
Address Latch Enable [Address 3] (Input, Active High)

This is a dual function input. When the device is configured for single bus operation this input acts as ALE. As ALE, this input latches the address on the AD 7-0 bus on its Low going edge. When the device is configured for dual bus operation this input acts as A3. As A3, this input is the third bit of the address bus.

$\overline{\text{DMARD}}$ [A2]
DMA Read [Address 2] (Input, Active Low [Active High])

This is a dual function input. When the device is configured for single bus operation this input acts as $\overline{\text{DMARD}}$. As $\overline{\text{DMARD}}$, this input is the read signal for the DMA 15-0 bus. When the device is configured for dual bus operation this input acts as A2. As A2, this input is the second bit of the address bus.

BHE [A1]
Bus High Enable [Address 1] (Input, Active High)

This is a dual function input. When the device is configured for single bus operation this input acts as BHE. As BHE, this input along with AS0 indicates on which lines the data transfer is to take place. When the device is configured for dual bus operation this input acts as A1. As A1, this input is the first bit of the address bus.

The following is the decoding for the BHE and AS0 inputs:

BHE	AS0	Bus Used
1	1	Upper Bus – DMA 15-8, DMAP 1
1	0	Full Bus – DMA 15-0, DMAP 1-0
0	1	Reserved
0	0	Lower Bus – DMA 7-0, DMAP 0

AS0 [A0]
Address Status [Address 0] (Input, Active High)

This is a dual function input. When the device is configured for single bus operation this input acts as AS0. As AS0, this input along with BHE indicates on which lines the data transfer is to take place. When the device is configured for dual bus operation this input acts as A0. As A0, this input is the zeroth bit of the address bus.

DREQ
DMA Request (Output, Active High, Three-State)

This output signal to the DMA controller will be active during DMA read and write cycles. During a DMA read cycle it will be active as long as there is a word (or a byte in the byte mode) in the FIFO to be transferred to memory. During a DMA write cycle it will be active as long as there is an empty space for a word (or a byte in the byte mode) in the FIFO.

$\overline{\text{DACK}}$
DMA Acknowledge (Input, Active Low)

This input signal from the DMA controller will be active during DMA read and write cycles. The $\overline{\text{DACK}}$ signal is used to access the DMA FIFO only and should never be active simultaneously with the $\overline{\text{CS}}$ signal, which accesses the registers only.

AD 7-0
Host Address Data Bus (Input/Output, Active High, Internal Pullup)

This bus is used only in the dual bus mode. This bus allows the host processor to access the device's internal registers while the DMA bus is transferring data. When using the multiplexed bus mode, these lines can be used for address and data. When using a non-multiplexed bus mode these lines can be used for the data only.

$\overline{\text{DMAWR}}$
DMA Write (Input, Active Low)

This signal writes the data on the DMA 15-0 bus into the internal FIFO when DACK is also active. When in the single bus mode this signal must be tied to the WR signal.

$\overline{RD}$
Read (Input, Active Low)

This signal reads the internal device registers and places their contents on the data bus, when either $\overline{CS}$ signal or $\overline{DACK}$ signal is active.

$\overline{WR}$
Write (Input, Active Low)

This signal writes the internal device registers with the value present on the data bus, when the $\overline{CS}$ signal is also active.

$\overline{CS}$
Chip Select (Input, Active Low)

This signal enables the read and write of the device registers. $\overline{CS}$ enables access to any register (including the FIFO) while the $\overline{DACK}$ enables access only to the FIFO. $\overline{CS}$ and $\overline{DACK}$ should never be active simultaneously in the single bus mode, they may however be active simultaneously in the dual bus mode provided the $\overline{CS}$ signal is not enabling access to the FIFO.

$\overline{INT}$
Interrupt (Output, Active Low, Open Drain)

This signal is a non-maskable interrupt flag to the host processor. This signal is latched on the output on the high going edge of the clock. This flag may be cleared by reading the Interrupt Status Register (ISTAT) or by performing a device reset (hard or soft). This flag is not cleared by a SCSI reset.

BUSMD 1-0
Bus Mode (Input, Active High)

These inputs configure the device for single bus or dual bus operation and the DMA width.

BUSMD1	BUSMD0	Bus Configuration
1	1	Two buses: 8-bit Host Bus & 16-bit DMA Bus Register Address on A 3-0 & Data on AD Bus
1	0	Two buses: Multiplexed & byte control Register Address on AD 3-0 & Data on AD Bus
0	1	Single bus: 8-bit Host Bus & 16-bit DMA Bus Register Address on A 3-0 & Data on DMA Bus
0	0	Single bus: 8-bit Host Bus & 8-bit DMA Bus Register Address on A 3-0 & Data on DMA Bus

CLK
Clock (Input)

Clock input used to generate all the internal clevice timings. The maximum frequency of this input is 25 MHz. A minimum of 10MHz is required to maintain the SCSI bus timings.

RESET
Reset (Input, Active High)

This input when active resets the device. The RESET input must be active for at least two CLK periods after the voltage on the power inputs has reached Vcc minimum.

SCSI Interface Signals

$\overline{SD}$ 7-0
SCSI Data (Input, Active Low, Schmitt Trigger)

These are SCSI data input pins.

$\overline{SDP}$
SCSI Data Parity (Input, Active Low, Schmitt Trigger)

This is the SCSI data parity input pin.

$\overline{SDC}$ 7-0
SCSI Data Control (Output, Active Low, Open Drain)

These are SCSI data output pins.

$\overline{SDCP}$
SCSI Data Control Parity (Output, Active Low, Open Drain)

This is the SCSI data parity output pin.

$\overline{MSG}$
Message (Input/Output, Active Low, Schmitt Trigger)

This is a bidirectional signal with a 48 mA output driver. It is an output in the target mode and a Schrnitt trigger input in the initiator mode.

C/$\overline{D}$
Command/Data (Input/Output, Schmitt Trigger)

This is a bidirectional signal with a 48 mA output driver. It is an output in the target mode and a Schrnitt trigger input in the initiator mode.

I/$\overline{O}$
Input/Output (Input/Output, Schmitt Trigger)

This is a bidirectional signal with a 48 mA output driver. It is an output in the target mode and a Schrnitt trigger input in the initiator mode.

$\overline{\text{ATN}}$
Attention (Input/Output, Active Low, Schmitt Trigger)

This signal is a 48 mA output in the initiator mode and a Schmitt trigger input in the target mode. This signal will be asserted when the device detects a parity error or it can be asserted via certain commands. In the target mode this pin is an input.

$\overline{\text{BSY}}$
Busy (Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{SEL}}$
Select (Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{RST}}$
Reset (Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{REQ}}$
Request (Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{ACK}}$
Acknowledge (Input, Active Low, Schmitt Trigger). This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{BSYC}}$
Busy Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. This pin is the $\overline{\text{BSY}}$ output for the SCSI bus.

$\overline{\text{SELC}}$
Select Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. When the device is configured in the Single-Ended SCSI Mode ($\overline{\text{DFMODE}}$ inactive), this pin is the $\overline{\text{SEL}}$ output for the SCSI bus.

$\overline{\text{RSTC}}$
Reset Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. The Reset SCSI command will cause the device to drive $\overline{\text{RSTC}}$ active for 25–40 microseconds, which will depend on the CLK frequency and the conversion factor. This pin is the $\overline{\text{RST}}$ output for the SCSI bus.

$\overline{\text{REQC}}$
Request Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. This signal is asserted only in the target mode.

$\overline{\text{ACKC}}$
Acknowledge Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. This signal is asserted only in the initiator mode.

FUNCTIONAL DESCRIPTION

Register Map

Address (Hex.)	Operation	Register
00	Read	Current Transfer Count Register LSB
00	Write	Start Transfer Count Register LSB
01	Read	Current Transfer Count Register MSB
01	Write	Start Transfer Count Register MSB
02	Read/Write	FIFO Register
03	Read/Write	Command Register
04	Read	Status Register
04	Write	SCSI Destination ID Register
05	Read	Interrupt Status Register
05	Write	SCSI Timeout Register
06	Read	Internal State Register
06	Write	Synchronous Transfer Period Register
07	Read	Current FIFO Internal State Register
07	Write	Synchronous Offset Register
08	Read/Write	Control Register 1
09	Write	Clock Factor Register
0A	Write	Forced Test Mode Register
0B	Read/Write	Control Register 2
0C	Read/Write	Control Register 3 Rev. ID Register
0F	Write	Data Alignment Register

Not all registers in this device are both readable and writable. Some read only registers share the same address with write only registers. The registers can be accessed by asserting the $\overline{CS}$ signal and then asserting either $\overline{RD}$ or $\overline{WR}$ signal depending on the operation to be performed. Only the FIFO Register can be accessed by asserting either $\overline{CS}$ or $\overline{DACK}$ in conjunction with $\overline{RD}$ and $\overline{WR}$ signals or $\overline{DMARD}$ and $\overline{DMAWR}$ signals. The register address inputs are ignored when $\overline{DACK}$ is used but must be valid when $\overline{CS}$ is used.

COMMANDS

The device commands can be broadly divided into two categories, DMA commands and non-DMA commands. DMA commands are those which cause data movement between the host memory and the SCSI bus while non-DMA commands are those that cause data movement between the device FIFO and the SCSI bus. The MSB of the command byte differentiates DMA commands from non-DMA commands.

Summary of Commands

Command	Command Code (Hex.)	
	Non-DMA Mode	DMA Mode
Initiator Commands		
Information Transfer	10	90
Initiator Command Complete Steps	11	91
Message Accepted	12	-
Transfer Pad Bytes	18	98
Set $\overline{\text{ATN}}$	1A	-
Reset $\overline{\text{ATN}}$	1B	-
Target Commands		
Send Message	20	A0
Send Status	21	A1
Send Data	22	A2
Disconnect Steps	23	A3
Terminate Steps	24	A4
Target Command Complete Steps	25	A5
Disconnect	27	A7
Receive Message	28	A8
Receive Command Steps	29	A9
Receive Data	2A	AA
Receive Command Steps	2B	AB
Target Abort DMA	04	84

Command	Command Code (Hex.)	
	Non-DMA Mode	DMA Mode
Idle State Commands		
Reselect Steps	40	C0
Select without $\overline{\text{ATN}}$ Steps	41	C1
Select with $\overline{\text{ATN}}$ Steps	42	C2
Select with $\overline{\text{ATN}}$ and Stop Steps	43	C3
Enable Selection/Reselection	44	C4
Disable Selection/Reselection		45
Select with $\overline{\text{ATN3}}$	46	C6
General Commands		
No Operation	00	80
Clear FIFO	01	81
Reset Device	02	82
Reset SCSI bus	03	83

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –55 to +125°C
Ambient Operating Temperature . . . . . 0 to +70°C
Maximum V_{CC} . . . . . –0.5 to +7.0 V
DC Voltage Applied to Any Pin . –0.5 to (V_{DD} + 0.3) V
Input Static Discharge Protection . . 3000 V pin to pin
(Human body model: 100 pF at 1.5 KΩ)

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0 to +70°C
Supply Voltage (V_{DD}) . . . . . 3.3 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC OPERATING CHARACTERISTICS V_{DD}=2.9 V to 3.7 V; T_{CASE} = 0° to + 100°

Parameter Symbol	Parameter Description	Pin Names	Test Condition	Min.	Max.	Unit
I_{CCS}	Static Supply Current				4.0	mA
I_{CCD}	Dynamic Supply Current				50	mA
I_{LU}	Latch Up Current			–100	+100	mA
SCSI Pins						
V_{IH}	Input High Voltage	All SCSI Inputs		2.0	V_{DD} +0.3	V
V_{IL}	Input Low Voltage	All SCSI Inputs		–0.3	0.8	V
V_{IHST}	Input Hysterisis	All SCSI Inputs	2.9 V < V_{DD} < 3.7 V	200		mV
V_{OH}	Output High Voltage	SD 7–0, SDP				
V_{SOL1}	SCSI Output Low Voltage	SD 7–0, SDP	I_{OL}= 4 mA	V_{SS}	0.4	V
V_{SOL2}	SCSI Output Low Voltage	SDC 7–0, SDCP, MSG, C/D, I/O, ATN, RSTC, SELC, BSYC, ACKC and REQC	I_{OL}= 48 mA	V_{SS}	0.5	V
I_{LI}	Input Leakage		0.0 V ≤ V_{IN} ≤ V_{DD}	–10	+10	µA
I_{LO}	Output Leakage		0.1 V ≤ V_{OUT} ≤ V_{DD}	–10	+10	µA
Bidirectional Pins						
V_{IH}	Input High Voltage			2.0	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			–0.3	0.8	V
V_{OH}	Output High Voltage	DMA 15–0, DMAP 1–0 and AD 7–0				
V_{OL}	Output Low Voltage	DMA 15–0, DMAP 1–0 and AD 7–0	I_{OL}= 0.5 mA	V_{SS}	0.2	V
			I_{OL}= 2 mA		0.45	V
I_{LI}	Input Leakage	DMA 15–0, DMAP 1–0 and AD 7–0	0.0 V ≤ V_{IN} ≤ V_{DD}		±15	µA
I_{LO}	Output Leakage	DMA 15–0, DMAP 1–0 and AD 7–0	0.1 V ≤ V_{OUT} ≤ V_{DD}		±15	µA
Output Pins						
V_{OH}	Output High Voltage	DRQ and INT				
V_{OL}	Output Low Voltage	DRQ and INT	I_{OL}= 0.5 mA		0.2	V
			I_{OL}= 2.5 mA		0.45	V