

16,384-word × 4-bit High Speed CMOS Static RAM

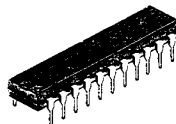
Description

CXK5464AP/AJ are 65,536 bits high speed CMOS static RAMs organized as 16,384 words by 4 bits and operate from a single 5V supply.

Features

- Fast access time :
CXK5464AP/AJ-25 25ns (Max.)
CXK5464AP/AJ-30 30ns (Max.)
CXK5464AP/AJ-35 35ns (Max.)
- Low power operation : 125mW (Typ.)
- Single + 5V supply : + 5V ± 10 %
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : Three-state output
- Directly TTL compatible : All inputs and outputs.
- High density : 300mil 22 pin plastic DIP
300mil 24 pin plastic SOJ

CXK5464AP
22 pin DIP (Plastic)



CXK5464AJ
24 pin SOJ (Plastic)



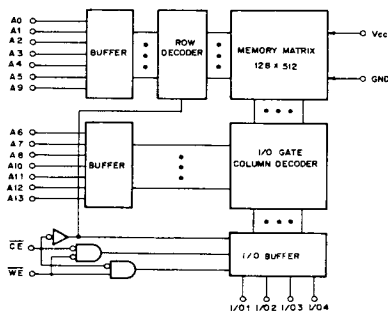
Function

16,384-word × 4-bit static RAM

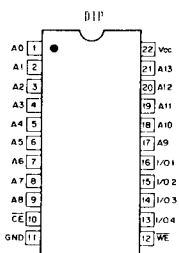
Structure

Silicon gate CMOS IC

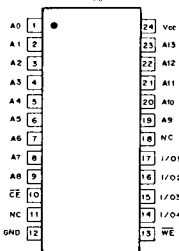
Block Diagram



Pin Configuration (Top view)



SOJ



Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input output
CE	Chip enable input
WE	Write enable input
Vcc	+ 5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 * to + 7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5 * to V _{CC} + 0.5	V
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature	T _{solder}	260 ± 10	°C • sec
Allowable power dissipation	P _D	1.0	W

* V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.**Truth Table**

CE	WE	Mode	I/O1 to I/O4	V _{CC} Current
H	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	Read	Data out	I _{CC1} , I _{CC2}
L	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.* ¹	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3* ²	—	0.8	V

* 1. V_{CC} = 5V, Ta = 25°C* 2. V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics**●DC and operating characteristics** ($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$)

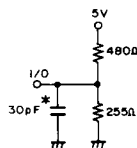
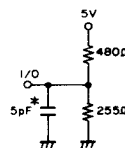
Item	Symbol	Test conditions	- 25/30/35			Unit
			Min.	Typ.*	Max.	
Input leak current	I_{LI}	$V_{IN} = GND$ to V_{CC}	- 1	—	1	μA
Output leak current	I_{LO}	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = GND$ to V_{CC}	- 1	—	1	μA
Operating supply current	I_{CC1}	$\overline{CE} = V_{IL}$, $I_{OUT} = 0mA$ $V_{IN} = V_{IH}/V_{IL}$	—	25	45	mA
Average operating current	I_{CC2}	Cycle = Min., Duty = 100 % $I_{OUT} = 0mA$	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	—	1	mA
	I_{SB2}	$\overline{CE} = V_{IH}$	—	15	30	mA
Output high voltage	V_{OH}	$I_{OH} = - 4.0mA$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$	—	—	0.4	V

* $V_{CC} = 5.0V$, $T_a = 25^\circ C$ **I/O capacitance**($T_a = 25^\circ C$, $f = 1MHz$)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

Note) This parameter is sampled and is not 100% tested.**AC characteristics****●AC test conditions**($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$)

Item	Conditions
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)**Output Load (2)****

* including scope and jig

** for t_{LZ} , t_{HZ} , t_{OW} , t_{WHZ} **Fig. 1**

● Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time (CE)	t _{CO}	—	25	—	30	—	35	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t _{LZ} *	5	—	5	—	5	—	ns
Chip disable to output in high Z	t _{HZ} *	0	10	0	15	0	15	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip enable to power down time	t _{PD}	—	20	—	25	—	25	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.

This parameter is sampled and is not 100% tested.

● Write cycle

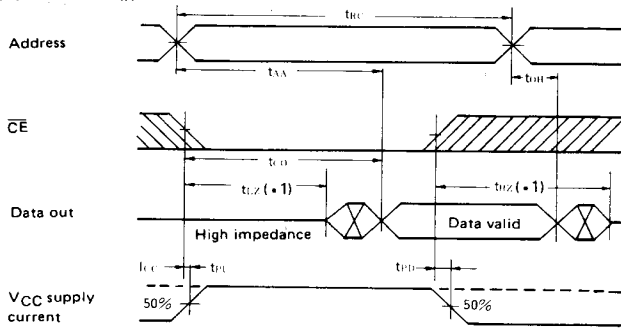
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	15	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	25	—	30	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	10	0	10	0	15	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.

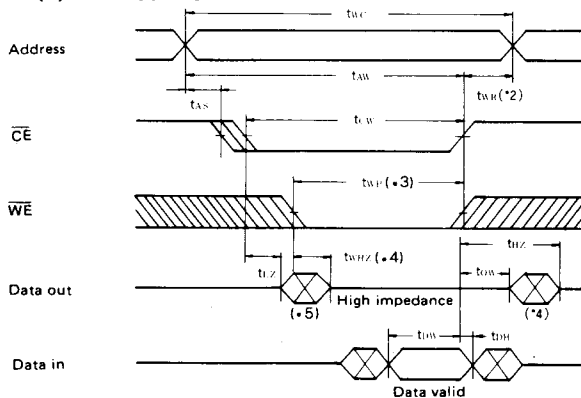
This parameter is sampled and is not 100% tested.

Timing Waveform

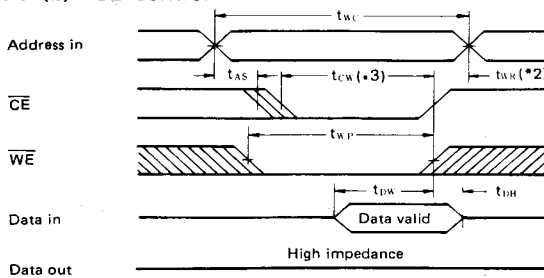
• Read cycle : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control

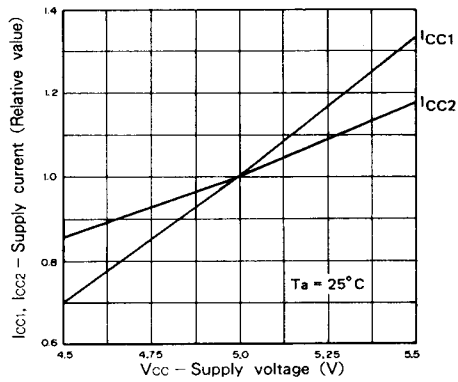


*Note)

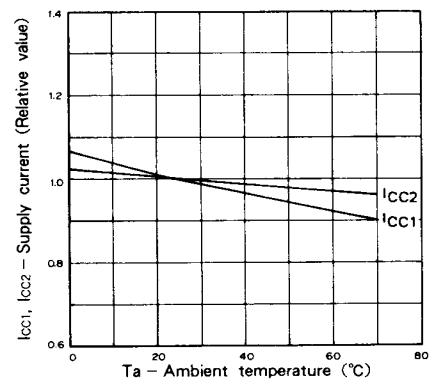
1. At any conditions, t_{HZ} is less than t_{LZ} .
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
4. If $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
5. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Example of Representative Characteristics

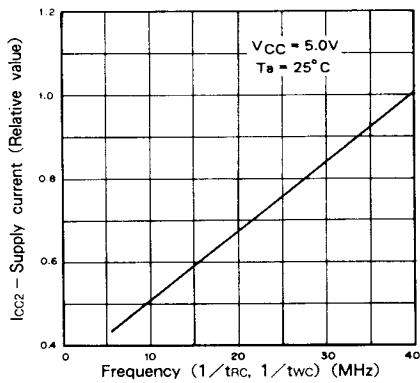
Supply current vs. Supply voltage



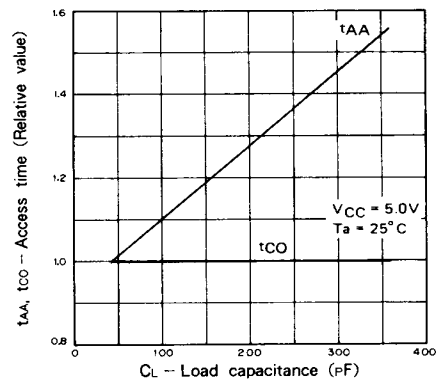
Supply current vs. Ambient temperature



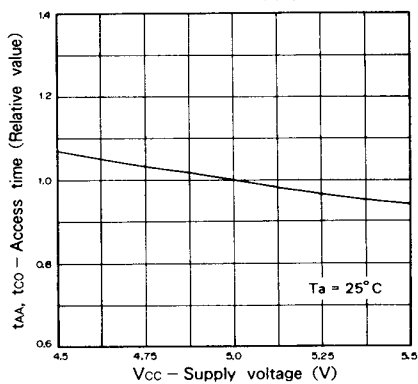
Supply current vs. Frequency



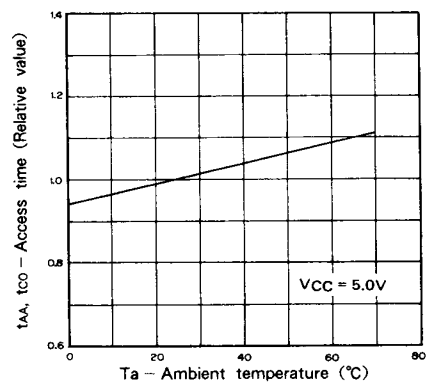
Access time vs. Load capacitance



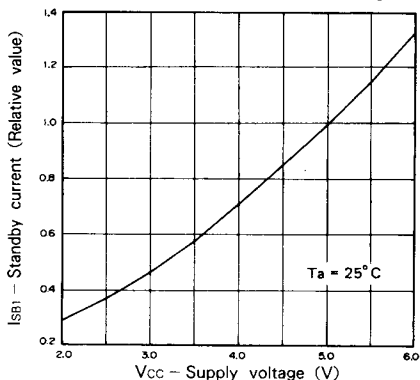
Access time vs. Supply voltage



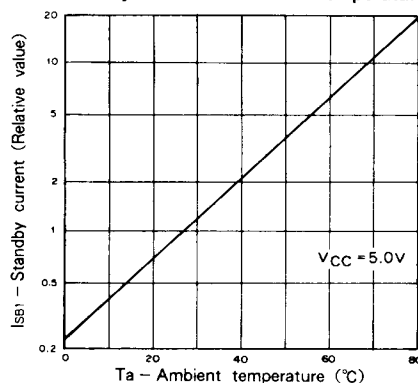
Access time vs. Ambient temperature



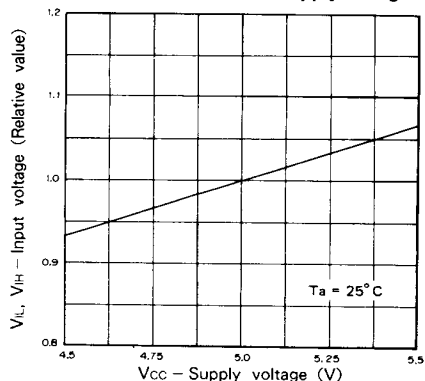
Standby current vs. Supply voltage



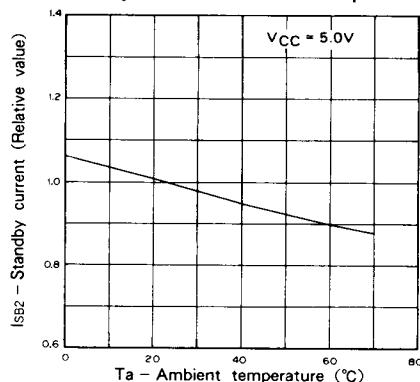
Standby current vs. Ambient temperature



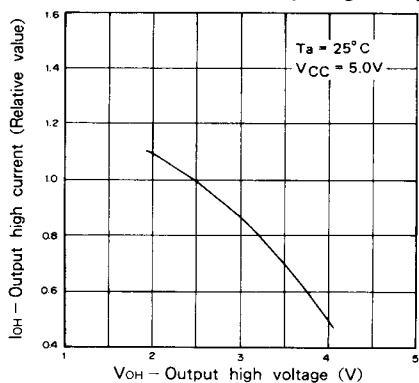
Input voltage level vs. Supply voltage



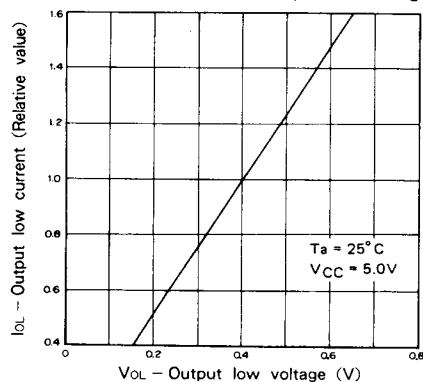
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

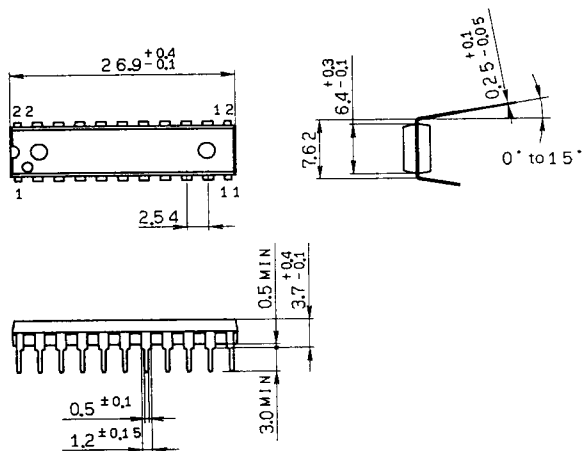


Output low current vs. Output low voltage



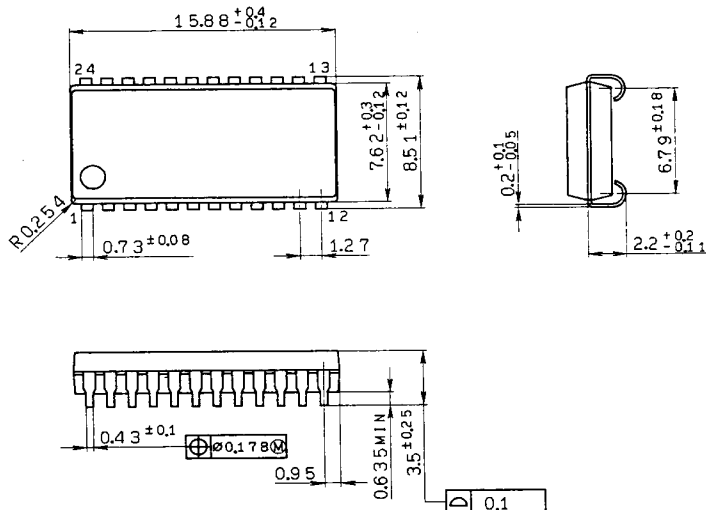
Package Outline Unit : mm

CXK5464AP 22 pin DIP (Plastic) 300mil 1.3g



DIP-22P-02

CXK5464AJ 24 pin SOJ (Plastic) 300mil 0.7g



SOJ-24P-01