

DALLAS
SEMICONDUCTOR

DS1643AL

Nonvolatile Timekeeping RAM

FEATURES

- Integrated NV SRAM, real time clock, crystal, power-fail control circuit and lithium energy source
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 120 ns and 150 ns
- Quartz accuracy ± 1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds with leap year compensation valid up to 2100
- Power-fail write protection allows for $\pm 10\%$ V_{CC} power supply tolerance
- Low Profile socketable module
 - 255 mil package height

ORDERING INFORMATION

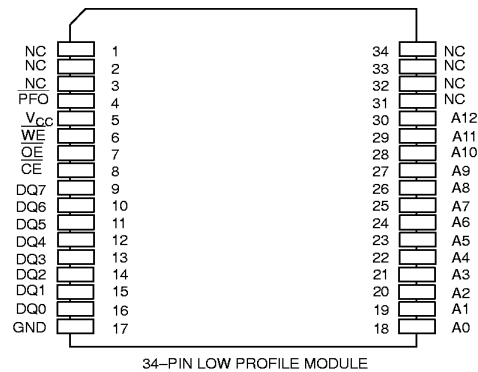
DS1643AL-XX 34-pin low profile module

-12 = 120 ns access
 -15 = 150 ns access

DESCRIPTION

The DS1643AL is an 8K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a byte-wide format. The nonvolatile time keeping RAM is functionally equivalent to any JEDEC standard 8K x 8 SRAM. The DS1643AL is a Low Profile Module that requires a PLCC surface mountable socket and, except for the additional Power Fail Output (PFO) signal, is functionally equivalent to the DS1643. The Real Time Clock (RTC) information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and

PIN ASSIGNMENT



leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1643AL also contains its own power-fail circuitry which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

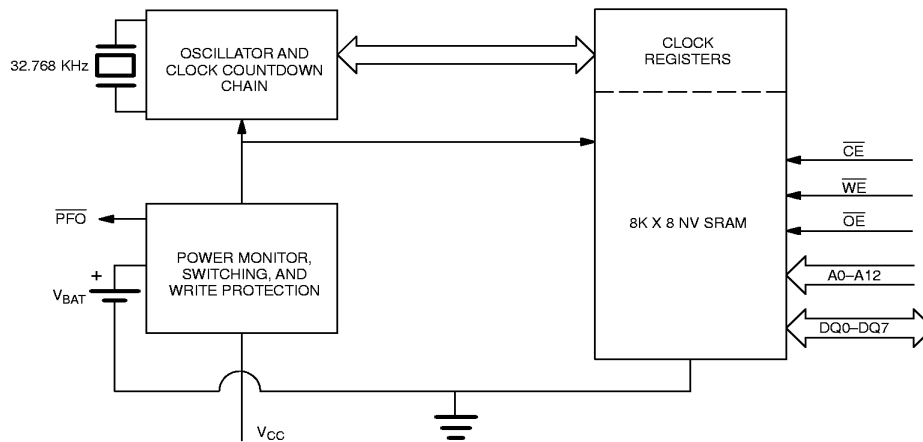
PIN DESCRIPTION

A0–A12	– Address Input
$\overline{CE}$	– Chip Enable
$\overline{OE}$	– Output Enable
$\overline{WE}$	– Write Enable
NC	– No Connection
V _{CC}	– +5 Volts
GND	– Ground
DQ0–DQ7	– Data Input/Output
$\overline{PFO}$	– Power–Fail Output

CLOCK OPERATIONS—READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the

DS1643AL clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when an one is written into the read bit, the seventh most significant bit in the control register. As long as a one remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1643AL registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

DS1643 BLOCK DIAGRAM Figure 1

DS1643AL TRUTH TABLE Table 1

V _{CC}	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS $\pm$ 10%	V _{IH}	X	X	X	DESELECT	HIGH-Z	STANDBY
	X	V _{IL}	X	X	DESELECT	HIGH-Z	STANDBY
	V _{IL}	V _{IH}	X	V _{IL}	WRITE	DATA IN	ACTIVE
	V _{IL}	V _{IH}	V _{IL}	V _{IH}	READ	DATA OUT	ACTIVE
	V _{IL}	V _{IH}	V _{IH}	V _{IH}	READ	HIGH-Z	ACTIVE
<4.5 VOLTS >V _{BAT}	X	X	X	X	DESELECT	HIGH-Z	CMOS STANDBY
<V _{BAT}	X	X	X	X	DESELECT	HIGH-Z	DATA RETENTION MODE

SETTING THE CLOCK

Bit 8 of the control register is the write bit. Setting the write bit to a one, like the read bit, halts updates to the DS1643AL registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a zero then transfers those values to the actual clock counters and allows normal operation to resume.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a one stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is

running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, and address for seconds register remain valid and stable).

CLOCK ACCURACY

The DS1643AL is guaranteed to keep time accuracy to within ± 1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1643AL does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T08 family) will not have any effect even though the DS1643AL appears to accept calibration data.



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	−0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	−20°C to +70°C
Soldering Temperature	260°C for 10 seconds (See Note 7)

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		$V_{CC}+0.3$	V	
Logic 0 Voltage All Inputs	V_{IL}	−0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS(0°C ≤ t_A ≤ 70°C; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}			65	mA	2, 3
TTL Standby Current ($\overline{CE} = V_{IH}$)	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE} = V_{CC}-0.2V$)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (any input)	I_{IL}	−1		+1	μA	
Output Leakage Current	I_{OL}	−1		+1	μA	
Output Logic 1 Voltage ($I_{OUT} = -1.0$ mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage ($I_{OUT} = +2.1$ mA)	V_{OL}			0.4	V	
Write Protection Voltage	V_{PF}	4.0	4.25	4.5	V	



AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1643AL-12 120 ns Access		DS1643AL-15 150 ns Access		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t _{RC}	120		150		ns	
Address Access Time	t _{AA}		120		150	ns	
$\overline{\text{CE}}$ Access Time	t _{CEA}		120		150	ns	
$\overline{\text{CE}}$ Data Off Time	t _{CEZ}		40		50	ns	
Output Enable Access Time	t _{OEa}		100		120	ns	
Output Enable Data Off Time	t _{OEZ}		35		45	ns	
Output Enable to DQ Low-Z	t _{OEL}	5		5		ns	
$\overline{\text{CE}}$ to DQ Low-Z	t _{CEL}	5		5		ns	
Output Hold from Address	t _{OH}	5		5		ns	
Write Cycle Time	t _{WC}	120		150		ns	
Address Setup Time	t _{AS}	0		0		ns	
$\overline{\text{CE}}$ Pulse Width	t _{CEW}	100		120		ns	
Address Hold from End of Write	t _{AH1}	5		5		ns	5
	t _{AH2}	30		30		ns	6
Write Pulse Width	t _{WEW}	75		90		ns	
$\overline{\text{WE}}$ Data Off Time	t _{WEZ}		40		50	ns	
$\overline{\text{WE}}$ or $\overline{\text{CE}}$ Inactive Time	t _{WR}	10		10		ns	
Data Setup Time	t _{DS}	85		110		ns	
Data Hold Time High	t _{DH1}	0		0		ns	5
	t _{DH2}	15		15		ns	6

AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5 ns

CAPACITANCE (t_A = 25°C)

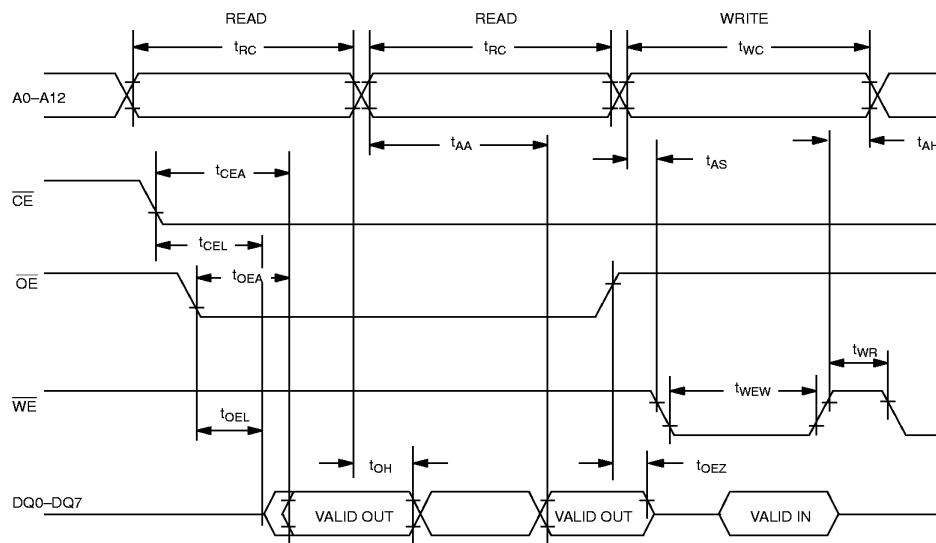
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C _I			7	pF	
Capacitance on DQ pins	C _{DQ}			10	pF	

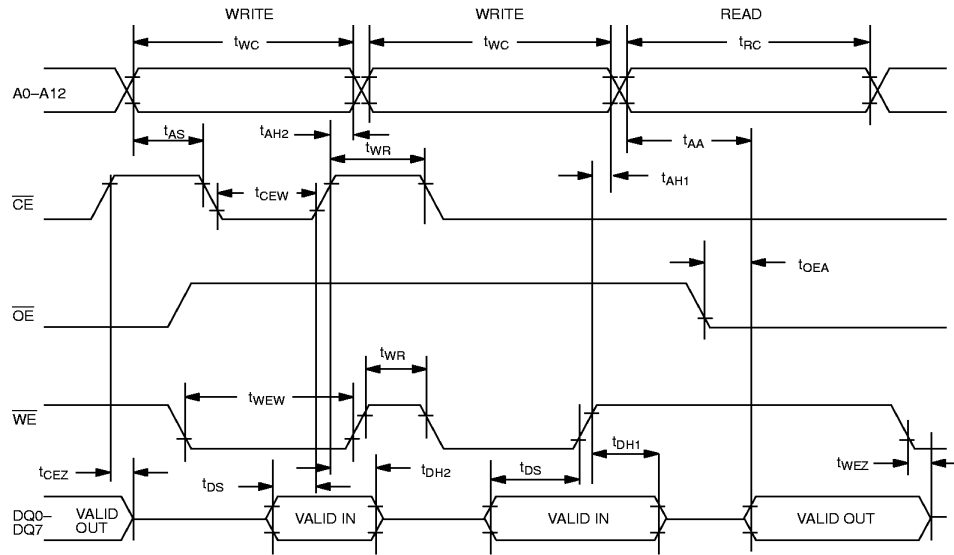
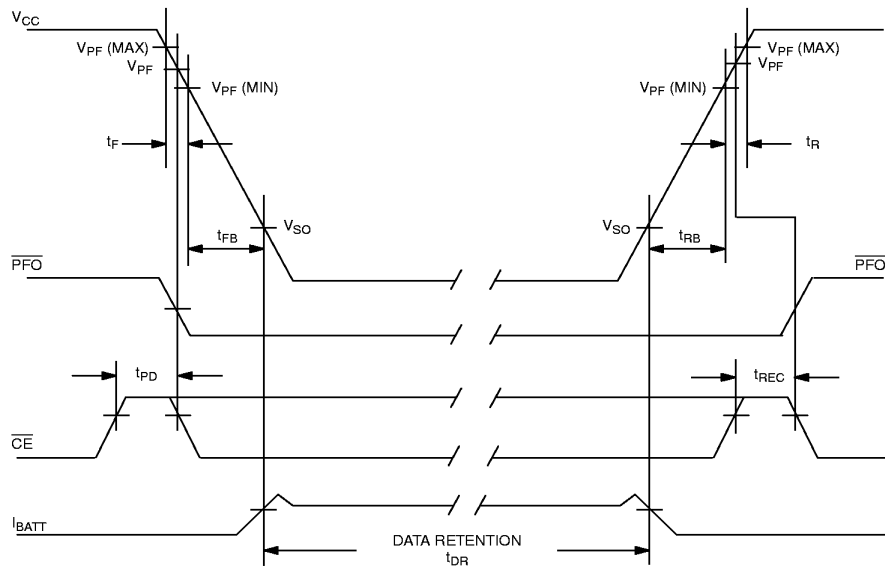


AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING)

(0°C to 70°C)

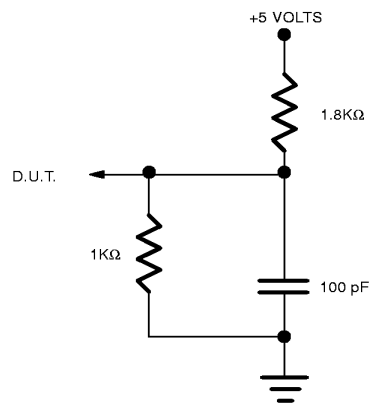
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{CE}}$ or $\overline{\text{WE}}$ at V_{IH} before Power Down	t_{PD}	0			μs	
$V_{PF}(\text{Max})$ to $V_{PF}(\text{Min})$ V_{CC} Fall Time	t_F	300			μs	
$V_{PF}(\text{Min})$ to V_{SO} V_{CC} Fall Time	t_{FB}	10			μs	
V_{SO} to $V_{PF}(\text{Min})$ V_{CC} Rise Time	t_{RB}	1			μs	
$V_{PF}(\text{Min})$ to $V_{PF}(\text{Max})$ V_{CC} Rise Time	t_R	0			μs	
Power-Up	t_{REC}	15	25	35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

DS1643AL READ CYCLE TIMING

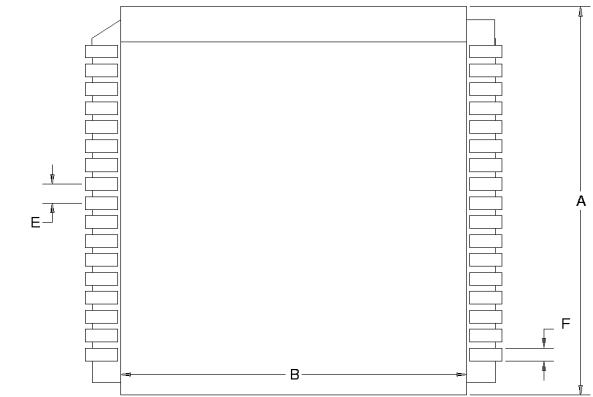
DS1643AL WRITE CYCLE TIMING**POWER-DOWN/POWER-UP TIMING**

NOTES:

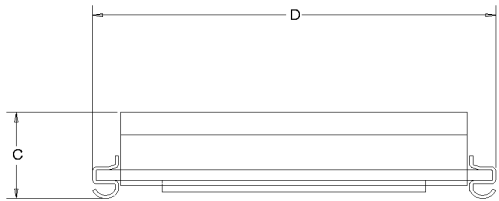
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Data retention time is at 25°C and is calculated from the date code on the device package. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.
5. t_{AH1} , t_{DH1} are measured from $\overline{WE}$ going high.
6. t_{AH2} , t_{DH2} are measured from $\overline{CE}$ going high.
7. Unencapsulated Low Profile Modules are not recommended for processing through conventional wavesoldering techniques. The use of a PLCC socket is recommended for production proposes.

OUTPUT LOAD

DS1643AL 34-PIN LOW PROFILE MODULE

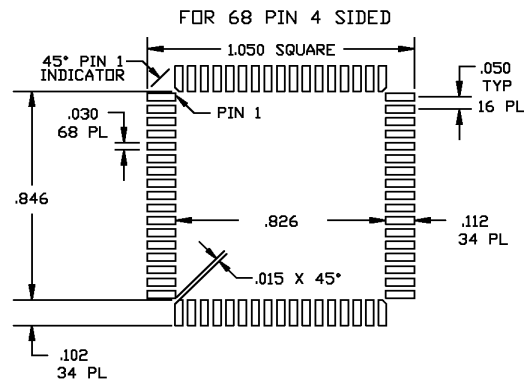


PKG	INCHES	
	DIM	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



NOTE:
Dallas Semiconductor recommends the AMP PLCC socket, P/N 822453-1, Revision A (date code 9810 or later), for use with our 34-pin LPM device.



RECOMMENDED DS1643AL MODULE SOCKET LAND PATTERNS

EITHER A TWO OR FOUR SIDED SOCKET MAY BE UTILIZED FOR DS1643AL INSTALLATION.

