

GSS4501S

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

N-CH BV_{DSS}	30V
$R_{DS(ON)}$	33m Ω
I_D	6A
P-CH BV_{DSS}	-30V
$R_{DS(ON)}$	50m Ω
I_D	-5.3A

Description

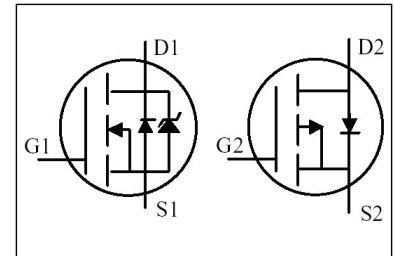
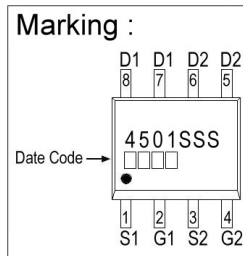
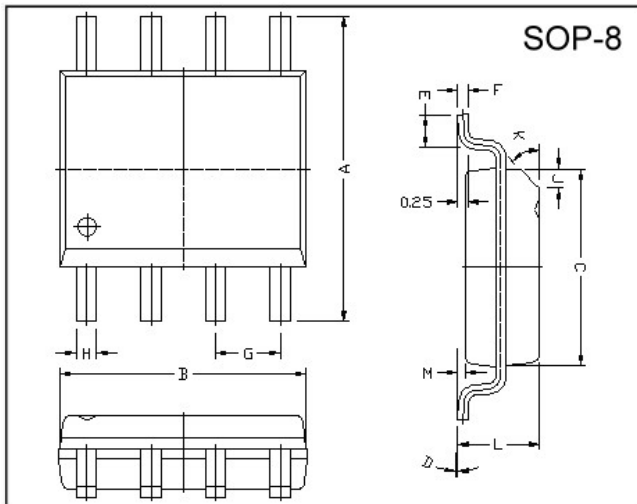
The GSS4501S provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOP-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

Features

- *Simple Drive Requirement
- *Low On-resistance
- *Schottky Diode Included

Package Dimensions



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		N-channel	P-channel	
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current ³	$I_D @ TA=25^\circ C$	6	-5.3	A
Continuous Drain Current ³	$I_D @ TA=70^\circ C$	4.8	-4.7	A
Pulsed Drain Current ¹	I_{DM}	20	-20	A
Total Power Dissipation	$P_D @ TA=25^\circ C$	2.0		W
Linear Derating Factor		0.016		W/°C
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55 ~ +150		°C

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient ³ Max.	R_{thj-a}	62.5	°C/W

N-Channel Electrical Characteristics (T_j = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	30	-	-	V	V _{GS} =0, I _D =250uA
Gate Threshold Voltage	V _{GS(th)}	1.0	-	3.0	V	V _{DS} =V _{GS} , I _D =250uA
Forward Transconductance	g _{fs}	-	12	-	S	V _{DS} =10V, I _D =6A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	100	uA	V _{DS} =30V, V _{GS} =0
Drain-Source Leakage Current(T _j =70°C)		-	-	1	mA	V _{DS} =24V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(ON)}	-	-	33	mΩ	V _{GS} =10V, I _D =6A
		-	-	50		V _{GS} =4.5V, I _D =5A
Total Gate Charge ²	Q _g	-	8.2	-	nC	I _D =6A V _{DS} =24V V _{GS} =4.5V
Gate-Source Charge	Q _{gs}	-	2	-		
Gate-Drain ("Miller") Change	Q _{gd}	-	4.3	-		
Turn-on Delay Time ²	T _{d(on)}	-	6	-	ns	V _{DS} =15V I _D =1A V _{GS} =10 R _G =3.3Ω R _D =15Ω
Rise Time	T _r	-	5.2	-		
Turn-off Delay Time	T _{d(off)}	-	18.8	-		
Fall Time	T _f	-	4.4	-		
Input Capacitance	C _{iss}	-	645	-	pF	V _{GS} =0V V _{DS} =25V f=1.0MHz
Output Capacitance	C _{oss}	-	150	-		
Reverse Transfer Capacitance	C _{rss}	-	95	-		

Source-Drain & Schottky Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	0.5	V	I _S =1.7A, V _{GS} =0V
Reverse Recovery Time	T _{rr}	-	16	-	ns	I _S =1.7A, V _{GS} =0V di/dt=100A/μs
Reverse Recovery Charge	Q _{rr}	-	8	-	nC	

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

3. Surface mounted on 1 in² copper pad of FR4 board; 135°C/W when mounted on Min. copper pad.

P-Channel Electrical Characteristics (T_j = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	-30	-	-	V	V _{GS} =0, I _D =-250uA
Gate Threshold Voltage	V _{GS(th)}	-1.0	-	-3.0	V	V _{DS} =V _{GS} , I _D =-250uA
Forward Transconductance	g _{fs}	-	8.5	-	S	V _{DS} =-10V, I _D =-5.3A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	-1	uA	V _{DS} =-30V, V _{GS} =0
Drain-Source Leakage Current(T _j =70°C)		-	-	-25	uA	V _{DS} =-24V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(ON)}	-	-	50	mΩ	V _{GS} =-10V, I _D =-5.3A
				90		V _{GS} =-4.5V, I _D =-4.2A
Total Gate Charge ²	Q _g	-	20	-	nC	I _D =-5.3A V _{DS} =-15V V _{GS} =-10V
Gate-Source Charge	Q _{gs}	-	3.5	-		
Gate-Drain ("Miller") Change	Q _{gd}	-	2	-		
Turn-on Delay Time ²	T _{d(on)}	-	12	-	ns	V _{DS} =-15V I _D =-1A V _{GS} =-10V R _G =6Ω R _D =15Ω
Rise Time	T _r	-	20	-		
Turn-off Delay Time	T _{d(off)}	-	45	-		
Fall Time	T _f	-	27	-		
Input Capacitance	C _{iss}	-	790	-	pF	V _{GS} =0V V _{DS} =-15V f=1.0MHz
Output Capacitance	C _{oss}	-	440	-		
Reverse Transfer Capacitance	C _{rss}	-	120	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	-1.2	V	I _S =-2.6A, V _{GS} =0V
Reverse Recovery Time	T _{rr}	-	33.4	-	ns	I _S =-2.6A, V _{GS} =0V dI/dt=100A/μs
Reverse Recovery Charge	Q _{rr}	-	52	-	nC	

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

3. Surface mounted on 1 in² copper pad of FR4 board; 135°C/W when mounted on Min. copper pad.

Characteristics Curve N-Channel

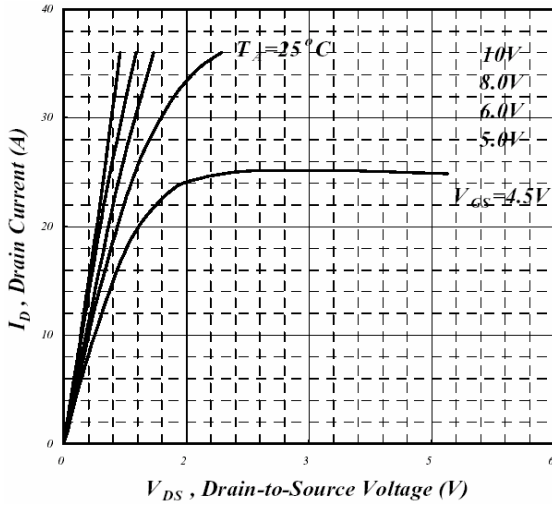


Fig 1. Typical Output Characteristics

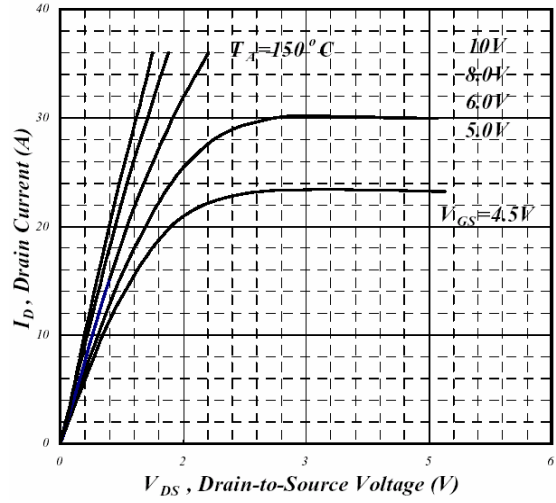


Fig 2. Typical Output Characteristics

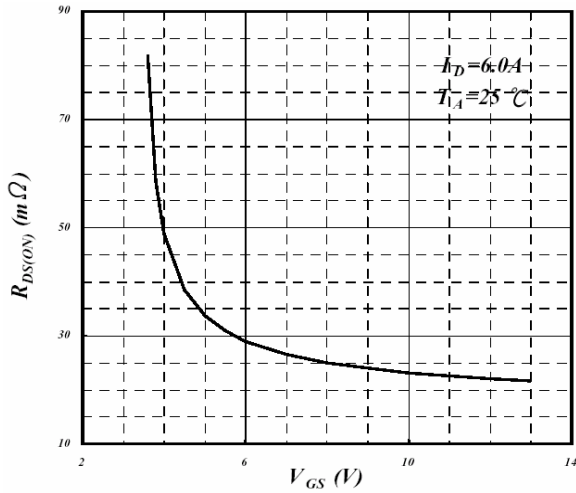


Fig 3. On-Resistance v.s. Gate Voltage

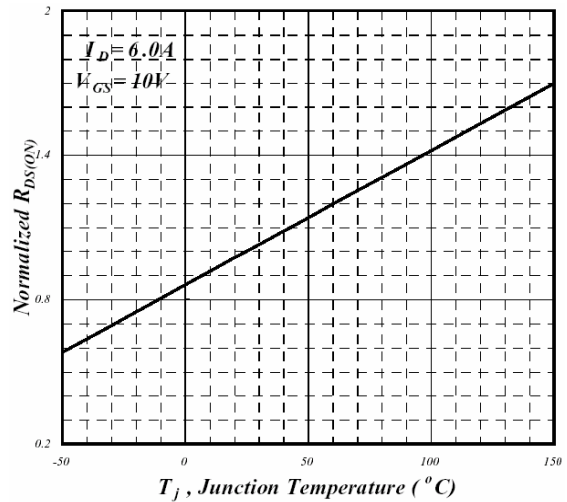


Fig 4. Normalized On-Resistance v.s. Junction Temperature

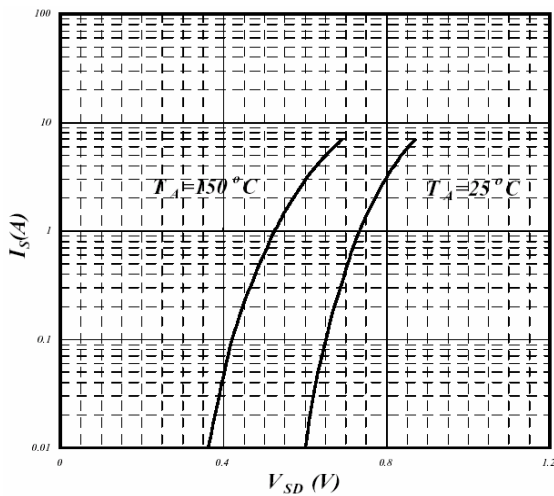


Fig 5. Forward Characteristics of Reverse Diode

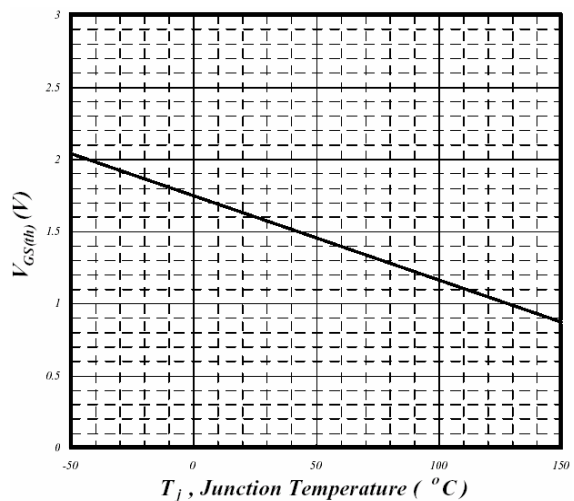


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

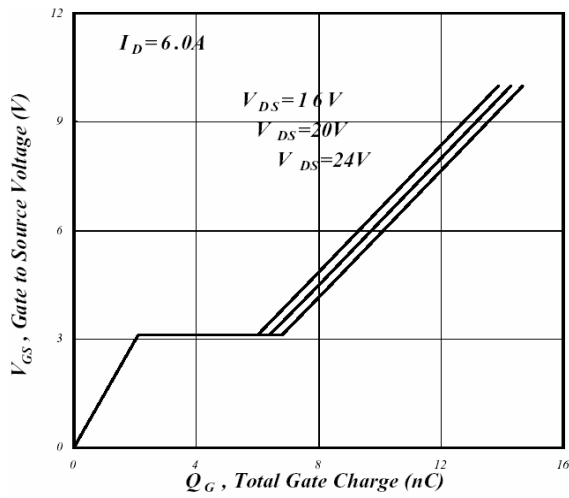


Fig 7. Gate Charge Characteristics

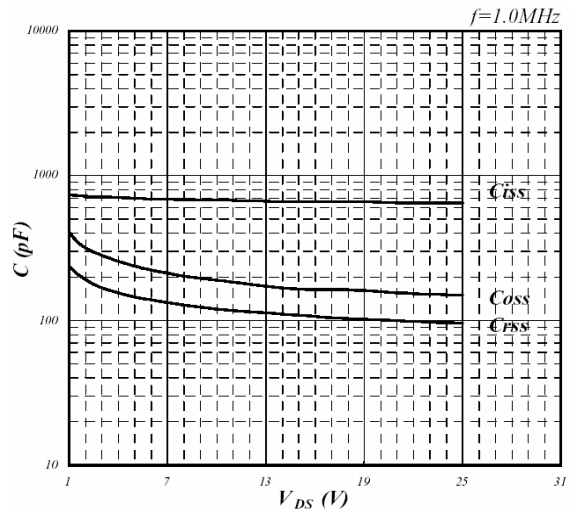


Fig 8. Typical Capacitance Characteristics

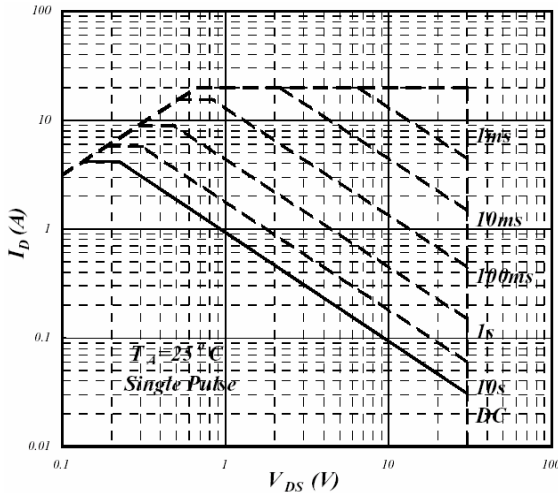


Fig 9. Maximum Safe Operating Area

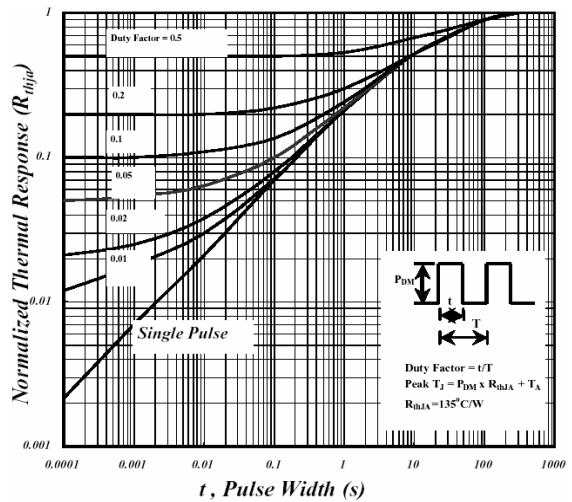


Fig 10. Effective Transient Thermal Impedance

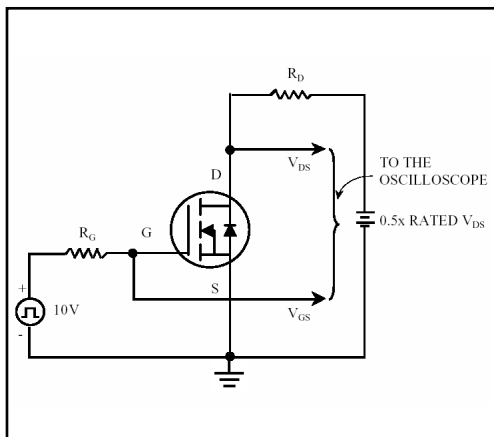


Fig 11. Switching Time Circuit

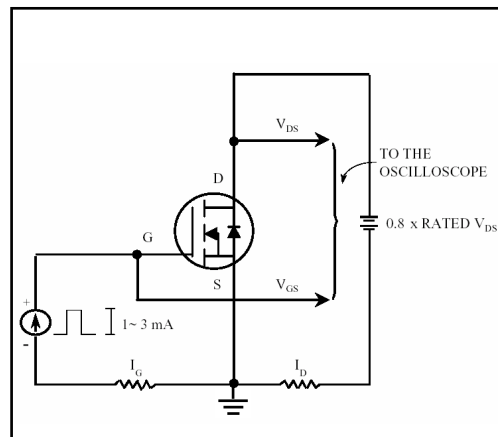


Fig 12. Gate Charge Circuit

P-Channel

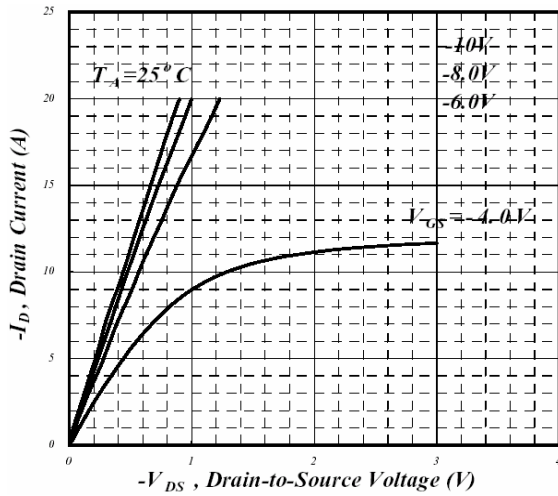


Fig 1. Typical Output Characteristics

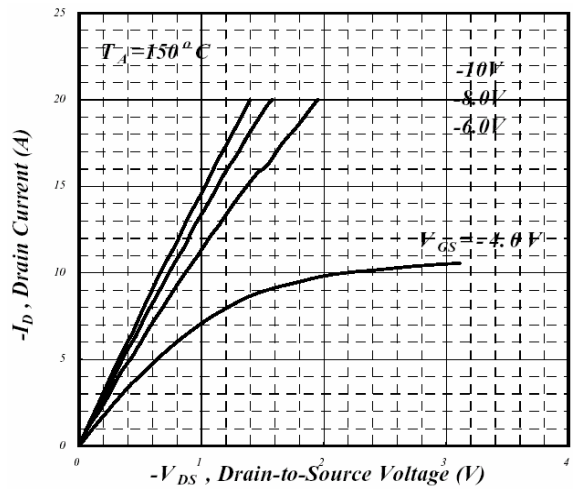


Fig 2. Typical Output Characteristics

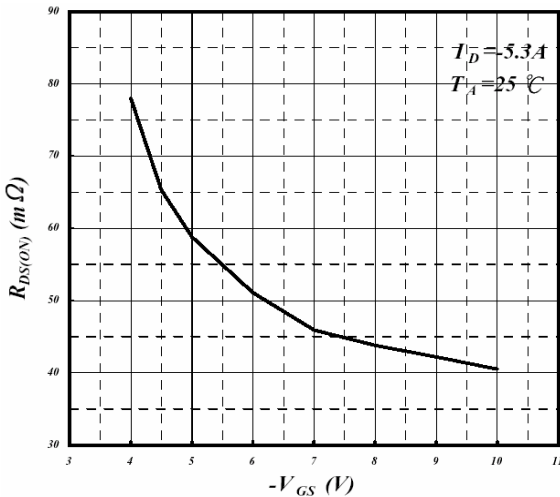


Fig 3. On-Resistance v.s. Gate Voltage

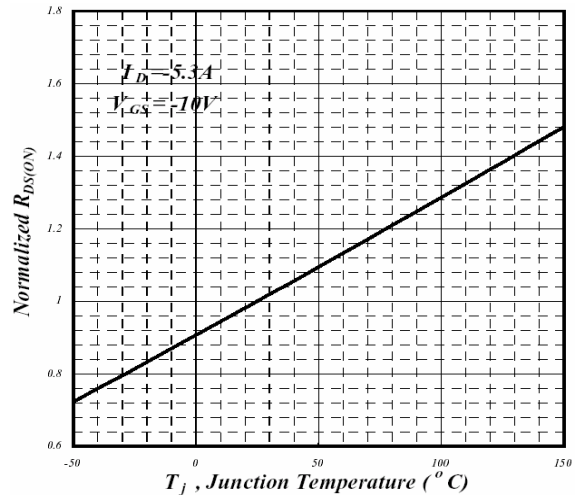


Fig 4. Normalized On-Resistance v.s. Junction Temperature

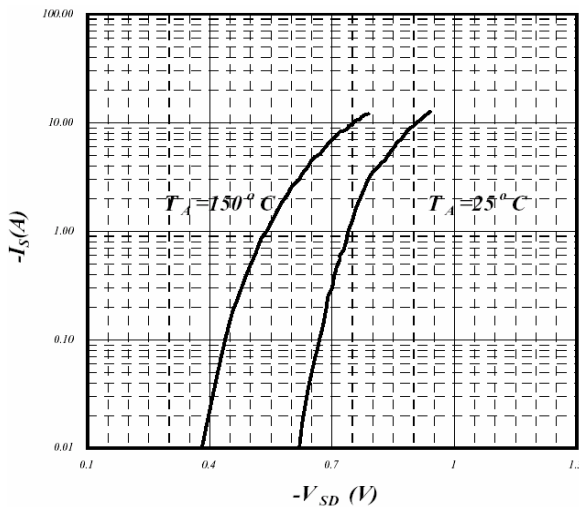


Fig 5. Forward Characteristics of Reverse Diode

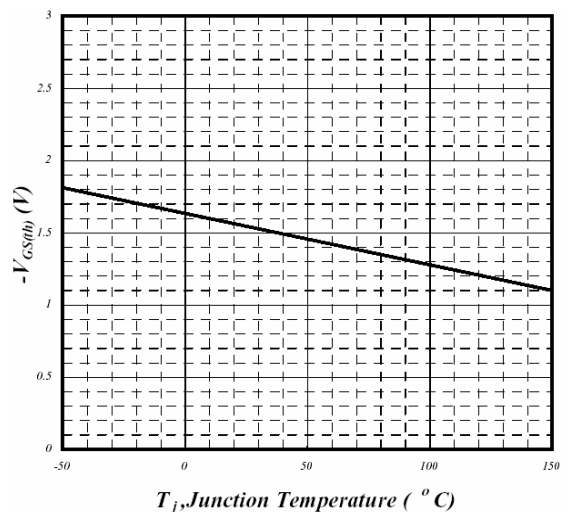


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

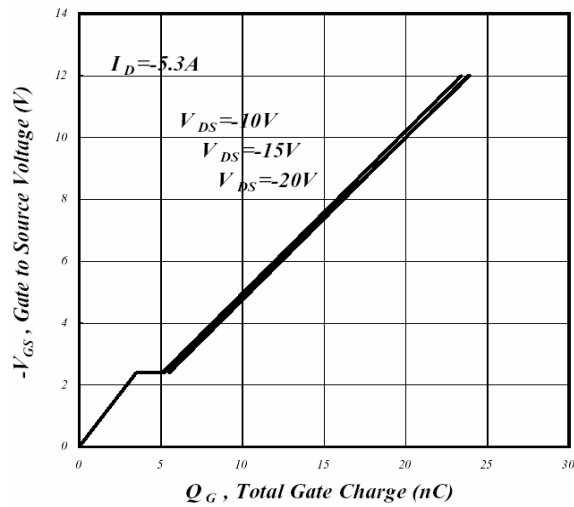


Fig 7. Gate Charge Characteristics

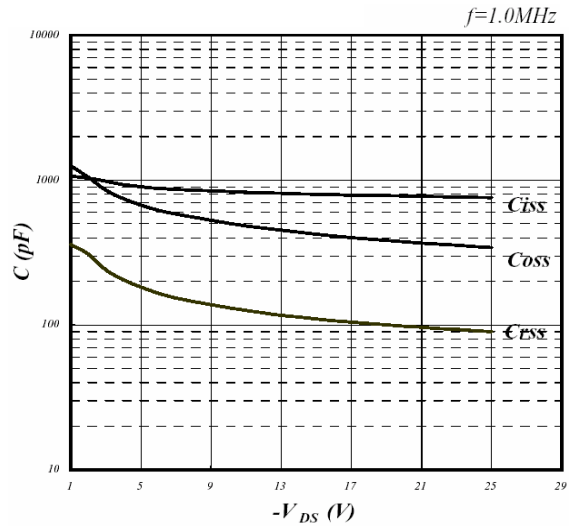


Fig 8. Typical Capacitance Characteristics

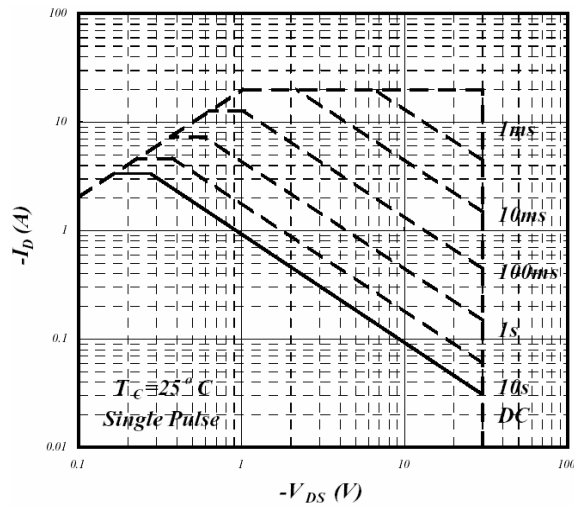


Fig 9. Maximum Safe Operating Area

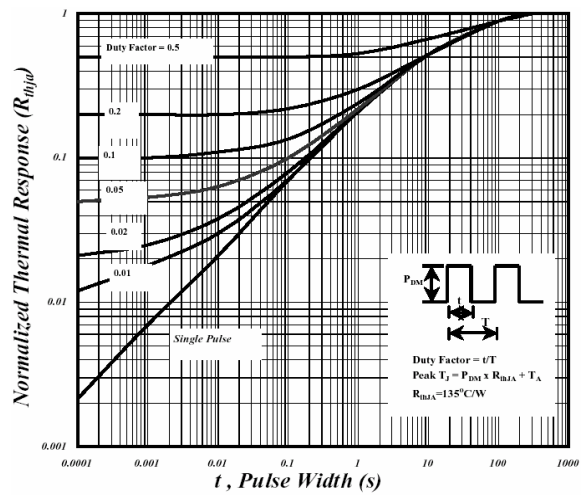


Fig 10. Effective Transient Thermal Impedance

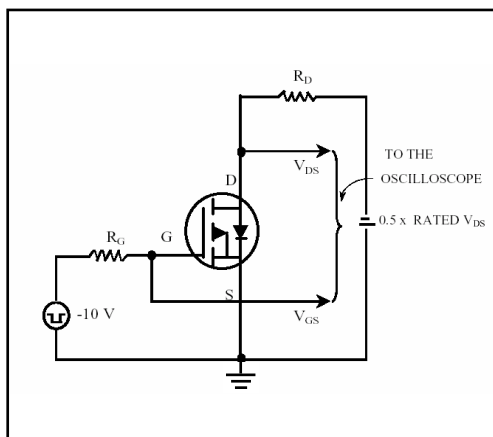


Fig 11. Switching Time Circuit

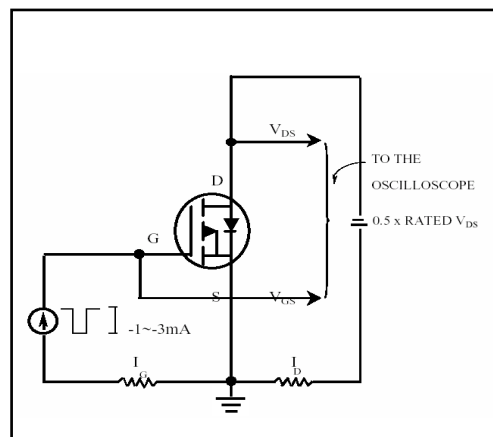


Fig 12. Gate Charge Circuit

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