HD74AC646/HD74ACT646 • Octal Transceiver/Register with 3-State Output

Description

The HD74AC646/HD74ACT646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the Low-to-High transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.

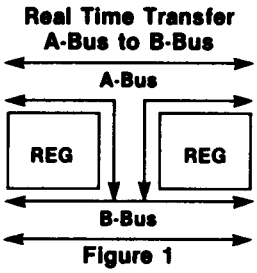


Figure 1

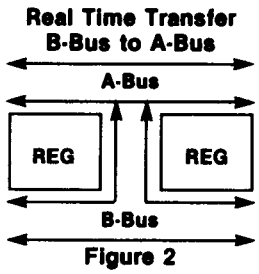


Figure 2

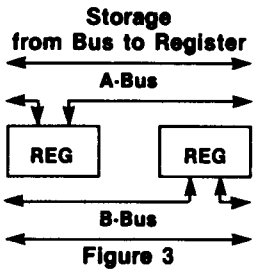


Figure 3

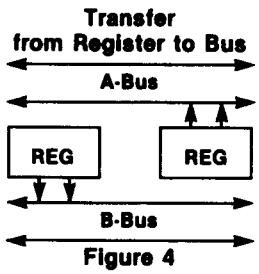
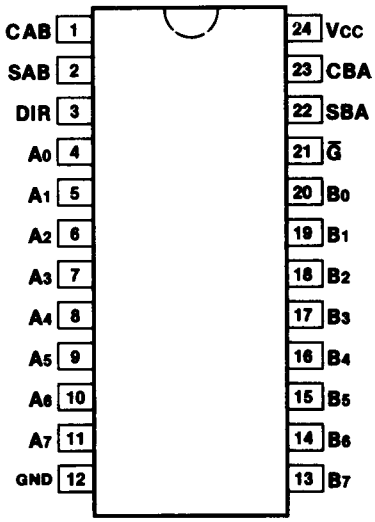


Figure 4

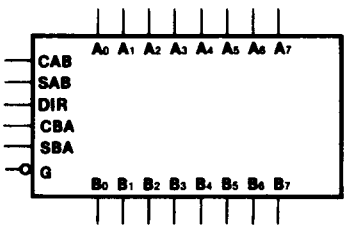
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3-State Outputs
- 300 mil Slim Dual In-Line Package
- Outputs Source/Sink 24 mA
- HD74ACT646 have TTL-Compatible Inputs

Pin Assignment



(Top View)

Logic Symbol



Pin Names

A_0-A_7	Data Register A Inputs
	Data Register A Outputs
B_0-B_7	Data Register B Inputs
	Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

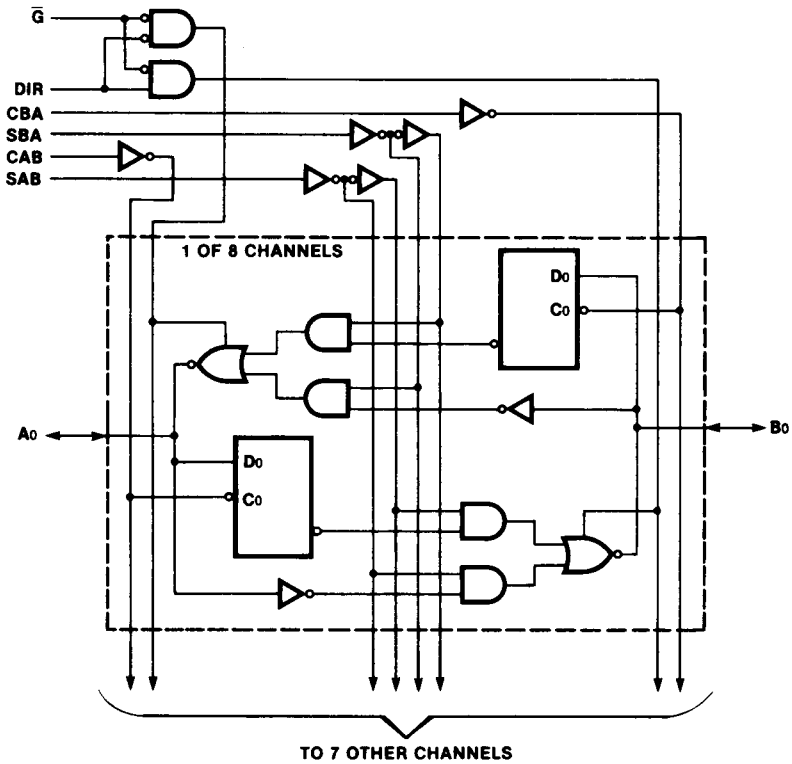
Truth Table

Inputs						Data I/O*		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A_0-A_7	B_0-B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	⌐	⌐	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
⌐ = Low-to-High Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN}=Vcc or Ground, Vcc=5.5V, Ta=Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN}=Vcc or Ground, Vcc=5.5V, Ta=25°C
I_{CCT}	Maximum Additional Icc/Input(HD74ACT646)	1.5	mA	V_{IN}=Vcc-2.1V, Vcc=5.5V, Ta=Worst Case

AC Characteristics: HD74AC646

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Clock to Bus	3.3	1.0	10.5	16.5	1.0	18.5	ns
		5.0	1.0	7.5	12.0	1.0	13.0	
t_{PHL}	Propagation Delay Clock to Bus	3.3	1.0	9.5	14.5	1.0	16.0	ns
		5.0	1.0	6.5	10.5	1.0	11.5	
t_{PLH}	Propagation Delay Bus to Bus	3.3	1.0	7.5	12.0	1.0	13.5	ns
		5.0	1.0	5.0	8.0	1.0	9.0	
t_{PHL}	Propagation Delay Bus to Bus	3.3	1.0	7.5	12.5	1.0	13.5	ns
		5.0	1.0	5.0	9.0	1.0	9.5	
t_{PLH}	Propagation Delay SBA or SAB to An or Bn (w/ An or Bn HIGH or LOW)	3.3	1.0	8.5	13.5	1.0	15.5	ns
		5.0	1.0	6.0	10.0	1.0	11.0	
t_{PHL}	Propagation Delay SBA or SAB to An or Bn (w/ An or Bn HIGH or LOW)	3.3	1.0	8.5	13.5	1.0	15.0	ns
		5.0	1.0	6.0	10.0	1.0	11.0	
t_{PZH}	Enable Time $\overline{G}$ to An or Bn	3.3	1.0	7.0	11.5	1.0	12.5	ns
		5.0	1.0	5.0	8.5	1.0	9.0	
t_{PZL}	Enable Time $\overline{G}$ to An or Bn	3.3	1.0	7.5	12.5	1.0	14.0	ns
		5.0	1.0	5.5	9.0	1.0	10.0	
t_{PHZ}	Disable Time $\overline{G}$ to An or Bn	3.3	1.0	8.0	12.5	1.0	13.5	ns
		5.0	1.0	6.5	10.0	1.0	11.0	
t_{PLZ}	Disable Time $\overline{G}$ to An or Bn	3.3	1.0	7.5	12.0	1.0	13.5	ns
		5.0	1.0	6.0	9.5	1.0	10.5	
t_{PZH}	Enable Time DIR to An or Bn	3.3	1.0	6.5	11.0	1.0	12.0	ns
		5.0	1.0	5.0	7.5	1.0	8.5	
t_{PZL}	Enable Time DIR to An or Bn	3.3	1.0	7.0	11.5	1.0	13.0	ns
		5.0	1.0	5.0	8.0	1.0	9.0	
t_{PHZ}	Disable Time DIR to An or Bn	3.3	1.0	7.5	11.5	1.0	12.5	ns
		5.0	1.0	5.5	9.5	1.0	10.0	
t_{PLZ}	Disable Time DIR to An or Bn	3.3	1.0	7.5	12.0	1.0	13.5	ns
		5.0	1.0	5.5	9.5	1.0	10.5	

*Voltage Range 3.3 is 3.3V±0.3V
Voltage Range 5.0 is 5.0V±0.5V

AC Operating Requirements: HD74AC646

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF		Ta = −40°C to +85°C, C_L = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Set-up Time, HIGH or LOW Bus to Clock	3.3	2.0	5.0	5.5	ns
		5.0	1.5	4.0	4.5	
t_h	Hold Time, HIGH or LOW Clock	3.3	−1.5	0.0	0.0	ns
		5.0	−0.5	0.5	1.0	
t_w	Clock Pulse Width HIGH or LOW	3.3	2.0	3.5	4.5	ns
		5.0	2.0	3.5	3.5	

*Voltage Range 3.3 is 3.3V±0.3V
Voltage Range 5.0 is 5.0V±0.5V

AC Characteristics:HD74ACT646

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C C_L = 50pF			Ta = −40°C to +85°C C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	5.0	100			90		MHz
t_{PLH}	Propagation Delay Clock to Bus	5.0	1.0	12.0	14.5	1.0	16.0	ns
t_{PHL}	Propagation Delay Clock to Bus	5.0	1.0	12.0	14.5	1.0	16.0	ns
t_{PLH}	Propagation Delay Bus to Bus	5.0	1.0	8.5	10.5	1.0	11.5	ns
t_{PHL}	Propagation Delay Bus to Bus	5.0	1.0	8.5	10.5	1.0	11.5	ns
t_{PHL}	Propagation Delay SBA or SAB to A or B(A or B LOW)	5.0	1.0	9.5	11.5	1.0	12.5	ns
t_{PHL}	Propagation Delay SBA or SAB to A or B(A or B HIGH)	5.0	1.0	9.5	11.5	1.0	12.5	ns
t_{PLH}	Propagation Delay SBA or SAB to A or B(A or B LOW)	5.0	1.0	9.5	11.5	1.0	12.5	ns
t_{PLH}	Propagation Delay SBA or SAB to A or B(A or B HIGH)	5.0	1.0	9.5	11.5	1.0	12.5	ns
t_{PZH}	Enable Time G to An or Bn	5.0	1.0	9.0	11.0	1.0	12.0	ns
t_{PZL}	Enable Time G to An or Bn	5.0	1.0	9.0	11.0	1.0	12.0	ns
t_{PHZ}	Disable Time G to An or Bn	5.0	1.0	10.5	13.0	1.0	14.5	ns
t_{PLZ}	Disable Time G to An or Bn	5.0	1.0	10.0	12.5	1.0	14.0	ns
t_{PZH}	Enable Time DIR to An or Bn	5.0	1.0	8.5	10.5	1.0	11.5	ns
t_{PZL}	Enable Time DIR to An or Bn	5.0	1.0	8.5	10.5	1.0	11.5	ns
t_{PHZ}	Disable Time DIR to An or Bn	5.0	1.0	9.5	11.5	1.0	12.5	ns
t_{PLZ}	Disable Time DIR to An or Bn	5.0	1.0	9.0	11.0	1.0	12.0	ns

*Voltage Range 5.0 is 5.0V±0.5V

AC Operating Requirements:HD74ACT646

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C C_L = 50pF		Ta = −40°C to +85°C C_L = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Set up Time, Bus to Clock High or Low	5.0	2.5	7.0	8.0	ns
t_h	Hold Time, Bus to Clock High or Low	5.0	0.0	1.5	1.5	ns
t_w	Pulse width, Clock Pulse width High or Low	5.0	4.5	7.0	8.0	ns

Voltage Range 5.0 is 5.0V±0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

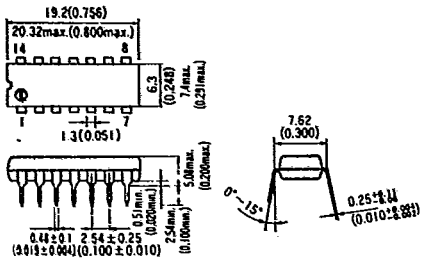
• Package code of Advanced CMOS Logic

HD74AC XXXX P

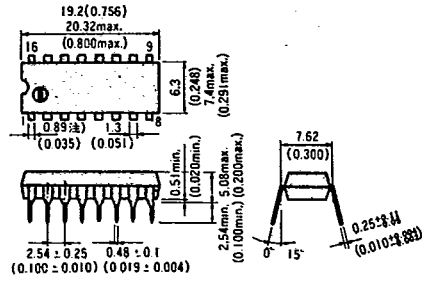
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

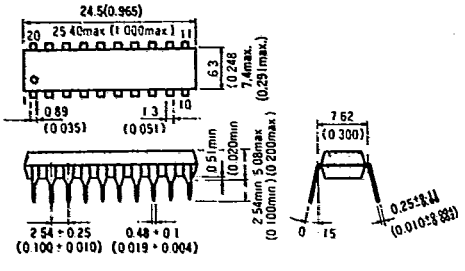
14 Pin type



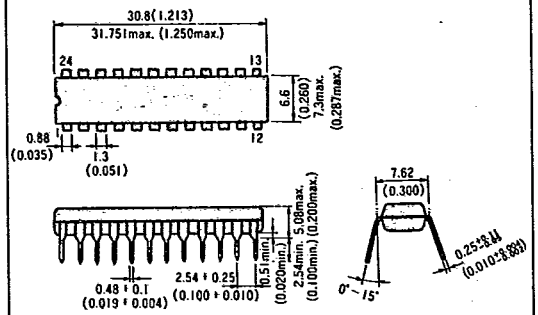
16 Pin type



20 Pin type



24 Pin type



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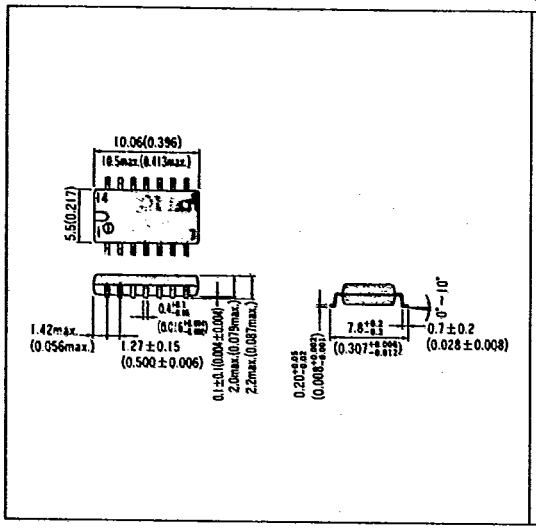
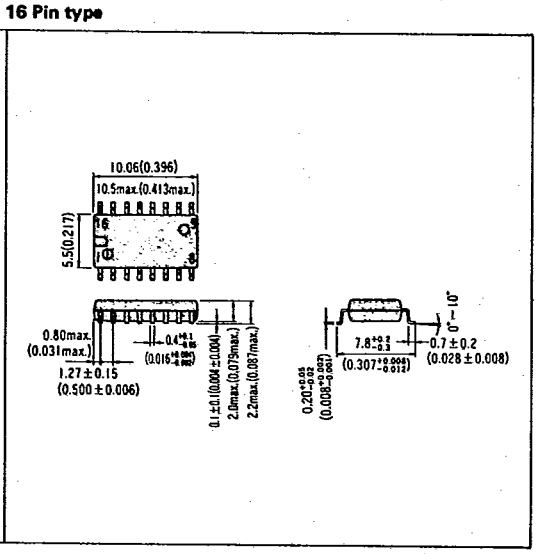
Package Information

Small Outline Package [Unit: mm (inch)]

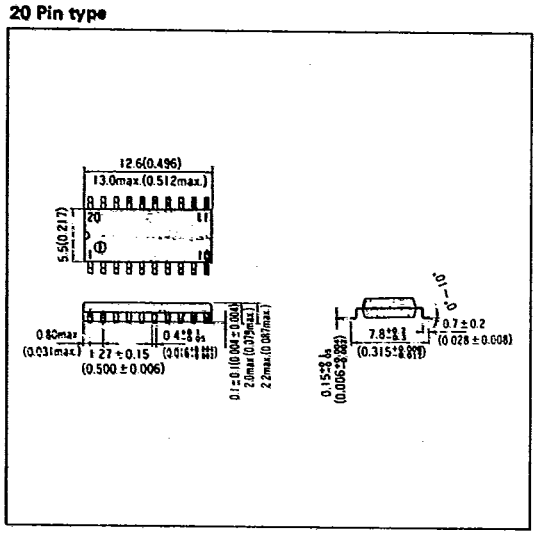
14 Pin type



16 Pin type



20 Pin type



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