

T-46-23-08



Integrated Device Technology, Inc.

CMOS STATIC RAMS
16K (4K x 4-BIT)
Separate Data Inputs and Outputs

IDT71681SA/LA
IDT71682SA/LA

FEATURES:

- Separate data inputs and outputs
- IDT71681SA/LA: outputs track inputs during write mode
- IDT71682SA/LA: high impedance outputs during write mode
- High speed (equal access and cycle time)
 - Military: 12/15/20/25/35/45/55/70/85/100ns (max.)
 - Commercial: 10/12/15/20/25/35/45ns (max.)
- Low power consumption
 - IDT71681/2SA
 - Active: 225mW (typ.)
 - Standby: 100µW (typ.)
 - IDT71681/2LA
 - Active: 225mW (typ.)
 - Standby: 10µW (typ.)
- Battery backup operation—2V data retention (LA version only)
- High-density 24-pin 300-mil ceramic or plastic DIP, 24-pin CERPACK, 24-pin SOIC, 24-pin SOJ and 28-pin leadless chip carrier

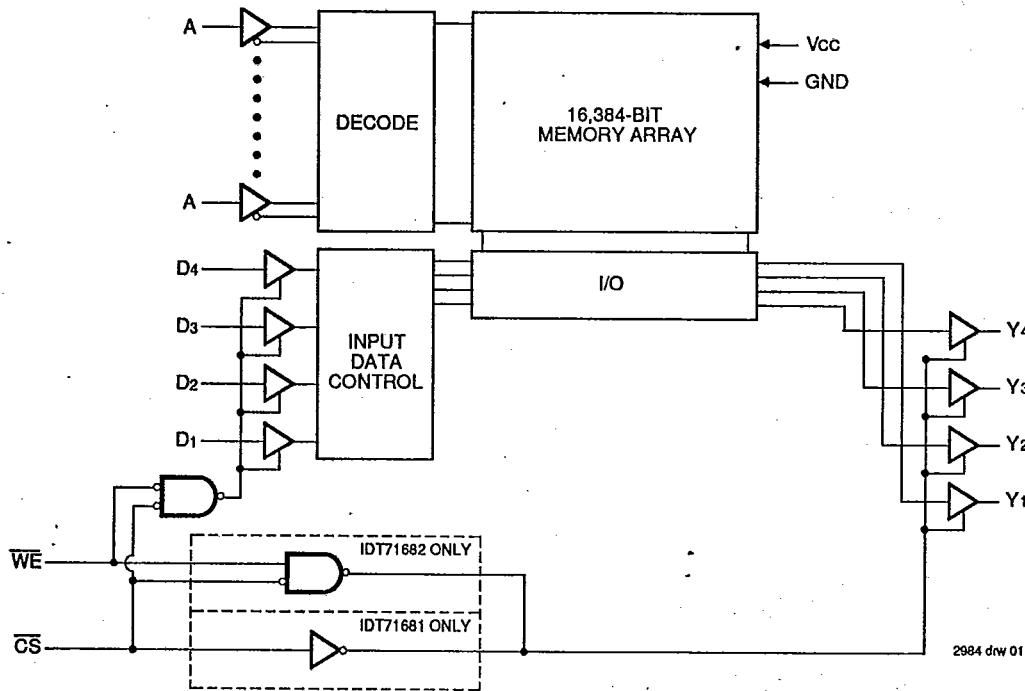
- Produced with advanced CEMOS™ high-performance technology
- CEMOS™ process virtually eliminates alpha particle soft-error rates
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for high-speed memory applications.

Access times as fast as 10ns are available with maximum power consumption of only 550mW. These circuits also offer a reduced power standby mode. When \overline{CS} goes high, the circuit will automatically go to, and remain in, this standby

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

DECEMBER 1990

IDT71681SA/LA, IDT71682SA/LA
CMOS STATIC RAMS 16K (4K x 4-BIT) Separate Data Inputs and Outputs

MILITARY AND COMMERCIAL TEMPERATURE RANGES

DESCRIPTION (Continued):

mode as long as CS remains high. In the standby mode, the devices consume less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) versions also offer a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply.

The IDT71681/IDT71682 are packaged in either space-saving 24-pin, 300-mil DIPs, SOICs, SOJs, CERPACKS, or 28-pin leadless chip carriers, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN DESCRIPTIONS

T-46-23-08

Name	Description
A0-A11	Address Inputs
CS	Chip Select
WE	Write Enable
D1-D4	DATAin
Y1-Y4	DATAout
VCC	Power
GND	Ground

2984 tdl 01

TRUTH TABLE⁽³⁾

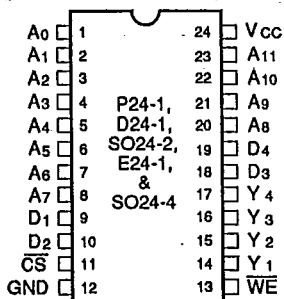
Mode	CS	WE	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DOUT	Active
Write ⁽¹⁾	L	L	DIN	Active
Write ⁽²⁾	L	L	High Z	Active

NOTES:

- For IDT71681 only.
- For IDT71682 only.
- H = VIH, L = VIL, X = don't care.

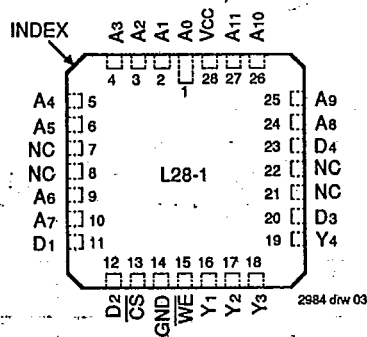
2984 tdl 02

PIN CONFIGURATIONS



2984 drw 02

DIP/SOIC/SOJ/CERPACK TOP VIEW



2984 drw 03

LCC TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	MIL.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
Pr	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2984 tdl 03

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:

- This parameter is determined by device characterization, but is not production tested.

2984 tdl 04

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IDT71681SA/LA, IDT71682SA/LA
CMOS STATIC RAMS 16K (4K x 4-BIT) Separate Data Inputs and Outputs

MILITARY AND COMMERCIAL TEMPERATURE RANGES

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2984 tbl 06

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

2984 tbl 05

DATA RETENTION CHARACTERISTICS

(LA Version Only)

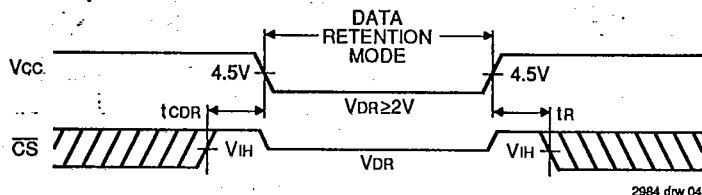
Symbol	Parameter	Test Condition	IDT71681/2LA			Unit	
			Min.	Typ. ⁽¹⁾	Max.		
VDR	Vcc for Data Retention	$\overline{CS} \geq V_{cc} - 0.2V$ $V_{IN} \geq V_{cc} - 0.2V$ or $\leq 0.2V$	2.0	—	—	V	
I _{CCDR}	Data Retention Current		MIL.	—	0.5 ⁽²⁾ 1.0 ⁽³⁾	100 ⁽²⁾ 150 ⁽³⁾	μA
			COM'L.	—	0.5 ⁽²⁾ 1.0 ⁽³⁾	20 ⁽²⁾ 30 ⁽³⁾	μA
t _{CDR} ⁽⁵⁾	Chip Deselect to Data Retention Time			0	—	—	ns
t _R ⁽⁵⁾	Operation Recovery Time		t _{RC} ⁽⁴⁾	—	—	ns	

NOTES:

- TA = +25°C.
- at Vcc = 2V
- at Vcc = 3V
- t_{RC} = Read Cycle Time.
- This parameter is guaranteed, but not tested.

2984 tbl 07

LOW Vcc DATA RETENTION WAVEFORM



2984 drw 04

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71681/2S			IDT71681/2L			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{LI}	Input Leakage Current	Vcc = Max., V _{IN} = GND to Vcc	MIL.	—	—	10	—	—	5	μA
			COM'L.	—	—	5	—	—	2	
I _{LO}	Output Leakage Current	Vcc = Max., $\overline{CS} = V_{IH}$, V _{OUT} = GND to Vcc	MIL.	—	—	10	—	—	5	μA
			COM'L.	—	—	5	—	—	2	
VOL	Output Low Voltage	I _{OL} = 10mA, Vcc = Min.	—	—	0.5	—	—	0.5	V	
		I _{OL} = 8mA, Vcc = Min.	—	—	0.4	—	—	0.4		
VOH	Output High Voltage	I _{OL} = -4mA, Vcc = Min.	2.4	—	—	2.4	—	—	V	

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IDT71681SA/LA, IDT71682SA/LA
CMOS STATIC RAMS 16K (4K x 4-BIT) Separate Data Inputs and Outputs

MILITARY AND COMMERCIAL TEMPERATURE RANGES

DC ELECTRICAL CHARACTERISTICS^(1,4)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

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Symbol	Parameter	Power	71681x10 ⁽⁵⁾ 71682x10 ⁽⁵⁾		71681x12 ⁽⁷⁾ 71682x12 ⁽⁷⁾		71681x15 71682x15		71681x20 71682x20		71681x25 71682x25		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC1}	Operating Power Supply Current CS = V _{IL} , Outputs Open, V _{CC} = Max., f = 0 ⁽³⁾	SA	120	—	110	120	110	120	90	100	90	100	mA
		LA	—	—	—	—	—	—	70	80	70	80	
I _{CC2}	Dynamic Operating Current CS = V _{IL} , Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽³⁾	SA	175	—	165	175	145	165	120	120	110	120	mA
		LA	—	—	—	—	—	—	100	110	90	100	
I _{SB}	Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽³⁾	SA	65	—	65	65	55	65	45	55	35	45	mA
		LA	—	—	—	—	—	—	30	35	25	30	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , V _{CC} = Max., V _{IN} ≥ V _{HC} or V _{IN} ≤ V _{LC} , f = 0 ⁽³⁾	SA	20	—	20	20	20	20	20	20	2	10	mA
		LA	—	—	—	—	—	—	0.5	5	0.05	0.3	



DC ELECTRICAL CHARACTERISTICS (Continued)^(1,4)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71681x35 71682x35		71681x45 71682x45		71681x55 ⁽⁶⁾ 71682x55 ⁽⁶⁾		71681x70 ^(2,6) 71682x70 ^(2,6)		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC1}	Operating Power Supply Current CS = V _{IL} , Outputs Open, V _{CC} = Max., f = 0 ⁽³⁾	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I _{CC2}	Dynamic Operating Current CS = V _{IL} , Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽³⁾	SA	100	110	100	110	—	110	—	110	mA
		LA	80	90	70	80	—	80	—	80	
I _{SB}	Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽³⁾	SA	30	35	30	35	—	35	—	35	mA
		LA	20	25	20	25	—	20	—	20	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , V _{CC} = Max., V _{IN} ≥ V _{HC} or V _{IN} ≤ V _{LC} , f = 0 ⁽³⁾	SA	2	10	2	10	—	10	—	10	mA
		LA	0.05	0.3	0.05	0.3	—	0.3	—	0.3	

NOTES:

1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/trc. f = 0 means no input lines change.
4. "x" in part numbers indicates power rating (SA or LA).
5. 0°C to +70°C temperature range only.
6. -55°C to +125°C temperature range only.
7. Military values for 12ns device are preliminary only.

2984 fbl 09

IDT71681SA/LA, IDT71682SA/LA
CMOS STATIC RAMS 16K (4K x 4-BIT) Separate Data Inputs and Outputs

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

T-46-23-08

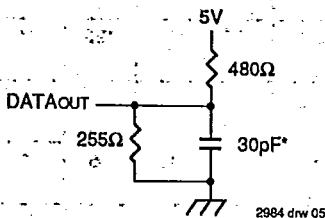


Figure 1. Output Load

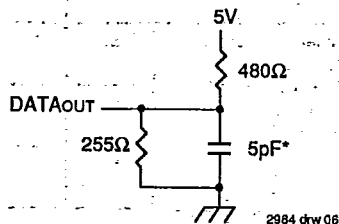


Figure 2. Output Load
(for tHZ, tLZ, tWZ, and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x10 ⁽¹⁾ 71682x10 ⁽¹⁾		71681x12 71682x12		71681x15 71682x15		71681x20 71682x20		71681x25 71682x25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	10	—	12	—	15	—	20	—	25	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	20	—	25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
tLZ	Chip Select to Output in Low Z ⁽³⁾	3	—	3	—	5	—	5	—	5	—	ns
tHZ	Chip Select to Output in High Z ⁽³⁾	—	6	—	7	—	7	—	9	—	10	ns
tPU	Chip Select to Power Up Time ⁽³⁾	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Select to Power Down Time ⁽³⁾	—	10	—	10	—	15	—	20	—	25	ns

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IDT71681SA/LA, IDT71682SA/LA
CMOS STATIC RAMS 16K (4K x 4-BIT) Separate Data Inputs and Outputs

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS (Continued) ($V_{CC} = 5.0V \pm 10\%$, All Temperature Ranges)

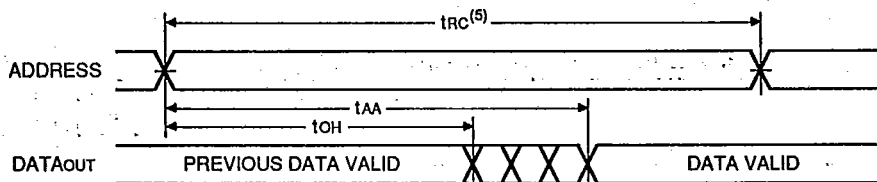
Symbol	Parameter	71681x35 71682x35		71681x45 71682x45		71681x55 ⁽²⁾ 71682x55 ⁽²⁾		71681x70 ⁽²⁾ 71682x70 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		Read Cycle								
t _{RC}	Read Cycle Time	35	—	45	—	55	—	70	—	ns
t _{AA}	Address Access Time	—	35	—	45	—	55	—	70	ns
t _{ACS}	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
t _{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t _{LZ}	Chip Select to Output in Low Z ⁽³⁾	5	—	5	—	5	—	5	—	ns
t _{HZ}	Chip Select to Output in High Z ⁽³⁾	—	15	—	20	—	25	—	30	ns
t _{PU}	Chip Select to Power Up Time ⁽³⁾	0	—	0	—	0	—	0	—	ns
t _{PD}	Chip Select to Power Down Time ⁽³⁾	—	35	—	40	—	50	—	60	ns

NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. "x" in part numbers indicates power rating SA or LA.

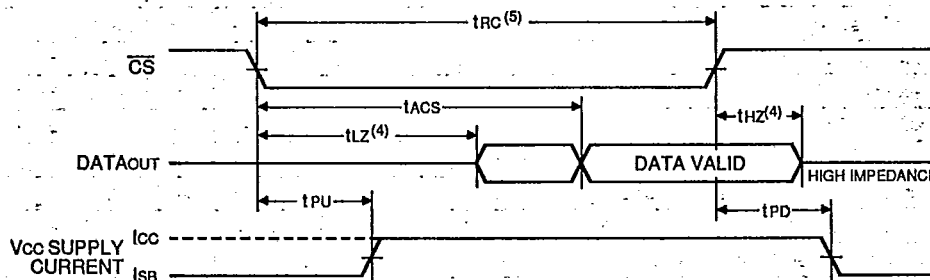
2984 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1^(1, 2)



2984 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 3)



2984 drw 08

NOTES:

1. WE is High for READ Cycle.
2. CS is Low for READ Cycle.
3. Address valid prior to or coincident with CS transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

IDT71681SA/LA, IDT71682SA/LA

CMOS STATIC RAMS 16K (4K x 4-BIT) Separate Data Inputs and Outputs

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

T-46-23-08

Symbol	Parameter	71681x10 ⁽¹⁾ 71682x10 ⁽¹⁾		71681x12 71682x12		71681x15 71682x15		71681x20 71682x20		71681x25 71682x25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	20	—	ns
tCW	Chip Select to End of Write	10	—	10	—	15	—	20	—	20	—	ns
tAW	Address Valid to End of Write	10	—	10	—	15	—	20	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	10	—	15	—	20	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	7	—	8	—	9	—	10	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tV	Data Valid to Output Valid (71681 only) ⁽³⁾	—	10	—	12	—	15	—	20	—	25	ns
tWY	Write Enable to Output Valid (71681 only) ⁽³⁾	—	10	—	12	—	15	—	20	—	25	ns
tWZ	Write Enable to Output in High Z (71682 only) ⁽³⁾	—	4	—	5	—	6	—	7	—	7	ns
tOW	Output Active from End of Write (71682 only) ⁽³⁾	0	—	0	—	0	—	0	—	0	—	ns

AC ELECTRICAL CHARACTERISTICS (Continued) (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

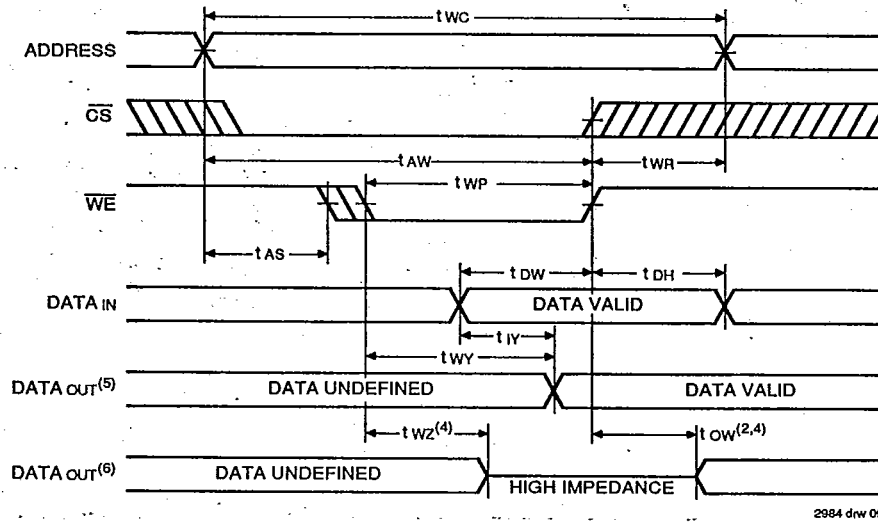
Symbol	Parameter	71681x35 71682x35		71681x45 71682x45		71681x55 ⁽²⁾ 71682x55 ⁽²⁾		71681x70 ⁽²⁾ 71682x70 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tWC	Write Cycle Time	30	—	40	—	50	—	60	—	ns
tCW	Chip Select to End of Write	25	—	35	—	50	—	60	—	ns
tAW	Address Valid to End of Write	25	—	35	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	25	—	30	—	35	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	20	—	25	—	ns
tDH	Data Hold Time	3	—	3	—	3	—	3	—	ns
tV	Data Valid to Output Valid (71681 only) ⁽³⁾	—	30	—	35	—	35	—	40	ns
tWY	Write Enable to Output Valid (71681 only) ⁽³⁾	—	30	—	35	—	35	—	40	ns
tWZ	Write Enable to Output in High Z (71682 only) ⁽³⁾	—	13	—	20	—	25	—	30	ns
tOW	Output Active from End of Write (71682 only) ⁽³⁾	0	—	0	—	0	—	0	—	ns

NOTES:

- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter guaranteed but not tested.
- "x" in part numbers indicates power rating SA or LA.

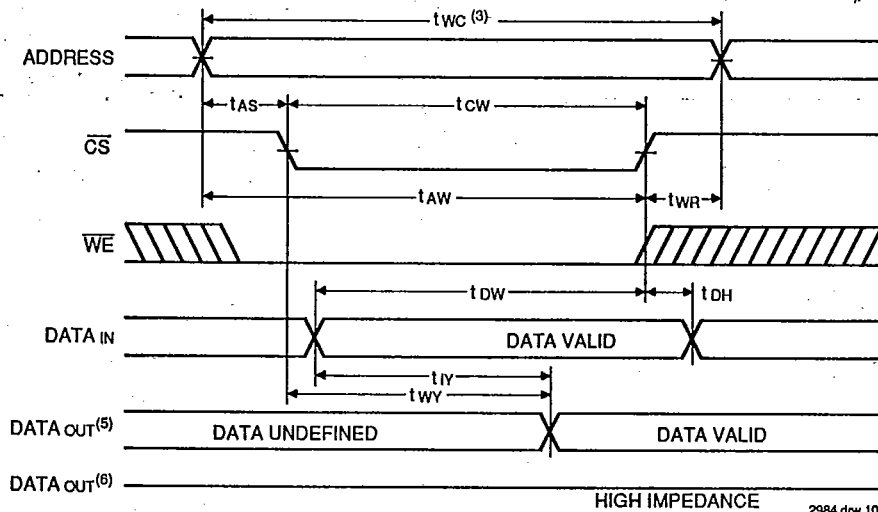
2984 tbl 12

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)⁽¹⁾ T-46-23-08



2984 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED)⁽¹⁾



2984 drw 10

NOTES:

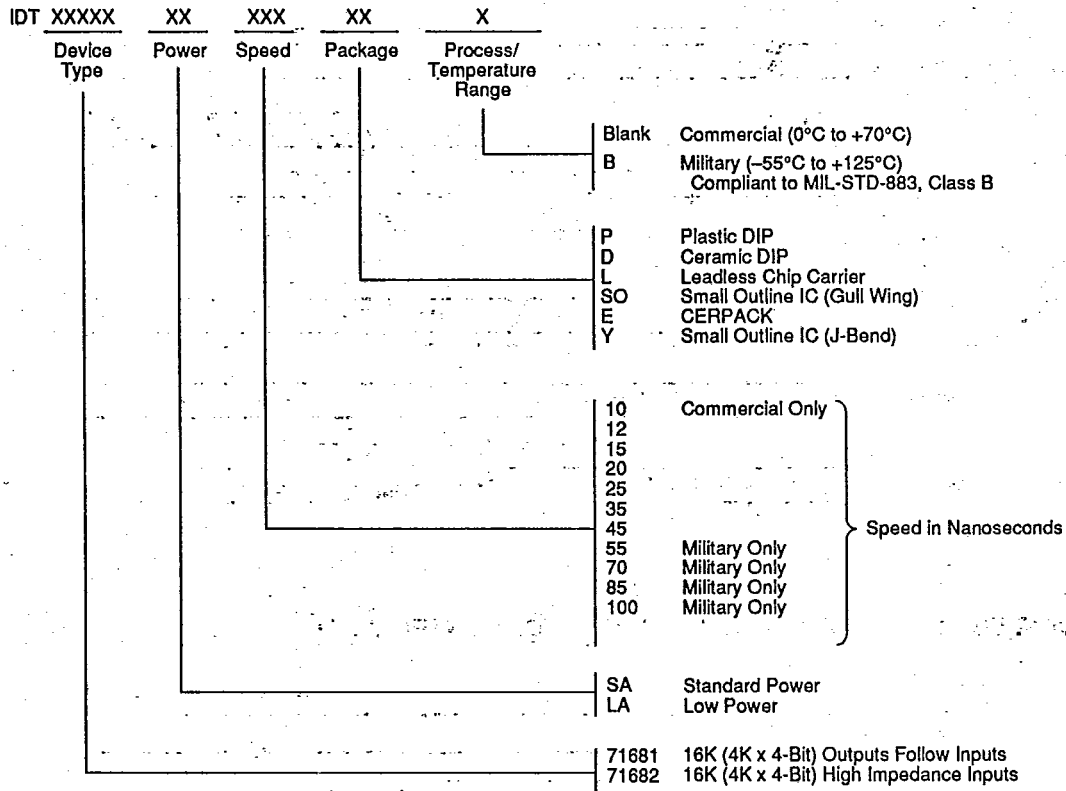
1. \overline{WE} or \overline{CS} must be high during all address transitions.
2. If the \overline{CS} goes high simultaneously with \overline{WE} high, the outputs remain in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured $\pm 200\text{mV}$ from steady state voltage with specified loading in Figure 2.
5. For IDT71681 only.
6. For IDT71682 only.

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IDT71681SA/LA, IDT71682SA/LA
CMOS STATIC RAMS 16K (4K x 4-BIT) Separate Data Inputs and Outputs

MILITARY AND COMMERCIAL TEMPERATURE RANGES

ORDERING INFORMATION



2984 drw 11