19-1567; Rev 1; 2/01

EVALUATION KIT AVAILABLE

+2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

General Description

The MAX2267/MAX2268/MAX2269 power amplifiers are optimized for IS-98-based CDMA and PDC cellular telephones operating in the Japanese cellular-frequency band. When matched for CDMA operation, the amplifiers achieve 27dBm output power with 35% efficiency (MAX2268), with margin over the adjacent and alternate channel specification. At a +17dBm output—a very common power level for CDMA phones—the MAX2268 still has 7% efficiency, yielding excellent overall talk time. At the same power level, the MAX2267/MAX2269 have an unprecedented 12%/17% efficiency, while still obtaining 28%/29% efficiency at maximum output power.

The MAX2267/MAX2268/MAX2269 have internally referenced bias ports that are normally terminated with simple resistors. The bias ports allow customization of ACPR margin and gain. They can also be used to "throttle back" bias current when generating low power levels. The MAX2267/MAX2268/MAX2269 have excellent gain stability over temperature (±0.8dB), so overdesign of driver stages and excess driver current are dramatically reduced, further increasing the phone's talk time. The devices can be operated from +2.7V to +4.5V while meeting all ACPR specifications over the entire temperature range.

The devices are packaged in a 16-pin TSSOP with exposed paddle (EP). For module or direct chip attach applications, the MAX2267 is also available in die form.

Applications

Cellular-Band CDMA Phones

Cellular-Band PDC Phones

2-Way Pagers

Power-Amplifier Modules

Selector Guide

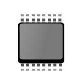
DEVICE	HIGH POWER-ADDED EFFICIENCY (%)		
	CDMA AT +27dBm	**CDMA AT +17dBm**	**PDC AT +29dBm**
MAX2267	28	12	—
MAX2268	34	7	41
MAX2269	29	17	—

Features

- ♦ **Low Average CDMA Current Consumption in Typical Urban Scenario**
  - **55mA (MAX2267)**
  - **90mA (MAX2268)**
  - **50mA (MAX2269)**
- ♦ **0.5µA Shutdown Mode Eliminates External Supply Switch**
- ♦ **±0.8dB Gain Variation Over Temperature**
- ♦ **No External Reference or Logic Interface Circuitry Needed**
- ♦ **Supply Current and ACPR Margin Dynamically Adjustable**
- ♦ **+2.7V to +4.5V Single-Supply Operation**
- ♦ **35% Efficiency at +2.7V Operation**

Ordering Information

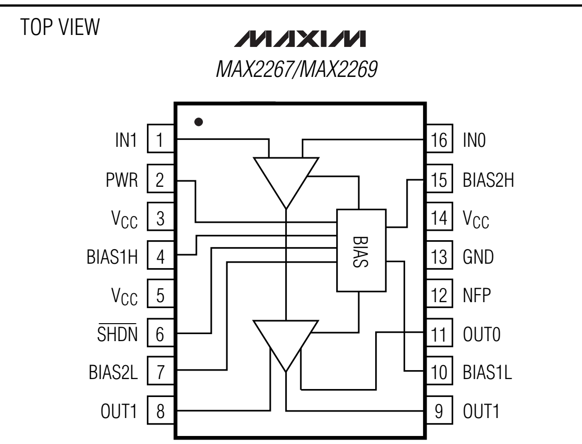
PART	TEMP. RANGE	PIN-PACKAGE
MAX2267EUE	-40°C to +85°C	16 TSSOP-EP
MAX2267E/D	-40°C to +85°C	Dice*
MAX2268EUE	-40°C to +85°C	16 TSSOP-EP
MAX2269EUE	-40°C to +85°C	16 TSSOP-EP



TSSOP-EP
5mm x 6.4mm

*Contact factory for dice specifications.

Pin Configurations/ Functional Diagrams



TSSOP-EP

Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND (no RF input) ....-0.3V to +5V
Logic Inputs to GND..................................-0.3V to (V_{CC} + 0.3V)
BIAS_ _ to GND ....-0.3V to (V_{CC} + 0.3V)
RF Input Power ....+6dBm (20mW)
Logic Input Current..±10mA
Output VSWR with +6dBm Input 2.5:1

Total DC Power Dissipation (T_{PADDLE} = +100°C)
16-Pin TSSOP-EP (derate 60mW/°C
above T_{PADDLE} = +100°C)..4W
θ_{JA} ....8°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +4.5V no input signal applied, $V_{\overline{SHDN}}$ = 2.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.5V and T_A = +25°C.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}			2.7		4.5	V
Idle Current	I_{CC}	MAX2267/MAX2269	PWR = V_{CC}		100		mA
			PWR = GND		34		
		MAX2268			90		
Shutdown Supply Current	I_{CC}	$\overline{SHDN}$ = PWR = GND			0.5	10	µA
Logic Input Current High		Logic = V_{CC}		-1		5	µA
Logic Input Current Low		Logic = GND		-1		1	µA
Logic Threshold High				2.0			V
Logic Threshold Low						0.8	V

AC ELECTRICAL CHARACTERISTICS—MAX2267

(MAX2267 EV kit, V_{CC} = V_{PWR} = $V_{\overline{SHDN}}$ = +3.5V, f_{IN} = 906MHz, CDMA modulation, $\overline{SHDN}$ = V_{CC}, matching networks tuned for 887MHz to 925MHz operation, 50Ω system, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Range (Notes 1, 2)	f_{IN}	PWR = V_{CC} or GND		887		925	MHz
Power Gain (Note 1)	G_P	T_A = +25°C		24.5	26		dB
		T_A = T_{MIN} to T_{MAX}		23			
		PWR = GND		20.5	23		
Gain Variation vs. Temperature (Note 1)		T_A = T_{MIN} to T_{MAX}, relative to T_A = +25°C			±0.8		dB
Output Power (High-Power Mode) (Note 1)	P_{OUT}	ACPR specification met with f_{IN} = 887MHz to 925MHz	PWR = V_{CC}	27			dBm
			PWR = V_{CC} = 2.8V	24.5	25.5		
Output Power (Low-Power Mode) (Note 1)	P_{OUT}	ACPR specification met with f_{IN} = 887MHz to 925MHz	PWR = GND	16	17.5		dBm
			PWR = GND, V_{CC} = 2.8V	14	15.5		

AC ELECTRICAL CHARACTERISTICS—MAX2267 (continued)

(MAX2267 EV kit, V_{CC} = V_{PWR} = $V_{\overline{SHDN}}$ = +3.5V, f_{IN} = 906MHz, CDMA modulation, $\overline{SHDN}$ = V_{CC}, matching networks tuned for 887MHz to 925MHz operation, 50Ω system, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Adjacent-Channel Power Ratio Limit (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 4.5V, offset = 885kHz, 30kHz BW, f_{IN} = 887MHz to 925MHz	-44	-48		dBc
Alternate-Channel Power Ratio Limit (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 4.5V, offset = 1980kHz, 30kHz BW, f_{IN} = 887MHz to 925MHz	-56	-57.5		dBc
Power-Added Efficiency (Note 3)	PAE	PWR = V_{CC}, P_{OUT} = +27dBm		28		%
		PWR = GND, P_{OUT} = 17.5dBm		12		
Power-Mode Switching Time		(Note 4)		550		ns
Turn-On Time (Notes 1, 4)		PWR = V_{CC} or GND		1	5	µs
Maximum Input VSWR	VSWR	f_{IN} = 887MHz to 925MHz, PWR = GND or V_{CC}		2.3:1		
Nonharmonic Spurious due to Load Mismatch (Notes 1, 5)		P_{IN} = +6dBm			-60	dBc
Noise Power (Note 6)		Measured at 851MHz		-137		dBm/Hz
		PWR = GND, measured at 851MHz		-134		
Harmonic Suppression		(Note 7)		32		dBc

AC ELECTRICAL CHARACTERISTICS—MAX2268

(MAX2268 EV kit, V_{CC} = $V_{\overline{SHDN}}$ = +3.5V, f_{IN} = 906MHz, CDMA modulation, matching networks tuned for 887MHz to 925MHz operation, 50Ω system, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range (Notes 1, 2)	f_{IN}		887		925	MHz
Power Gain (Note 1)	G_P	T_A = +25°C	25.5	27		dB
		T_A = T_{MIN} to T_{MAX}	24			
Gain Variation vs. Temperature (Note 1)		T_A = T_{MIN} to T_{MAX}, relative to T_A = +25°C		±0.7		dB
Output Power (Note 1)	P_{OUT}	ACPR specification met with f_{IN} = 887MHz to 925MHz, V_{CC} = 3.5V	27			dBm
		ACPR specification met with f_{IN} = 887MHz to 925MHz, V_{CC} = 2.8V	24.5	25.5		
Adjacent-Channel Power Ratio (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 4.5V, offset = 885kHz, 30kHz BW, f_{IN} = 887MHz to 925MHz	-44	-48		dBc
Alternate-Channel Power Ratio (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 4.5V, offset = 1980kHz, 30kHz BW, f_{IN} = 887MHz to 925MHz	-56	-57.5		dBc
Power-Added Efficiency (Note 3)	PAE	P_{IN} adjusted to give P_{OUT} = 27dBm		35		%
		P_{IN} adjusted for P_{OUT} = 13.6dBm		5.5		
Turn-On Time (Notes 1, 4)				1	5	µs
Maximum Input VSWR	VSWR	f_{IN} = 887MHz to 925MHz		1.5:1		

AC ELECTRICAL CHARACTERISTICS—MAX2268 (continued)

(MAX2268 EV kit, V_{CC} = $V_{\overline{SHDN}}$ = +3.5V, f_{IN} = 906MHz, CDMA modulation, matching networks tuned for 887MHz to 925MHz operation, 50Ω system, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Nonharmonic Spurious Due to Load Mismatch (Notes 1, 5)		P_{IN} = +6dBm			-60	dBc
Noise Power (Note 6)		Measured at 851MHz		-138		dBm/Hz
Harmonic Suppression		(Note 7)		47		dBc

AC ELECTRICAL CHARACTERISTICS—MAX2269

(MAX2269 EV kit, V_{CC} = V_{PWR} = $V_{\overline{SHDN}}$ = +3.5V, f_{IN} = 906MHz, CDMA modulation, $\overline{SHDN}$ = V_{CC}, matching networks tuned for 887MHz to 925MHz operation, 50Ω system, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Range (Notes 1, 2)	f_{IN}	PWR = V_{CC} or GND		887		925	MHz
Power Gain (Note 1)	G_P	T_A = +25°C		24.5	26		dB
		T_A = T_{MIN} to T_{MAX}		23			
		PWR = GND		23.5	26		
Gain Variation vs. Temperature (Note 1)		T_A = T_{MIN} to T_{MAX}, relative to T_A = +25°C			±0.8		dB
Output Power (High-Power Mode) (Note 1)	P_{OUT}	ACPR specification met with f_{IN} = 887MHz to 925MHz	PWR = V_{CC}	27			dBm
			PWR = V_{CC} = 2.8V	24.5	25.5		
Output Power (Low-Power Mode) (Note 1)	P_{OUT}	ACPR specification met with f_{IN} = 887MHz to 925MHz	PWR = GND	15.5	17		dBm
			PWR = GND, V_{CC} = 2.8V	13.5	15		
Adjacent-Channel Power Ratio Limit (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 4.5V, offset = 885kHz, 30kHz BW, f_{IN} = 887MHz to 925MHz		-44	-48		dBc
Alternate-Channel Power Ratio Limit (Notes 1, 2)	ACPR	V_{CC} = 2.8V to 4.5V, offset = 1980kHz, 30kHz BW, f_{IN} = 887MHz to 925MHz		-56	-57.5		dBc
Power-Added Efficiency (Note 3)	PAE	PWR = V_{CC}, P_{OUT} = +27dBm			29		%
		PWR = GND, P_{OUT} = 17dBm			17		

AC ELECTRICAL CHARACTERISTICS—MAX2269 (continued)

(MAX2269 EV kit, $V_{CC} = V_{PWR} = V_{\overline{SHDN}}$ = +3.5V, f_{IN} = 906MHz, CDMA modulation, $\overline{SHDN} = V_{CC}$, matching networks tuned for 887MHz to 925MHz operation, 50Ω system, T_A = +25°C, unless otherwise noted.)

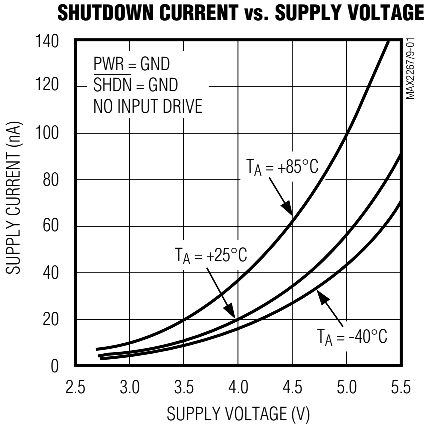
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Mode Switching Time		(Note 4)		550		ns
Turn-On Time (Notes 1, 4)		PWR = V_{CC} or GND		1	5	µs
Maximum Input VSWR	VSWR	f_{IN} = 887MHz to 925MHz, PWR = GND or V_{CC}		2.4:1		
Nonharmonic Spurious due to Load Mismatch (Notes 1, 5)		P_{IN} = +6dBm			-60	dBc
Noise Power (Note 6)		Measured at 851MHz		-137		dBm/Hz
		PWR = GND, measured at 851MHz		-130		
Harmonic Suppression		(Note 7)		32		dBc

Note 1: Minimum and maximum values are guaranteed by design and characterization, not production tested.
Note 2: P_{MAX} is met over this frequency range at the ACPR limit with a single matching network. For optimum performance at other frequencies, the output matching network must be properly designed. See the *Applications Information* section. Operation between 750MHz and 1000MHz is possible but has not been characterized.
Note 3: PAE is specified into a 50Ω load, while meeting the ACPR requirement.
Note 4: Time from logic transition until P_{OUT} is within 1dB of its final mean power.
Note 5: Murata isolator as load with 20:1 VSWR any phase angle after isolator.
Note 6: Noise power can be improved by using the circuit in Figures 1 and 2.
Note 7: Harmonics measured on the evaluation kit, which provides some harmonic attenuation in addition to the rejection provided by the IC. The combined suppression is specified.
Note 8: ≥+25°C guaranteed by production test, ≤+25°C guaranteed through correlation to worst-case temperature testing.

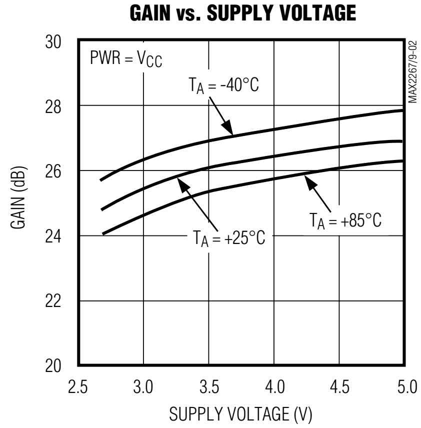
Typical Operating Characteristics

(MAX2267/MAX2268/MAX2269 EV kits, V_{CC} = +3.5V, $\overline{SHDN} = V_{CC}$, CDMA modulation, T_A = +25°C, unless otherwise noted.)

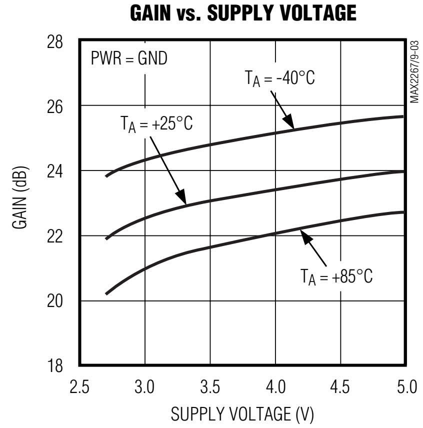
MAX2267
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



MAX2267
GAIN vs. SUPPLY VOLTAGE



MAX2267
GAIN vs. SUPPLY VOLTAGE

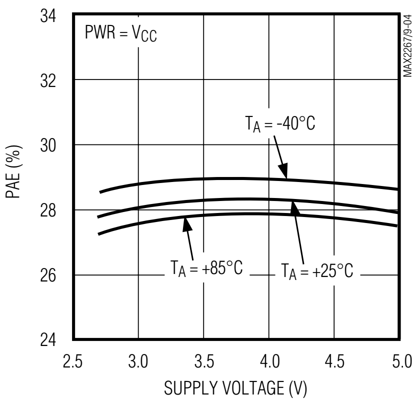


+2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

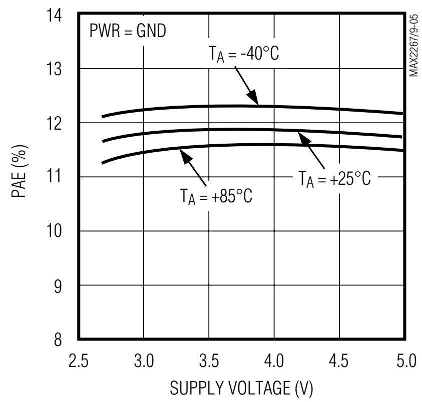
Typical Operating Characteristics (continued)

(MAX2267/MAX2268/MAX2269 EV kits, V_{CC} = +3.5V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

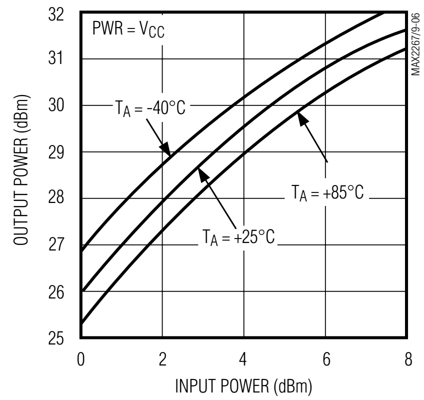
MAX2267
POWER-ADDED EFFICIENCY vs. SUPPLY VOLTAGE



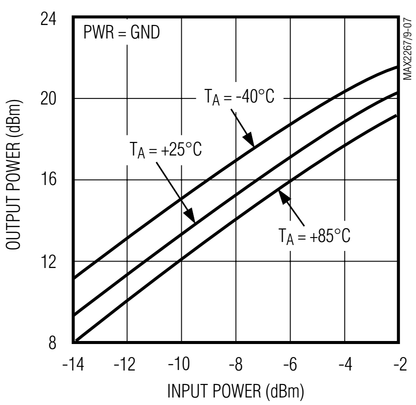
MAX2267
POWER-ADDED EFFICIENCY vs. SUPPLY VOLTAGE



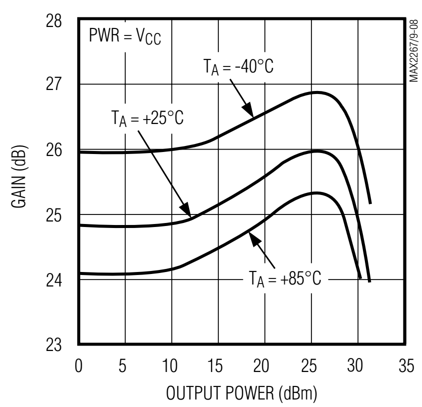
MAX2267
OUTPUT POWER vs. INPUT POWER



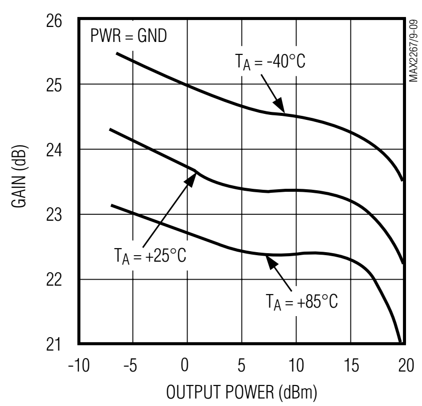
MAX2267
OUTPUT POWER vs. INPUT POWER



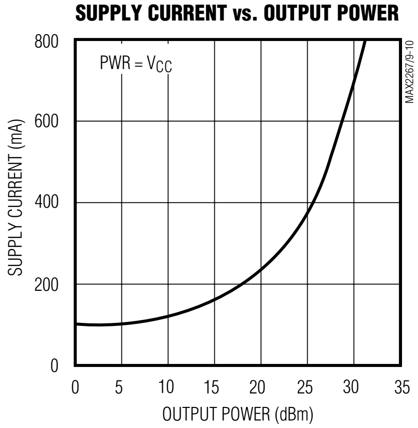
MAX2267
GAIN vs. OUTPUT POWER



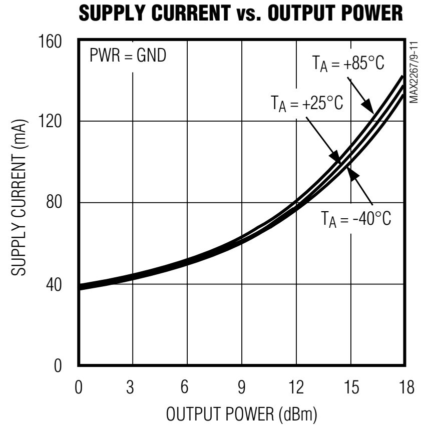
MAX2267
GAIN vs. OUTPUT POWER



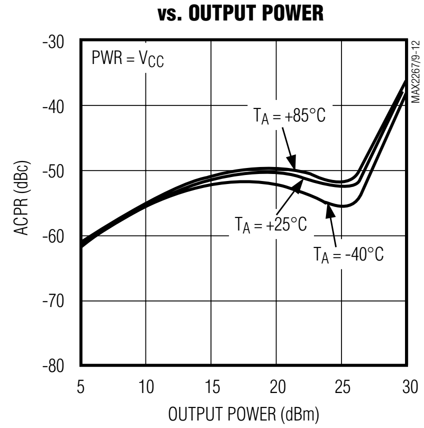
MAX2267
SUPPLY CURRENT vs. OUTPUT POWER



MAX2267
SUPPLY CURRENT vs. OUTPUT POWER



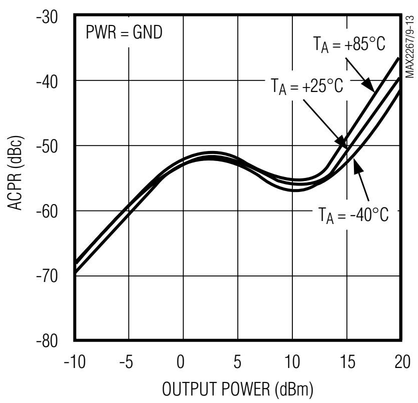
MAX2267
ADJACENT-CHANNEL POWER RATIO vs. OUTPUT POWER



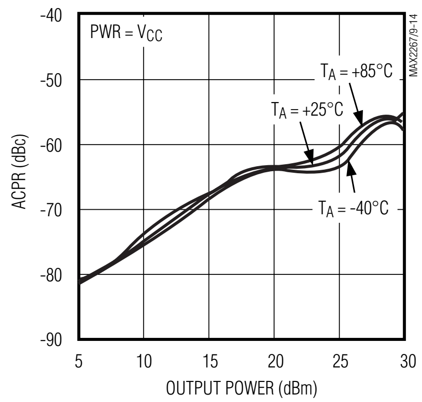
Typical Operating Characteristics (continued)

(MAX2267/MAX2268/MAX2269 EV kits, V_{CC} = +3.5V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

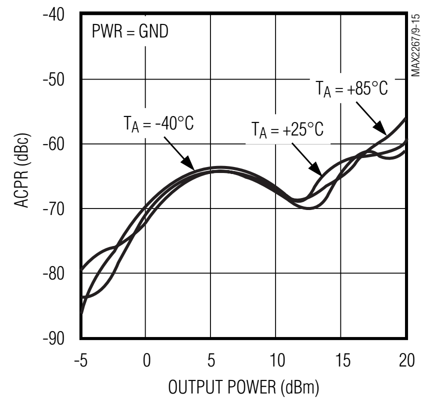
MAX2267
ADJACENT-CHANNEL POWER RATIO vs. OUTPUT POWER



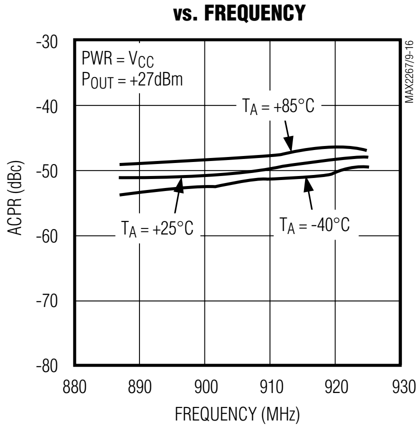
MAX2267
ALTERNATE-CHANNEL POWER RATIO vs. OUTPUT POWER



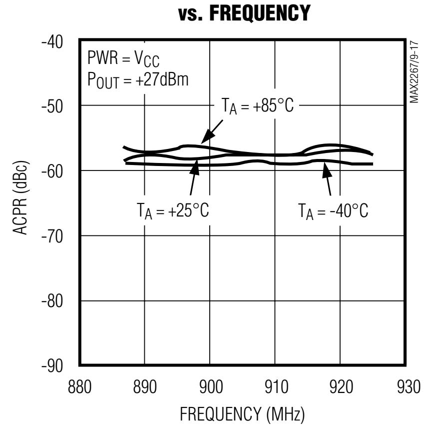
MAX2267
ALTERNATE-CHANNEL POWER RATIO vs. OUTPUT POWER



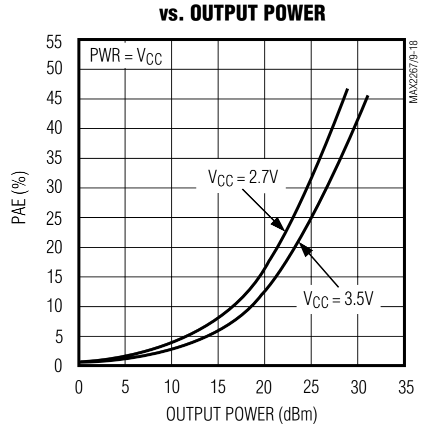
MAX2267
ADJACENT-CHANNEL POWER RATIO vs. FREQUENCY



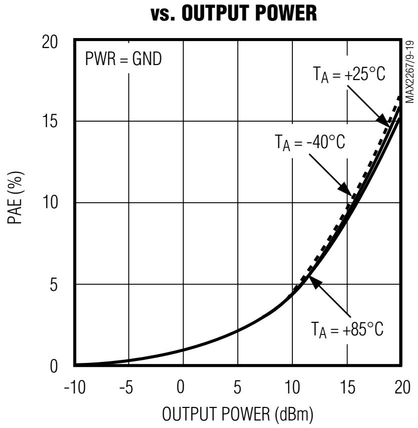
MAX2267
ALTERNATE-CHANNEL POWER RATIO vs. FREQUENCY



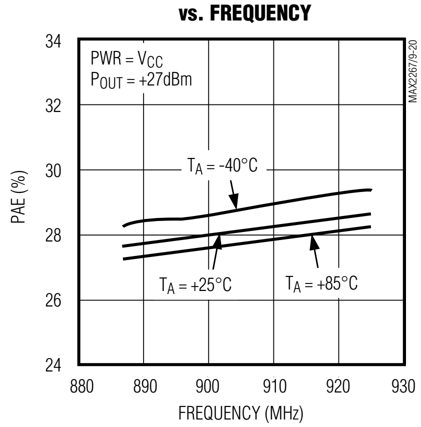
MAX2267
POWER-ADDED EFFICIENCY vs. OUTPUT POWER



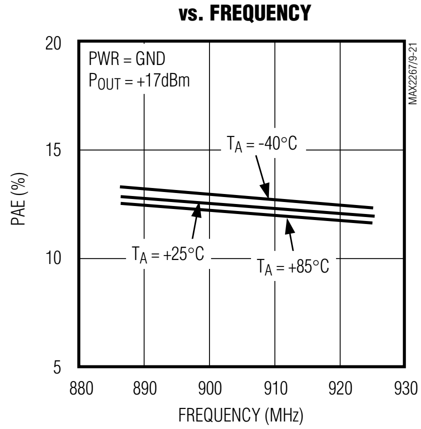
MAX2267
POWER-ADDED EFFICIENCY vs. OUTPUT POWER



MAX2267
POWER-ADDED EFFICIENCY vs. FREQUENCY



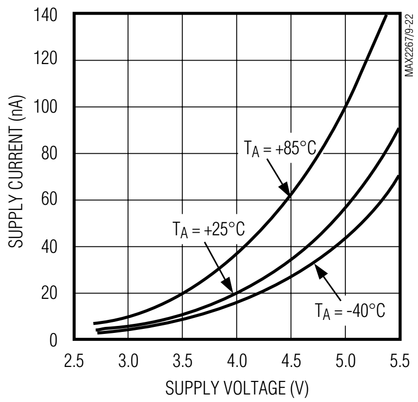
MAX2267
POWER-ADDED EFFICIENCY vs. FREQUENCY



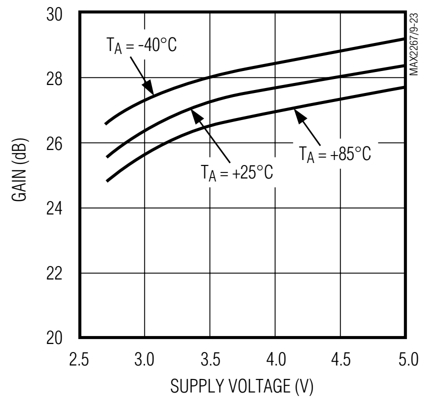
Typical Operating Characteristics (continued)

(MAX2267/MAX2268/MAX2269 EV kits, V_{CC} = +3.5V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

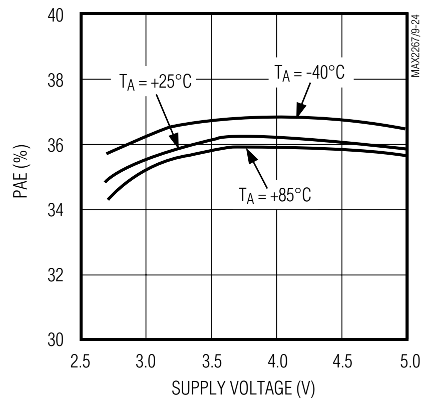
MAX2268
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



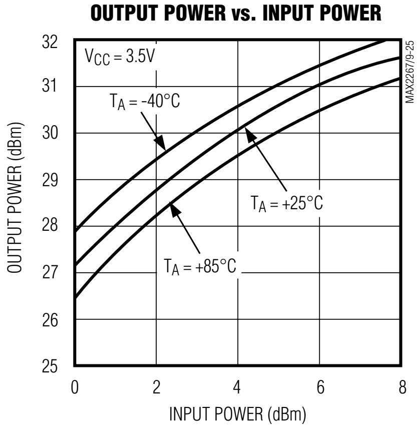
MAX2268
GAIN vs. SUPPLY VOLTAGE



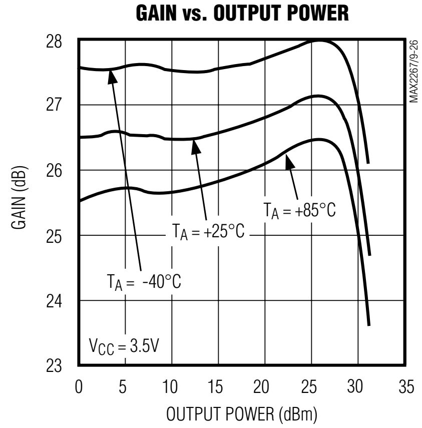
MAX2268
POWER-ADDED EFFICIENCY vs. SUPPLY VOLTAGE



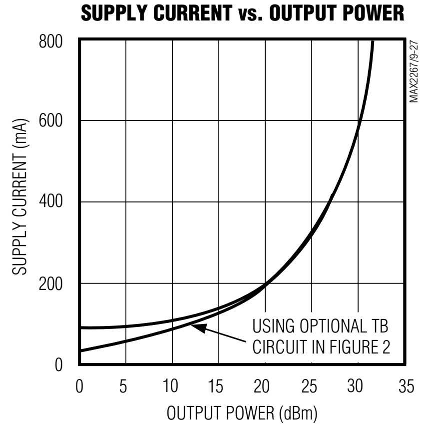
MAX2268
OUTPUT POWER vs. INPUT POWER



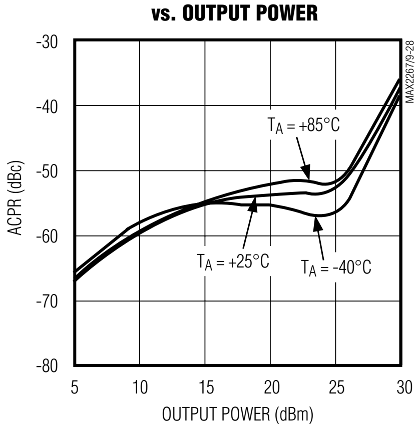
MAX2268
GAIN vs. OUTPUT POWER



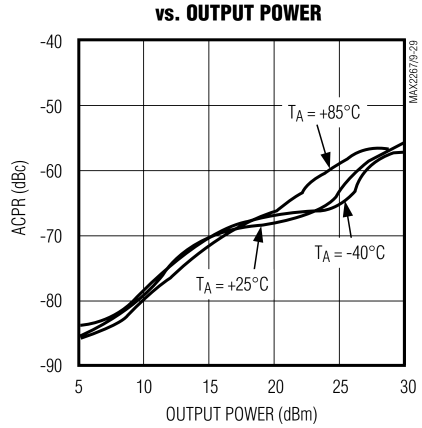
MAX2268
SUPPLY CURRENT vs. OUTPUT POWER



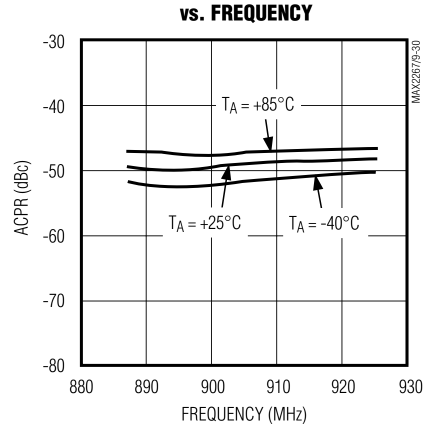
MAX2268
ADJACENT-CHANNEL POWER RATIO vs. OUTPUT POWER



MAX2268
ALTERNATE-CHANNEL POWER RATIO vs. OUTPUT POWER



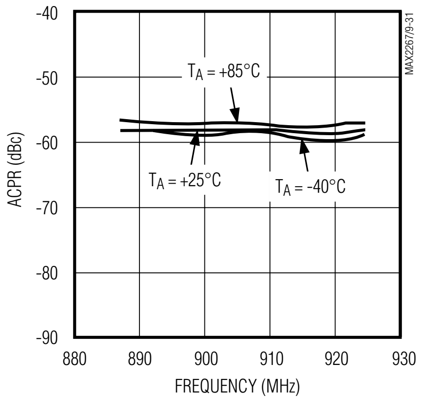
MAX2268
ADJACENT-CHANNEL POWER RATIO vs. FREQUENCY



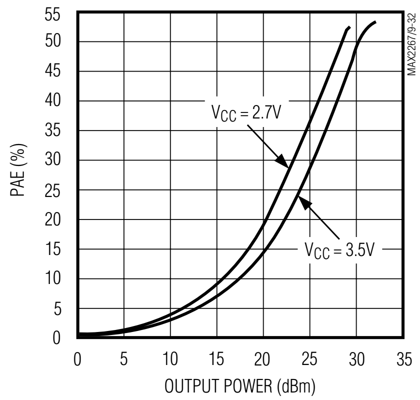
Typical Operating Characteristics (continued)

(MAX2267/MAX2268/MAX2269 EV kits, V_{CC} = +3.5V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

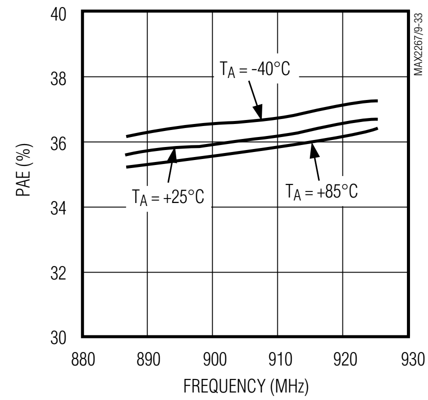
MAX2268
ALTERNATE-CHANNEL POWER RATIO vs. FREQUENCY



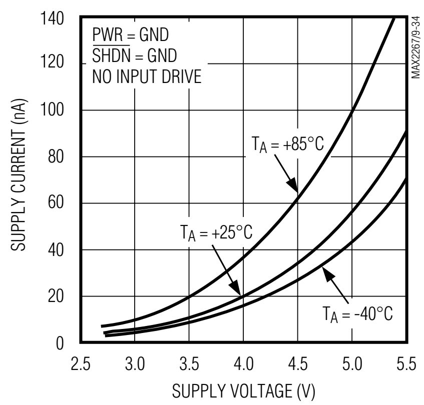
MAX2268
POWER-ADDED EFFICIENCY vs. OUTPUT POWER



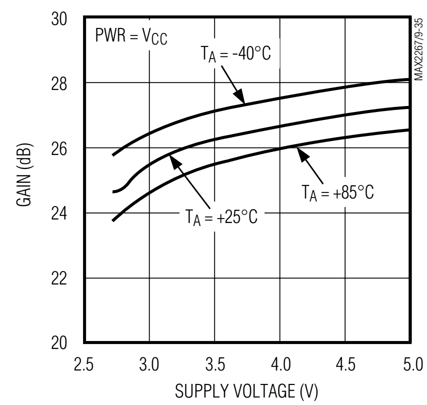
MAX2268
POWER-ADDED EFFICIENCY vs. FREQUENCY



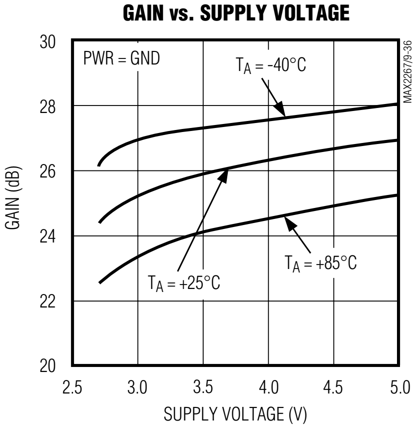
MAX2269
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



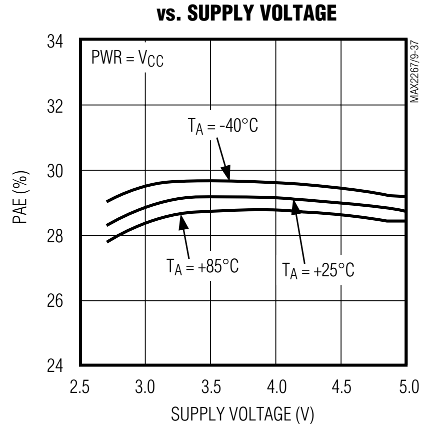
MAX2269
GAIN vs. SUPPLY VOLTAGE



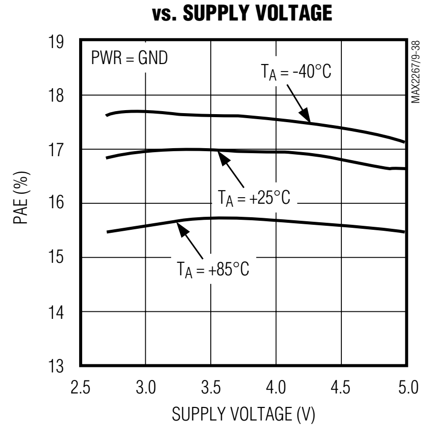
MAX2269
GAIN vs. SUPPLY VOLTAGE



MAX2269
POWER-ADDED EFFICIENCY vs. SUPPLY VOLTAGE



MAX2269
POWER-ADDED EFFICIENCY vs. SUPPLY VOLTAGE

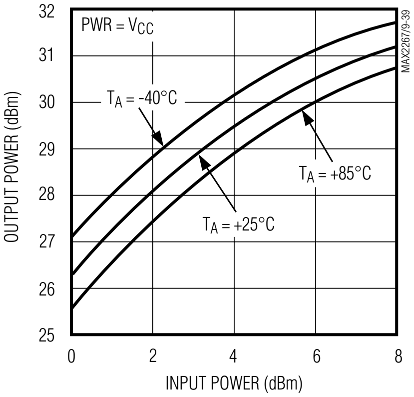


+2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

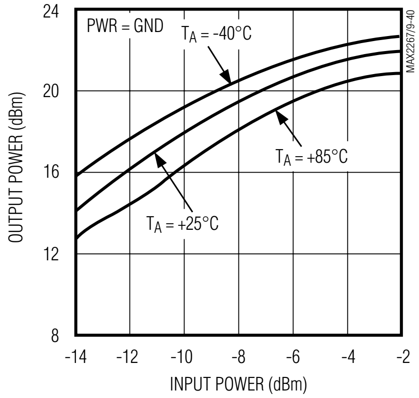
Typical Operating Characteristics (continued)

(MAX2267/MAX2268/MAX2269 EV kits, V_{CC} = +3.5V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

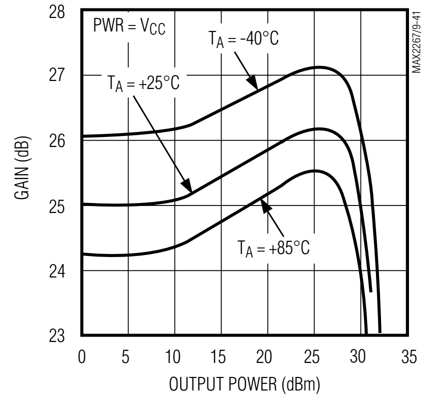
MAX2269
OUTPUT POWER vs. INPUT POWER



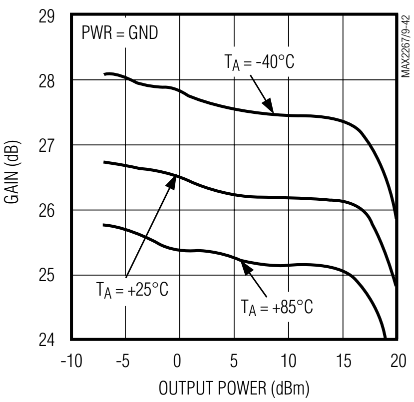
MAX2269
OUTPUT POWER vs. INPUT POWER



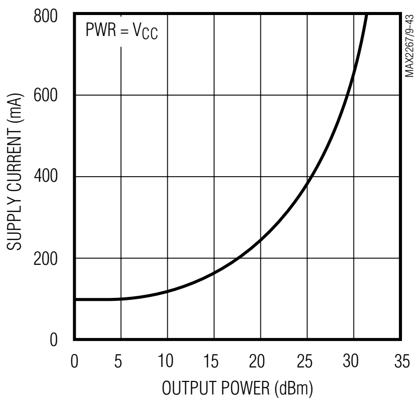
MAX2269
GAIN vs. OUTPUT POWER



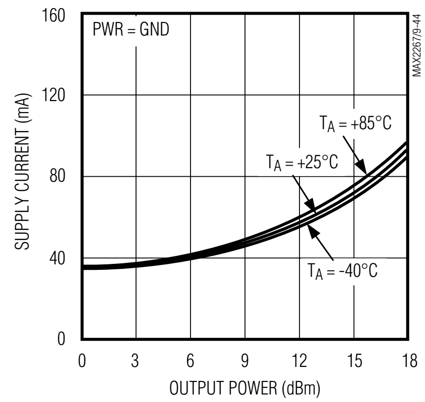
MAX2269
GAIN vs. OUTPUT POWER



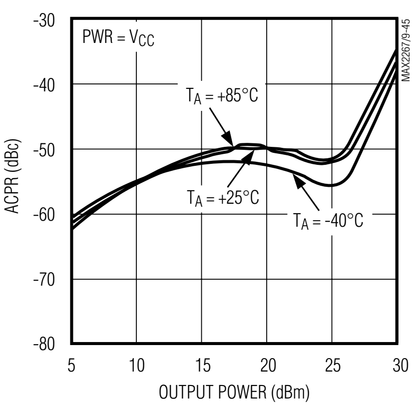
MAX2269
SUPPLY CURRENT vs. OUTPUT POWER



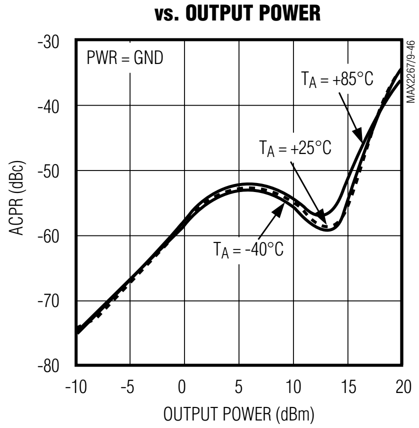
MAX2269
SUPPLY CURRENT vs. OUTPUT POWER



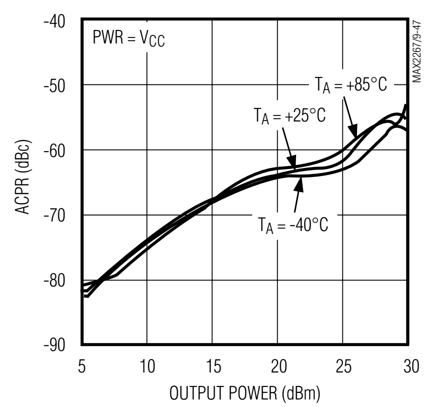
MAX2269
ADJACENT-CHANNEL POWER RATIO vs. OUTPUT POWER



MAX2269
ADJACENT-CHANNEL POWER RATIO vs. OUTPUT POWER



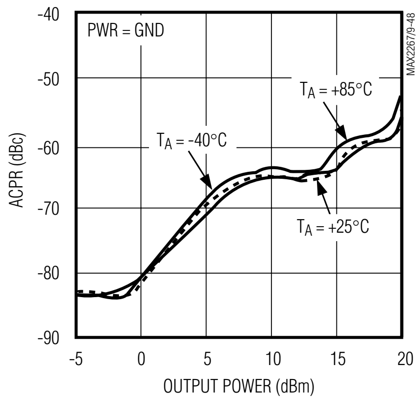
MAX2269
ALTERNATE-CHANNEL POWER RATIO vs. OUTPUT POWER



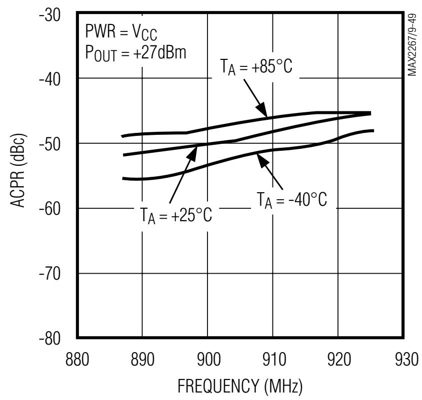
Typical Operating Characteristics (continued)

(MAX2267/MAX2268/MAX2269 EV kits, V_{CC} = +3.5V, $\overline{SHDN}$ = V_{CC}, CDMA modulation, T_A = +25°C, unless otherwise noted.)

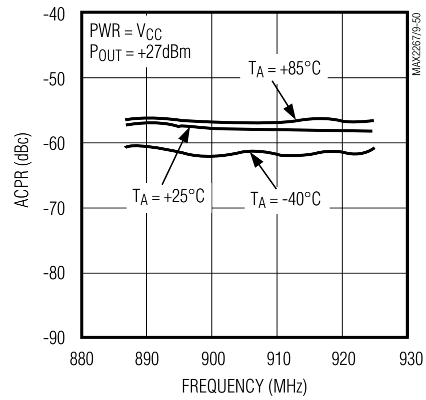
MAX2269
ALTERNATE-CHANNEL POWER RATIO
vs. OUTPUT POWER



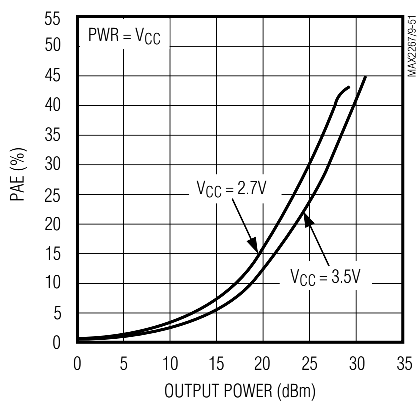
MAX2269
ADJACENT-CHANNEL POWER RATIO
vs. FREQUENCY



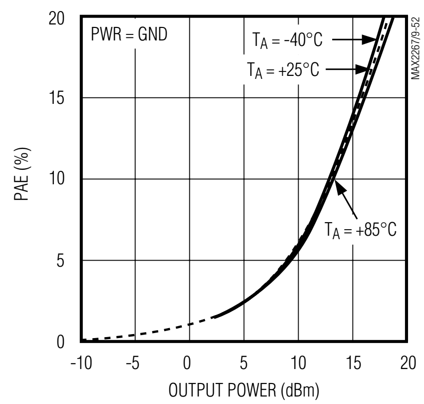
MAX2269
ALTERNATE-CHANNEL POWER RATIO
vs. FREQUENCY



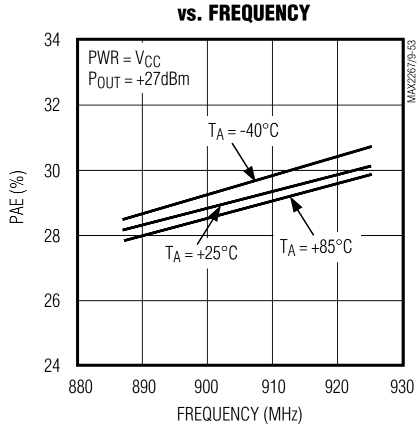
MAX2269
POWER-ADDED EFFICIENCY
vs. OUTPUT POWER



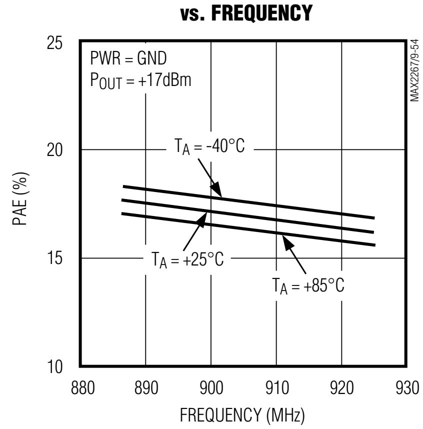
MAX2269
POWER-ADDED EFFICIENCY
vs. OUTPUT POWER



MAX2269
POWER-ADDED EFFICIENCY
vs. FREQUENCY



MAX2269
POWER-ADDED EFFICIENCY
vs. FREQUENCY



+2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

Pin Description

PIN		NAME	FUNCTION
MAX2267 MAX2269	MAX2268		
1	1	IN1	RF Input Port. Requires external matching network.
2	—	PWR	Mode-Select Input. Drive low to select the low-power mode (BIAS1L and BIAS2L). Drive high to select high-power mode (BIAS1H and BIAS2H).
3, 5, 14	3, 5	V_{CC}	Voltage Supply. It is critical to bypass these pins with capacitors to GND as close to the pins as possible.
4	4	BIAS1H	High-Power Mode First Stage Bias Control. See *General Description*.
6	2, 6	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to enable shutdown. Drive high for normal operation. On the MAX2268, make sure that both pins get driven simultaneously. To place the MAX2267 into shutdown mode, also pull the PWR pin low.
7	—	BIAS2L	Low-Power Mode Second Stage Bias Control. See *General Description*.
8, 9	8, 9	OUT1	RF Output Ports. Require an appropriate output matching network and collector bias.
10	—	BIAS1L	Low-Power Mode First Stage Bias Control. See *General Description*.
11	—	OUT0	RF Output Port. Requires an appropriate output matching network and collector bias.
12	12	NFP	Noise Filtering Pin. Connect noise filtering network as described in *Noise Filtering* section. If unused, leave open.
—	7, 10, 11, 14, 16	N.C.	Not internally connected. Do not make any connections to these pins.
13, Slug	13, Slug	GND	Ground. Solder the package slug to high-thermal-conductivity circuit board ground plane.
15	15	BIAS2H	High-Power Mode Second Stage Bias Control. See *General Description*.
16	—	IN0	RF Input Port. Requires external matching network.

Detailed Description

The MAX2267/MAX2268/MAX2269 are linear power amplifiers (PAs) intended for CDMA and TDMA applications. The devices have been fully characterized in the 887MHz to 925MHz Japanese cellular band and can be used from 750MHz to 1000MHz by adjusting the input and output match. In CDMA applications, they provide +27dBm of output power and up to 35% power-added efficiency (PAE) from a single +2.7V to +4.5V supply.

An inherent drawback of traditional PAs is that their efficiency drops rapidly with reduced output power. For example, in a PA designed for maximum efficiency at +27dBm, the efficiency at +15dBm falls well below 4.5% (over 200mA from a 3.5V supply). This behavior significantly reduces talk time in CDMA phones because over 90% of the time they are at output powers below +16dBm. The MAX2267/MAX2268/MAX2269 are optimized for lowest current draw at output powers that are most likely to occur in real-life situations. This provides up to 50% reduced average PA current.

High-Power and Low-Power Modes

The MAX2267/MAX2269 are designed to provide optimum PAE in both high- and low-power modes. For a +3.5V supply, maximum output power is +27dBm in high-power mode. In low-power mode, output power is +17dBm and +17.5dBm, respectively. Use the system's microcontroller to determine required output power, and switch between the two modes as appropriate with the PWR logic pin.

Bias Control

The bias current of the first stage in low-power mode is proportional to the current flowing out of BIAS1L. The voltage at BIAS1L is fixed by an internal bandgap reference, so the current out of this pin is inversely proportional to the value of the resistor between this pin and ground. Similarly, the bias current of the first stage in high-power mode is proportional to the current flowing out of BIAS1H. The current in the second stage is proportional to the currents out of BIAS2L and BIAS2H for low- and high-power modes, respectively.

Additionally, these resistors allow for customization of gain and alternate- and adjacent-channel power ratios. Increasing the bias current in the first stage increases the gain and improves alternate-channel power ratio at the expense of efficiency. Increasing the bias current in the second stage increases gain at the expense of efficiency as well as adjacent- and alternate-channel power ratios.

The PA bias current can be dynamically adjusted by summing a current into the bias pin of interest with an external source such as a DAC. See the MAX2268 *Typical Application Circuit* for using a voltage DAC and current setting resistors RTB1 and RTB2. Choosing RTB1 = R1 and RTB2 = R2 allows current adjustment between 0mA to double the nominal idle current with DAC voltages between 0V and 2.4V. The DAC must be able to source approximately 100µA.

Shutdown Mode

Pull pins 2 and 6 low to place the MAX2267/MAX2268/MAX2269 into shutdown mode. In this mode, all gain stages are disabled and supply current drops to 0.5µA.

Applications Information

Increasing Efficiency

The MAX2269 incorporates an additional external switch to increase efficiency to 17% at +17dBm and to 29% at +27dBm. This increase in efficiency is mainly due to the additional isolation between the high- and low-power outputs provided by the external switch.

External Components

The MAX2267/MAX2268/MAX2269 require matching circuits at their inputs and outputs for operation in a 50Ω system. The simplified application circuits in Figures 1, 2, and 3 describe the topology of the circuit-

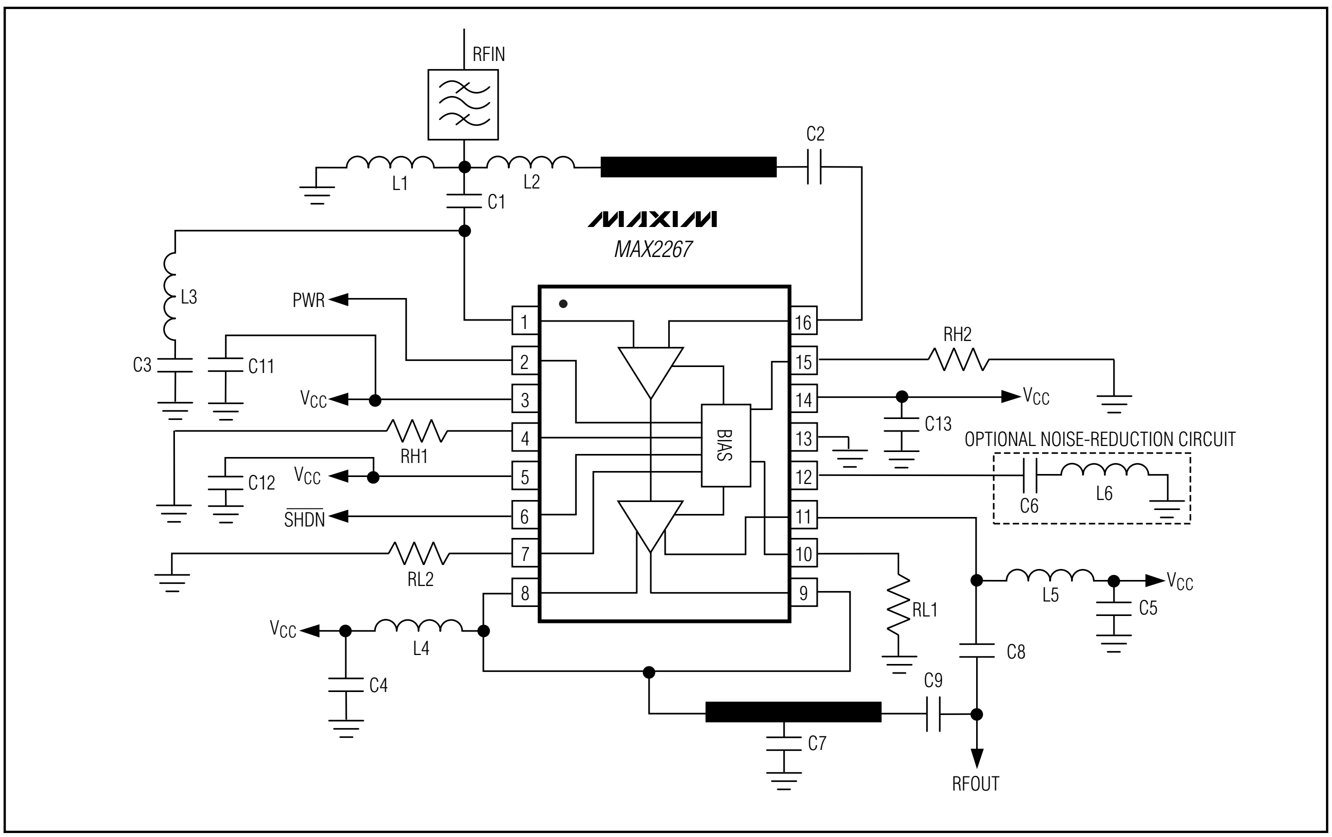


Figure 1. MAX2267 Typical Application Circuit

+2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

ry for each device. For more detailed circuit diagrams, refer to the MAX2267/MAX2268/MAX2269 EV kit manual. The EV kit manual suggests component values that are optimized for best simultaneous efficiency and return loss performance. Use high-quality components in these matching circuits for greatest efficiency.

Layout and Power-Supply Bypassing

A properly designed PC board is essential to any RF/microwave circuit. Be sure to use controlled impedance lines on all high-frequency inputs and outputs. Proper grounding of the GND pins is fundamental; if the PC board uses a topside RF ground, connect all GND pins (especially the TSSOP package exposed GND pad) directly to it. On boards where the ground plane is not on the component side, it's best to connect all GND pins to the ground plane with plated through-holes close to the package.

To minimize coupling between different sections of the system, the ideal power-supply layout is a star configuration with a large decoupling capacitor at a central V_{CC} node. The V_{CC} traces branch out from this central node, each leading to a separate V_{CC} node on the PC board. A second bypass capacitor with low ESR at the RF frequency of operation is located at the end of each trace. This arrangement provides local decoupling at the V_{CC} pin.

Input and output impedance-matching networks are very sensitive to layout-related parasitics. It is important to keep all matching components as close to the IC as possible to minimize the effects of stray inductance and stray capacitance of PC board traces.

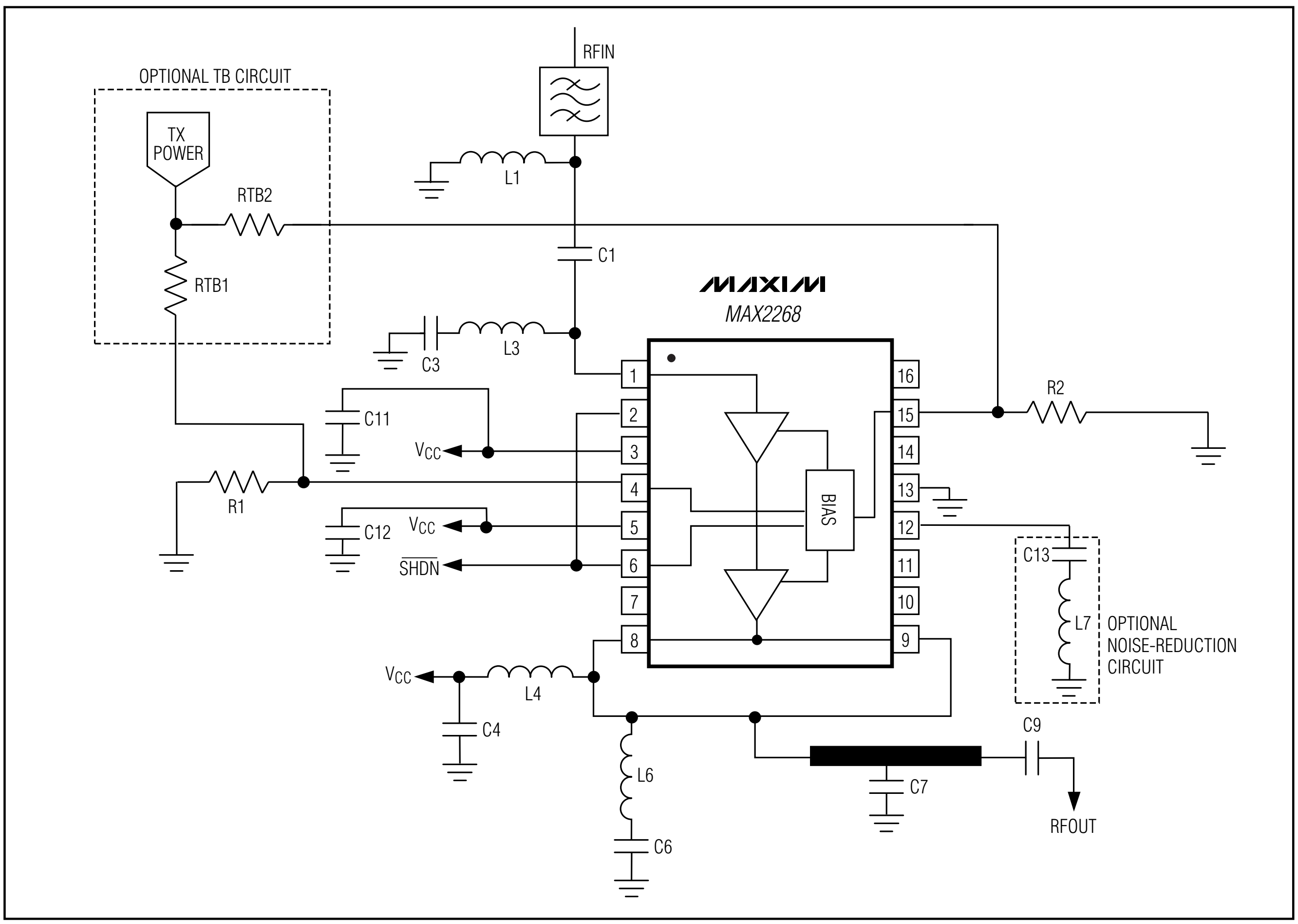


Figure 2. MAX2268 Typical Application Circuit

Noise Filtering

For improved noise performance, the MAX2267/MAX2268/MAX2269 allow for additional noise filtering for further suppression of transmit noise. Use the recommended component values in the MAX2267/MAX2268/MAX2269 EV kit manual for optimal noise power.

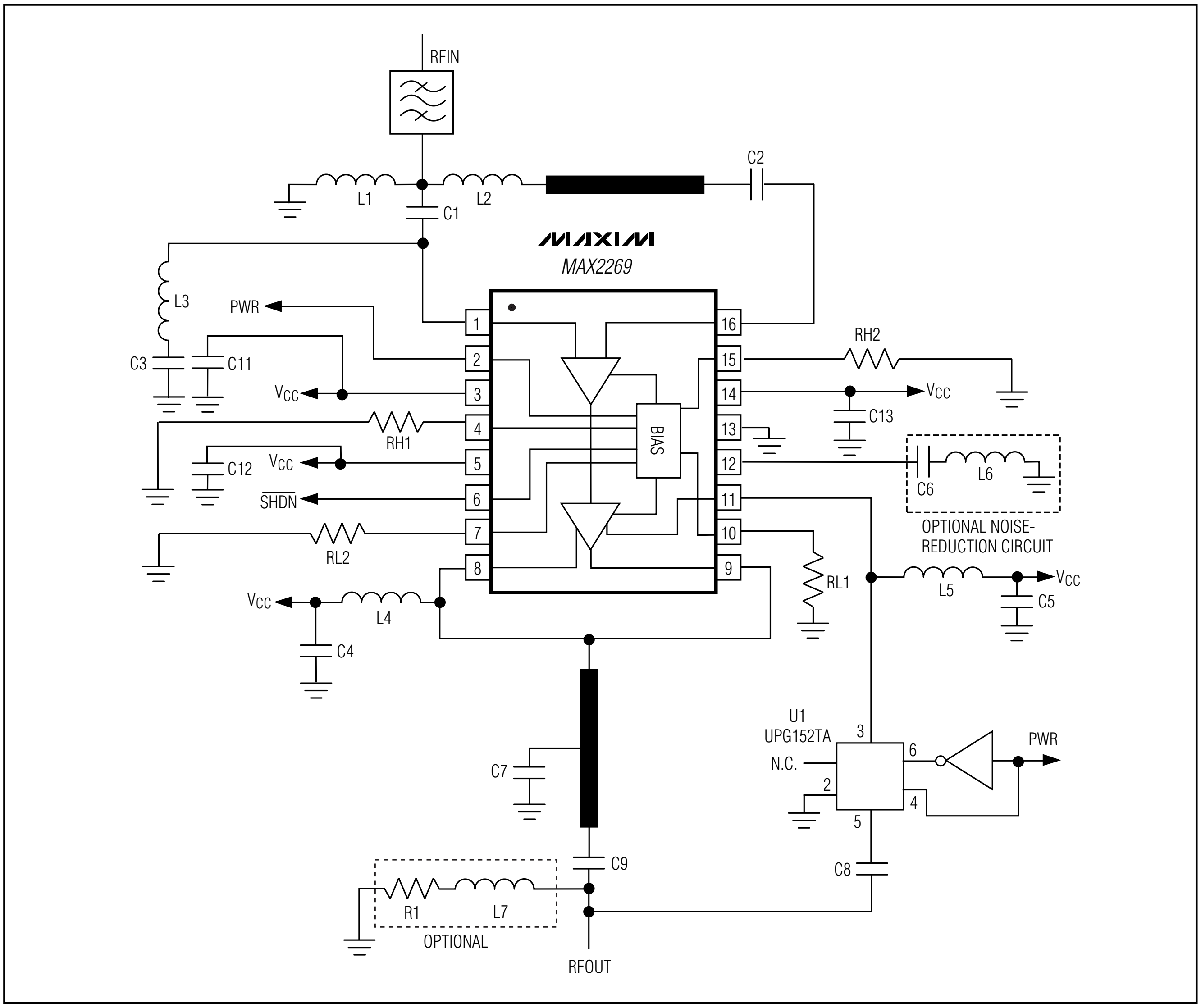
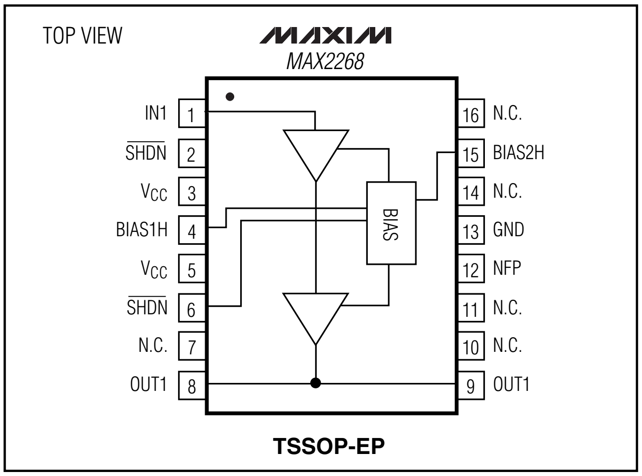


Figure 3. MAX2269 Typical Application Circuit

+2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

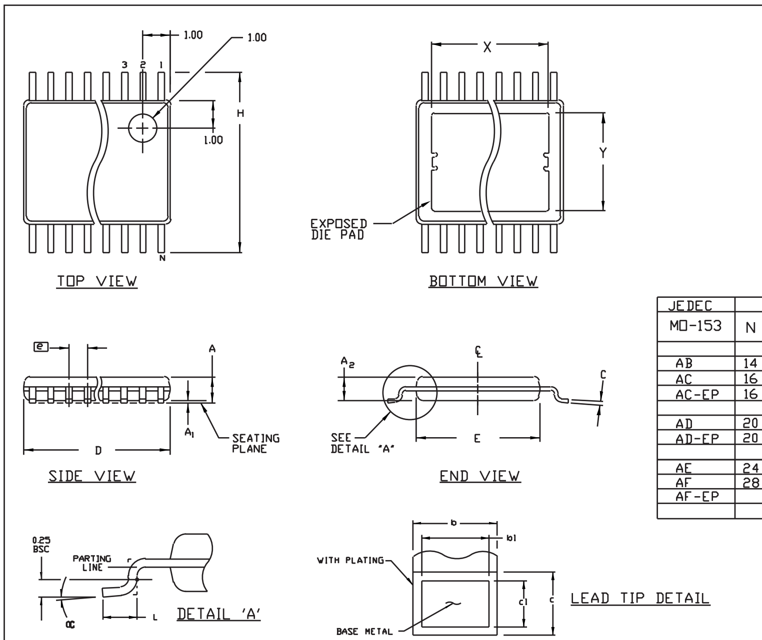
Pin Configurations/ Functional Diagrams (continued)



Chip Information

TRANSISTOR COUNT: 1256

Package Information



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.
5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV C | 1/1

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