High-Performance DrMOS

6 mm x 6 mm x 0.8 mm IQFN

TDA21220

Data Sheet

Revision 1.9, 2011-03-31
Preliminary

Industry and Multi Market

Edition 2011-03-31

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.9, 2011-03-31	
All	Update format of document.
Table 6	Define the AC values.
Figure 1	Update the package picture
Table 14	Correct a typo on logic function of SMOD pin
Figure 9	Clarify the definition of T_GHtsshd and T_GLtsshd
Table 11	Update the Toff_min_PWM to min 65ns

1 Applications

- Desktop and Server VR11.X and VR12 Vcore and non-Vcore buck-converter
- Network and Telecom processor VR
- Single Phase and Multiphase POL
- CPU/GPU Regulation in Notebook, Desktop Graphics Cards, DDR Memory, Graphic Memory
- High Power Density Voltage Regulator Modules (VRM).

2 Features

- Compliant to Intel® VR12 Driver and Mosfets Module (DrMOS) for Desktop/Server Applications
- For synchronous Buck step down voltage applications
- Maximum average current of 50 A
- Input voltage range +4.5 V to +16 V
- Power MOSFETs rated 25 V for safe operation under all conditions
- Extremely fast switching technology for improved performance at high switching frequencies (> 1 MHz)
- Remote driver disable function
- Switch modulation (SMOD#) of low side MOSFET
- Includes bootstrap diode
- Shoot through protection
- +5 V High and Low Side driving voltage
- Compatible to standard +3.3 V PWM controller integrated circuits
- Three-state PWM input functionality
- Small package: IQFN40 (6 x 6 x 0.8 mm³)
- RoHS compliant

Table 1 Product Identification

Part Number	Temp Range	Package	Marking
TDA21220	-25 to 125°C	6 x 6 x 0.8 mm³ PG-IQFN-40-1	TDA21220

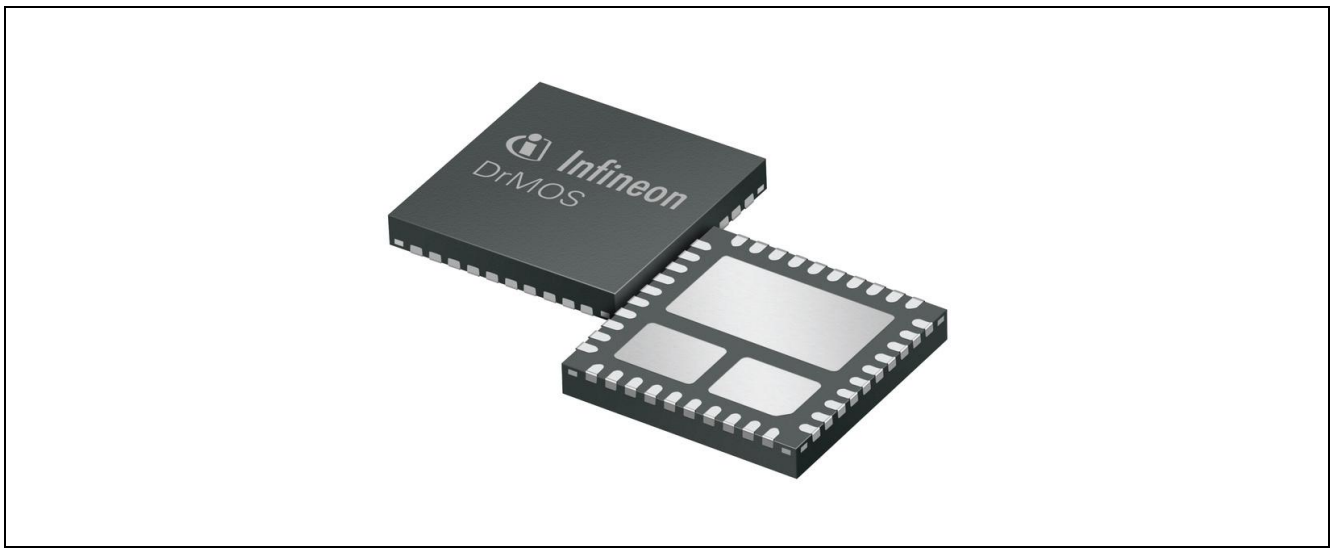


Figure 1 Picture of the Product

3 Description

3.1 Pinout

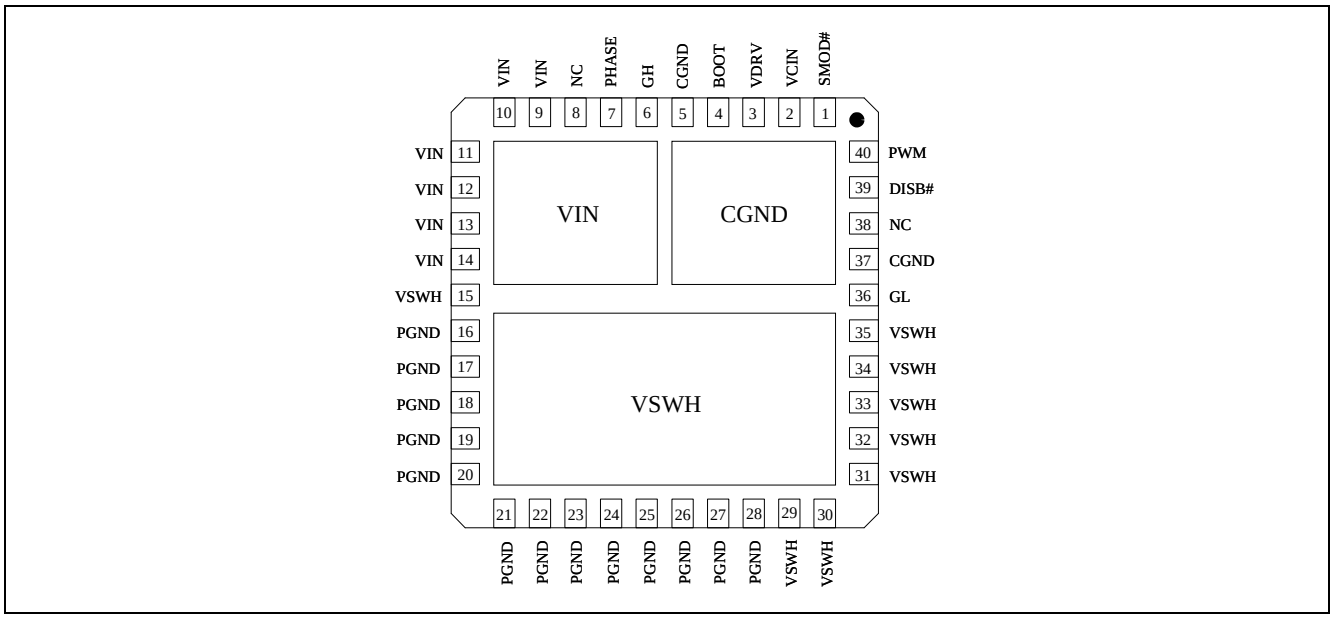


Figure 2 Pinout, Numbering and Name of Pins (transparent top view)

Note: Signals marked with "#" at the end are active low signals.

Table 2 I/O Signals

Pin No.	Name	Pin Type	Buffer Type	Function
1	SMOD#	I	+3.3 V logic	**High and Low Side gate disable** When SMOD# is "low" the GL is "off"
6	GH	O	Analog	**High side gate signal** Monitoring of High Side MOSFET gate
7	PHASE	O	Analog	**Switch node output** Internally connected to VSWH pin, Connect to BOOT capacitor
4	BOOT	I	Analog	**Bootstrap voltage pin** Connect to BOOT capacitor
15, 29 to 35, VSWH pad	VSWH	O	Analog	**Switch node output** High current output switching node
36	GL	O	Analog	**Low side gate signal** Monitoring of Low Side MOSFET gate
39	DISB#	I	+3.3 V logic	**Disable signal (active low)** Pull to GND to disable the IC.
40	PWM	I	+3.3 V logic	**PWM drive logic input** The three state PWM input is compatible with 3.3 V.

Table 3 Power Supply

Pin No.	Name	Pin Type	Buffer Type	Function
2	VCIN	POWER	–	**Logic supply voltage** 5 V bias voltage for the internal logic
3	VDRV	POWER	–	**FET gate supply voltage** High and Low Side gate drive 5 V supply
9 to 14, Vin pad	VIN	POWER	–	**Input voltage** Supply of the drain of the High Side MOSFET

Table 4 Ground Pins

Pin No.	Name	Pin Type	Buffer Type	Function
5, 37, CGND pad	CGND	GND	–	**Control signal ground** Should be connected to PGND externally
16 to 28	PGND	GND	–	**Power ground** All these pins must be connected to the power GND plane through multiple low inductance vias.

Table 5 Not Connected

Pin No.	Name	Pin Type	Buffer Type	Function
8, 38	NC	–	–	**No internal connection** Leave pin floating or tie to GND.

3.2 General Description

The Infineon TDA21220 is a multichip module that incorporates Infineon's premier MOSFET technology for a single high side and a single low side MOSFET coupled with a robust, high performance, high switching frequency gate driver in a single 40 pin QFN package. The optimized gate timing allows for significant light load efficiency improvements over discrete solutions. State of the art MOSFET technology provides exceptional full load performance. Thus this device has a clear advantage over existing approaches in the marketplace when both full load and light load efficiencies are important.

When combined with the Infineon's Primarion™ Controller Family of Digital Multi-phase Controllers, the TDA21220 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications.

The TDA21220 is pin to pin compatible and compliant with the Intel 6x6 DrMOS specification. The device package height is only 0.8 mm, and is an excellent choice for applications with critical height limitations.

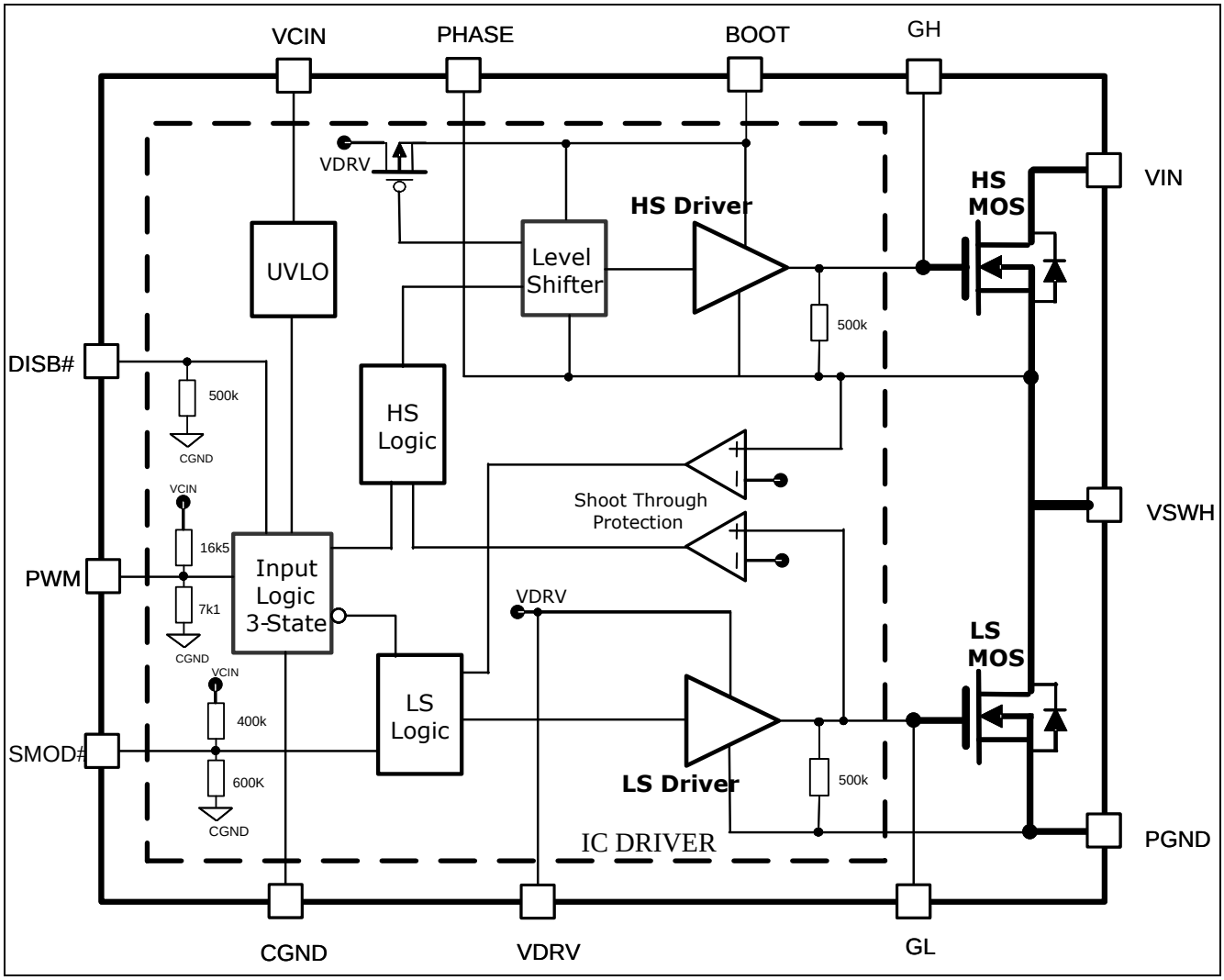


Figure 3 Simplified Block Diagram

4 Electrical Specification

4.1 Absolute Maximum Ratings

Note: T_A = 25°C

Stresses above those listed in **Table 6** "Absolute Maximum Ratings" may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure to the absolute maximum ratings for extended periods may adversely affect the operation and reliability of the device.

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency of the PWM input	f_{SW}	–	–	1.2	MHz	–
Maximum average load current	I_{OUT}	–	–	50	A	–
Input Voltage	V_{IN} (DC)	-0.30	–	25	V	–
Logic supply voltage	V_{CIN} (DC)	-0.30	–	6.5	V	–
High and Low side driver voltage	V_{DRV} (DC)	-0.30	–	6.5	V	–
Switch node voltage	V_{SWH} (DC)	-1	–	25	V	–
	V_{SWH} (AC)	-10[1]	–	25	V	–
PHASE node voltage	V_{PHASE} (DC)	-1	–	25	V	–
	V_{PHASE} (AC)	-10	–	25	V	–
BOOT voltage	V_{BOOT} (DC)	-0.3	–	31.5	V	–
	V_{BOOT} (AC)	-1[1]	–	31.5	V	–
	$V_{BOOT-PHASE}$ (DC)	-1	–	6.5	V	–
SMOD# voltage	$V_{SMOD\#}$ (DC)	-0.3	–	5.5	V	–
DISB# voltage	V_{DISB}[2]	-0.3	–	5.5	V	–
PWM voltage	V_{PWM}[2]	-0.3	–	5.5	V	–
Junction temperature	T_{Jmax}	-40	–	150	°C	–
Storage temperature	T_{STG}	-55	–	150	°C	–

Note: All rated voltages are relative to voltages on the CGND and PGND pins unless otherwise specified.

[1] AC is limited to 10 ns

[2] Latch Up class II- Level B (Jedec 78). Please refer to Quality Report for details.

4.2 Thermal Characteristics

Table 7 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-soldering point[1]	θ_{JS}	–	5	–	K/W	–
Thermal resistance, junction-top of package	θ_{Jtop}	–	20	–		–

4.3 Recommended Operating Conditions and Electrical Characteristics

Note: V_{DRV} = V_{CIN} = 5 V, T_At = 25°C

Table 8 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	5	–	16	V	–
MOSFET driver voltage	V_{DRV}	4.5	5	6		–
Logic supply voltage	V_{CIN}	4.5	5	6		–
Junction temperature	T_{jOP}	-25	–	+125	°C	–

Table 9 Voltage Supply And Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Driver current	I_{VDRV_300kHz}	–	10	–	mA	DISB# = 5 V, f_{SW} = 300 kHz
	I_{VDRV_PWML}	–	25	–	µA	DISB# = 5 V, PWM = 0 V
IC current (control)	I_{VCIN_PWML}	–	400	–		DISB# = 5 V, PWM = 0 V SMOD# = Open
	I_{VCIN_O}	–	500	–		DISB# = 5 V, PWM = Open SMOD# = Open
IC quiescent	I_{CIN}+I_{DRV}	–	–	550		DISB# = 0 V
UVLO rising	V_{UVLO_R}	2.9	3.5	3.9	V	VCIN rising
UVLO falling	V_{UVLO_F}	2.5	3.1	3.3		VCIN falling

[1] The junction-soldering point is referred to the VSWH bottom exposed pad.

Table 10 Logic Inputs And Threshold

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DISB#	Input low	V_{DISB_L}	0.7	1.1	1.3	V	V_{DISB} falling
	Input high	V_{DISB_H}	1.9	2.1	2.4		V_{DISB} rising
	Sink current	I_{DISB}	–	2	–	µA	V_{DISB} = 1 V
SMOD#	Input low	$V_{SMOD\#\_L}$	0.7	1.1	1.3	V	$V_{SMOD\#}$ falling
	Input high	$V_{SMOD\#\_H}$	1.9	2.1	2.4		$V_{SMOD\#}$ rising
	Open voltage	$V_{SMOD\#\_O}$	–	3.0	–		–
	Sink current	$I_{SMOD\#}$	–	-8	–	µA	$V_{SMOD\#}$ = 1 V
PWM	Input low	V_{PWM_L}	–	–	0.7	V	V_{PWM} falling
	Input high	V_{PWM_H}	2.4	–	–		V_{PWM} rising
	Input resistance	$R_{IN\text{-}PWM}$	3	5	7	kΩ	V_{PWM} = 1 V
	Open voltage	V_{PWM_O}	–	1.5	–	V	V_{PWM_O}
	Tristate shutdown window[1]	V_{PWM_S}	1.2	–	1.9		–

Table 11 Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Three State to GL/GH rising delay	T_pts	–	15	–	ns	GH, GL unloaded
GL Shutdown Hold-Off time	T_GLtsshd	–	150	–		
GH Shutdown Hold-Off time	T_GHtsshd	–	85	–		
GH Turn-on propagation delay	T_pdhu	–	15	–		
GH Turn-off propagation delay	T_pdlu	–	20	–		
GL Turn-on propagation delay	T_pdhl	–	20	–		
GL Turn-off propagation delay	T_pdll	–	10	–		
DISB# Turn-off propagation delay falling	T_pdl_DISB	–	20	–		
DISB# Turn-on propagation delay rising	T_pdh_DISB	–	20	–		
PWM minimum pulse width high side	Ton_min_PWM	–	25	–		
PWM minimum off time	Toff_min_PWM	65	–	–		

[1] Maximum voltage range for tri-state

5 Theory of Operation

The TDA21220 incorporates a high performance gate driver, one high-side power MOSFET and one low-side power MOSFET in a single 40 lead QFN package. The advantages of this arrangement are found in the areas of increased performance, increased efficiency and lower overall package and layout inductance.This module is ideal for use in Synchronous Buck Regulators either as a stand-alone power stage that can deliver up to 50 A or with an interleaved approach for higher current loads.

The power MOSFETs are tailored for this device. The gate driver is a robust high-performance driver rated at the switching node for DC voltages ranging from -1 V to +25 V. The closely coupled driver and MOSFETs enable efficiency improvements that are hard to match using discrete components. The power density for transmitted power of this approach is approximately 40 W within a 36 mm^2 area.

5.1 Driver Characteristics

The gate driver of the TDA21220 has 2 voltage inputs, VCIN and VDRV. VCIN is the 5 V logic supply for the driver. VDRV is also 5 V and is used to drive the High and Low Side MOSFETs. Ceramic capacitors should be placed very close to these input voltage pins to decouple the sensitive control circuitry from a noisy environment.

The MOSFETs selected for this application are optimized for 5 V gate drive, thus giving the end user optimized high load as well as light load efficiency. The reference for the power circuitry including the driver output stage is PGND and the reference for the gate driver control circuit (VCIN) is CGND.

Referring to the Block Diagram page, VCIN is internally connected to the UVLO circuit and for VCIN voltages less than required for proper circuit operation will provide shut-down. VDRV supplies both, the floating high side drive and the low-side drive circuits. An active boot circuit for the high side gate drive is also included. A second UVLO circuitry, sensing the BOOT voltage level, is implemented to prevent false GH turn on during insufficient power supply level condition (BOOT Cap charging/discharging sequence). During undervoltage both GH and GL are driven low actively; further passive pull-down (500 kΩ) is placed across gate-source of both FETs.

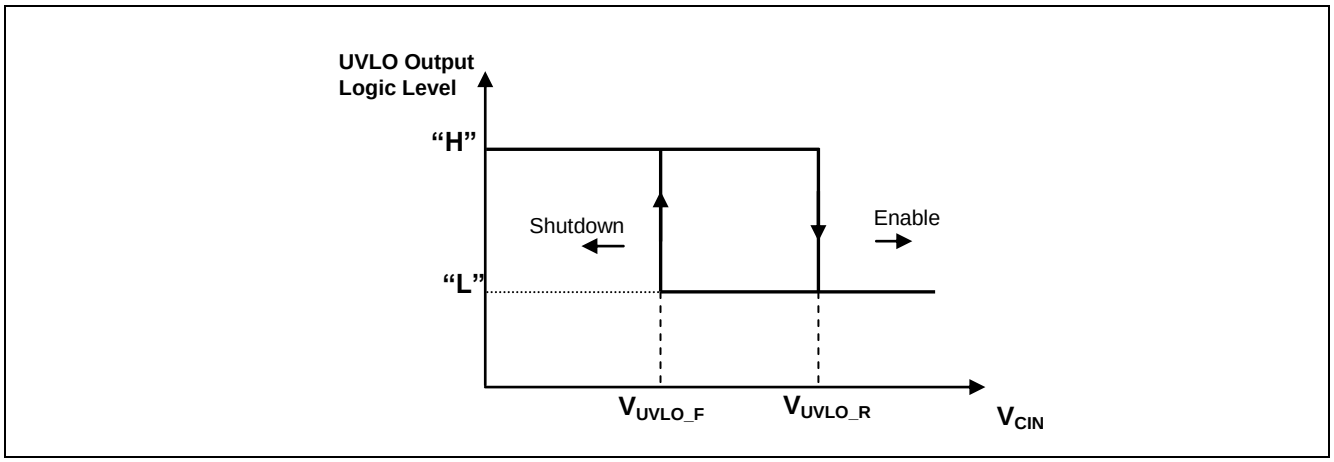


Figure 4 Internal Output Signal from UVLO Unit

5.2 Inputs to the Internal Control Circuits

The **PWM** is the control input to the IC from an external PWM controller and is compatible with 3.3 V.

The PWM input has three-state functionality. When the voltage remains in the specified PWM-shutdown-window for at least the PWM-shutdown-holdoff time T_tsshd, the operation will be suspended by keeping both MOSFET gate outputs low. Once left open, the pin is internally fixed to V_{PWM_O} = 1.5 V level.

Table 12 PWM Pin Functionality

PWM logic level	Driver output
Low	GL= High, GH = Low
High	GL = Low, GH = High
Open (left floating, or High impedance)	GL = Low, GH = Low

The possibility to use a wide range of VCIN power supply voltages (from 4.5 V to 5.5 V) implies a shifting in the threshold voltages for the following parameters: V_{PMW_O}, V_{PWM_H}, V_{PWM_L}. The typical behavior of these thresholds with the VCIN power supply is shown in the following graph:

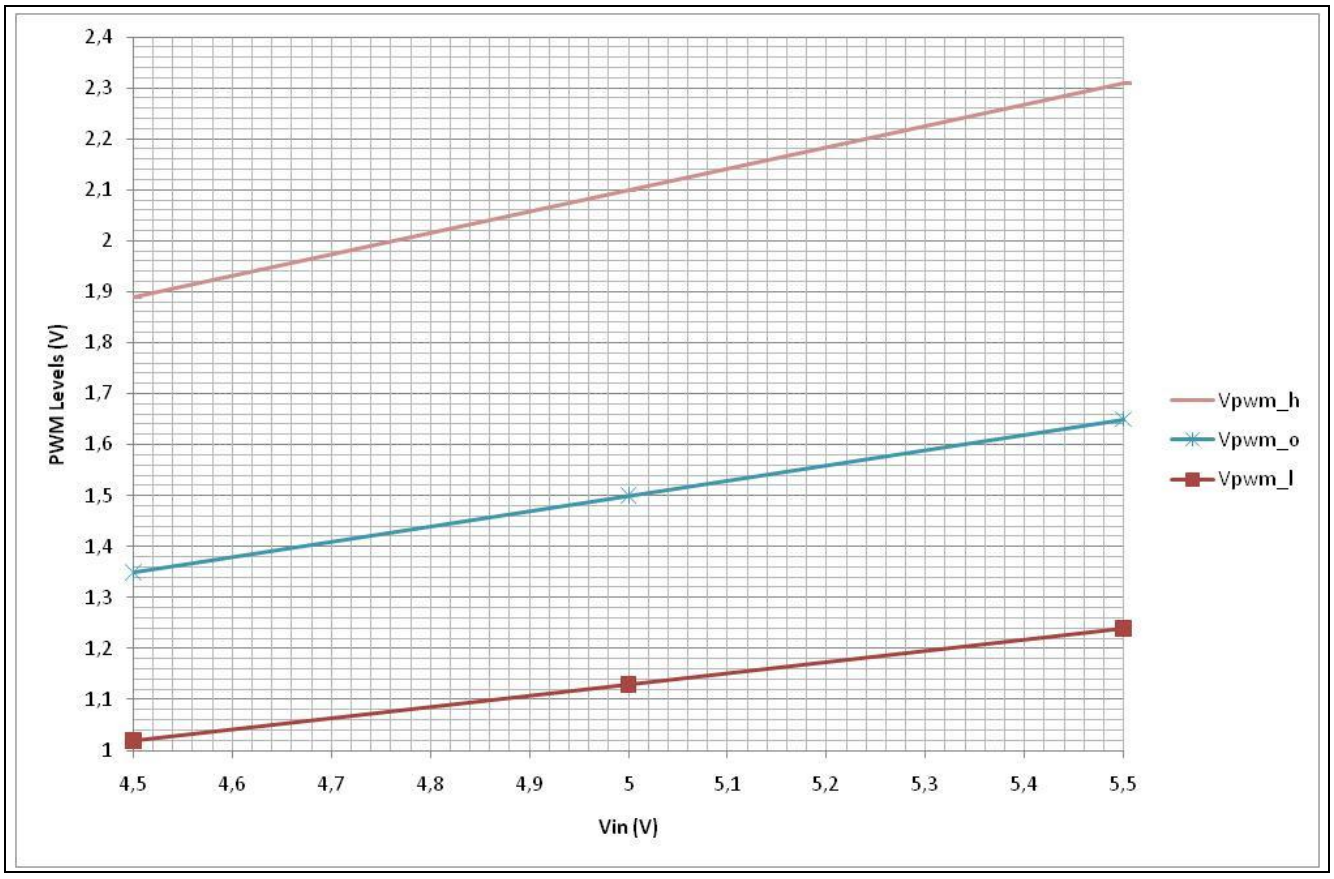


Figure 5 Variation of PWM Levels versus VCIN Logic Supply Voltage

Attention: The VPWM_S also scales in the same way.

The **DISB#** is an active low signal. When DISB# is pulled low, the power stage is disabled. The disable pin is pulled down also during the thermal shut down condition.

Table 13 DISB# Pin Functionality

DISB# logic level	Driver output
Low	Shutdown : GL = GH = Low
High	Enable : GL = GH = Active
Open (left floating, or High impedance)	Shutdown : GL = GH = Low

The **SMOD#** feature is provided to disable the low sides MOSFET during active operation. When synchronized with the PWM signal, **SMOD#** intended to improve light load efficiency by saving the gate charge loss of the low-side MOSFET. Once left open, the pin is internally fixed to $V_{SMOD\#\_O}$ =3 V level.

Table 14 SMOD# Pin Functionality

SMOD# logic level	Driver output
Low	Shutdown : GL = Low GH = PWM
High	Enable : GL = GH = Active
Open (left floating, or High impedance)	Enable : GL = GH = Active

5.3 Shoot Through Protection

The TDA21220 driver includes gate drive functionality to protect against shoot through. In order to protect the power stage from overlap, both High Side and Low Side MOSFETs being on at the same time, the adaptive control circuitry monitors the voltage at the “VSWH” pin. When the PWM signal goes low, the High Side MOSFET will begin to turn off, after the propagation delay (T_pdlu). Once the “VSWH” pin falls below 1 V, the Low Side MOSFET is gated on after the predefined delay time, (T_pdhl). Additionally, the gate to source voltage of the High Side MOSFET is also monitored. When VGS(High Side) is discharged below 1 V, a threshold known to turn High Side MOSFET off, a secondary delay is initiated, (T_pdhl), which results in Low Side being gated “ON” irregardless of the state of the “VSWH” pin.This way it will be ensured that the converter can sink current efficiently and the bootstrap capacitor will be refreshed appropriately during each switching cycle. See **Figure 9** for more detail.

GH and GL are monitoring pins to check the internal gate drive signals.

5.4 Safe Operating Area

The maximum load current versus the temperature of the PCB (below the device) is given below:

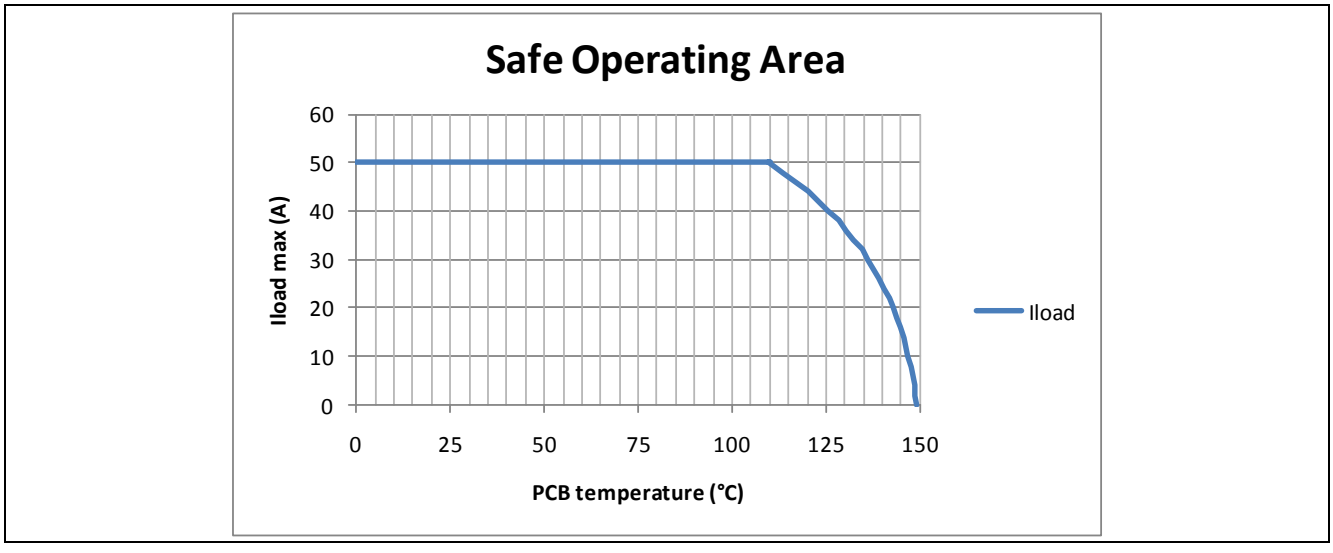


Figure 6 Safe Operating Area

6 Application

6.1 Implementation

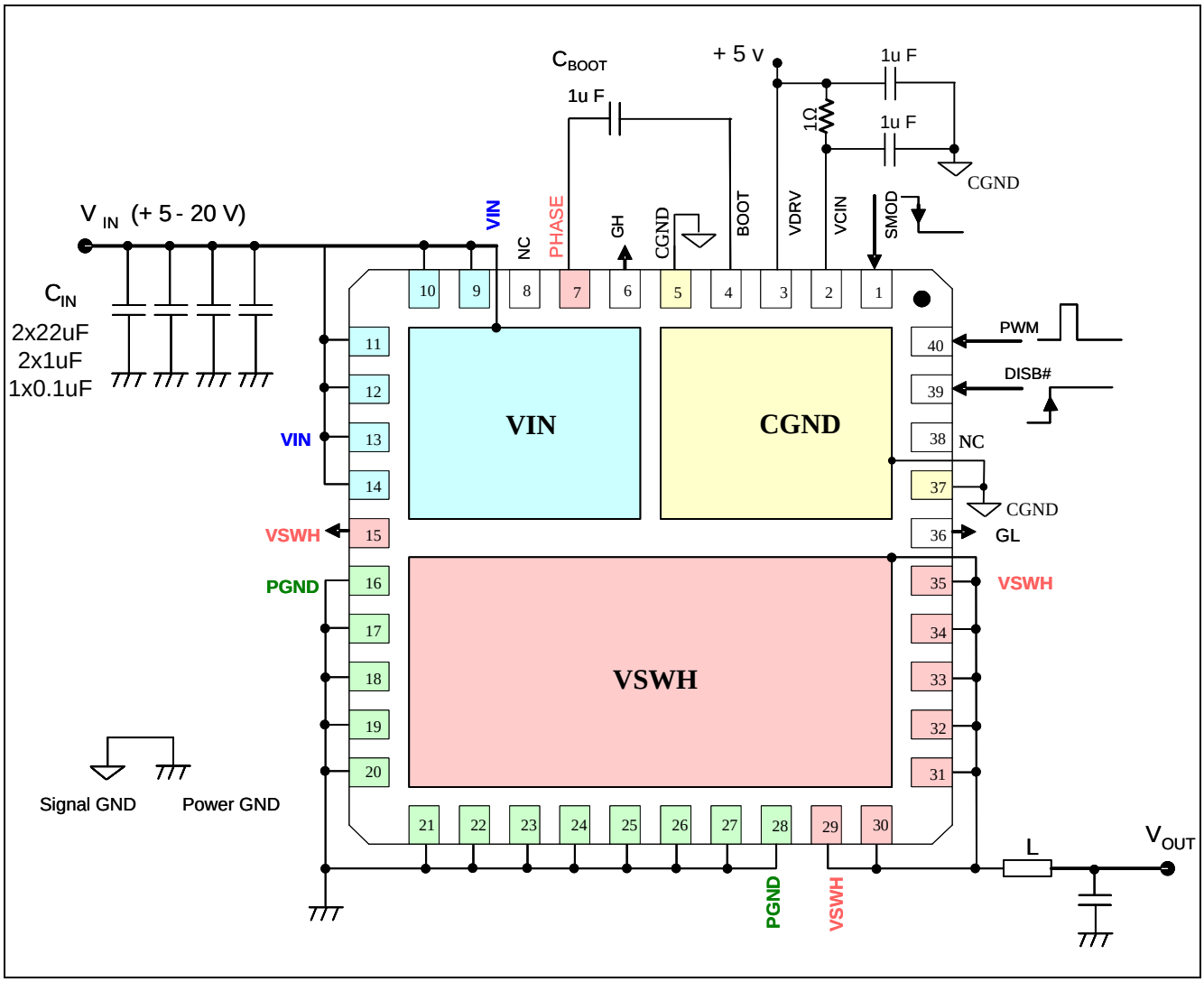


Figure 7 Pin Interconnection Outline (transparent top view)

Note:

1. *Pin PHASE is internally connected to VSWH node*
2. *It is recommended to place a RC filter between VCIN and VDRV as shown.*
3. *During power-up and down sequences, the PWM signal must be either low or tri-state (open voltage), but never high, in order to avoid uncontrolled output voltage.*

6.2 Typical Application

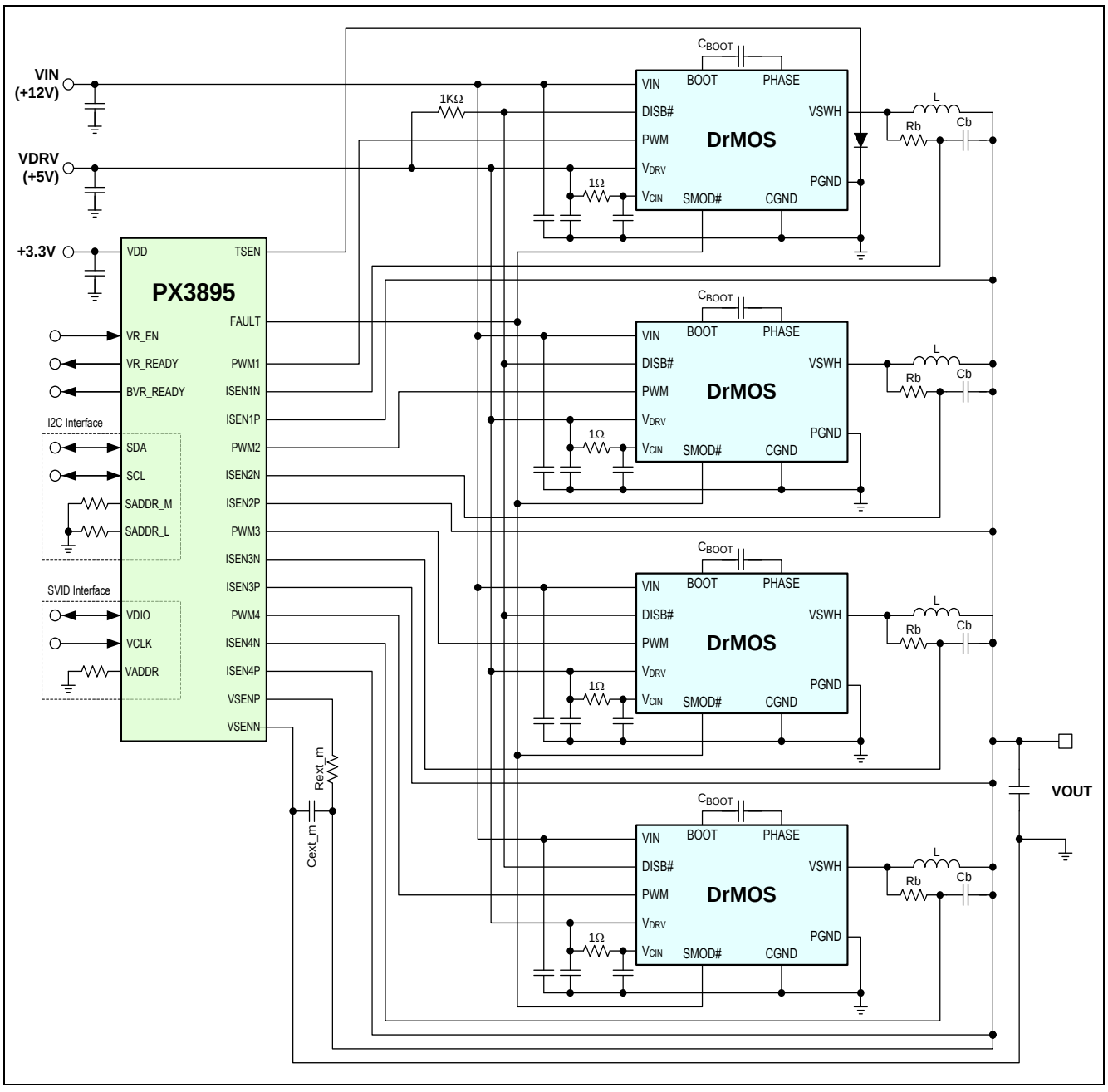


Figure 8 Four Phases Voltage Regulator Typical Application (Simplified Schematic)

7 Gate Driver Timing Diagram

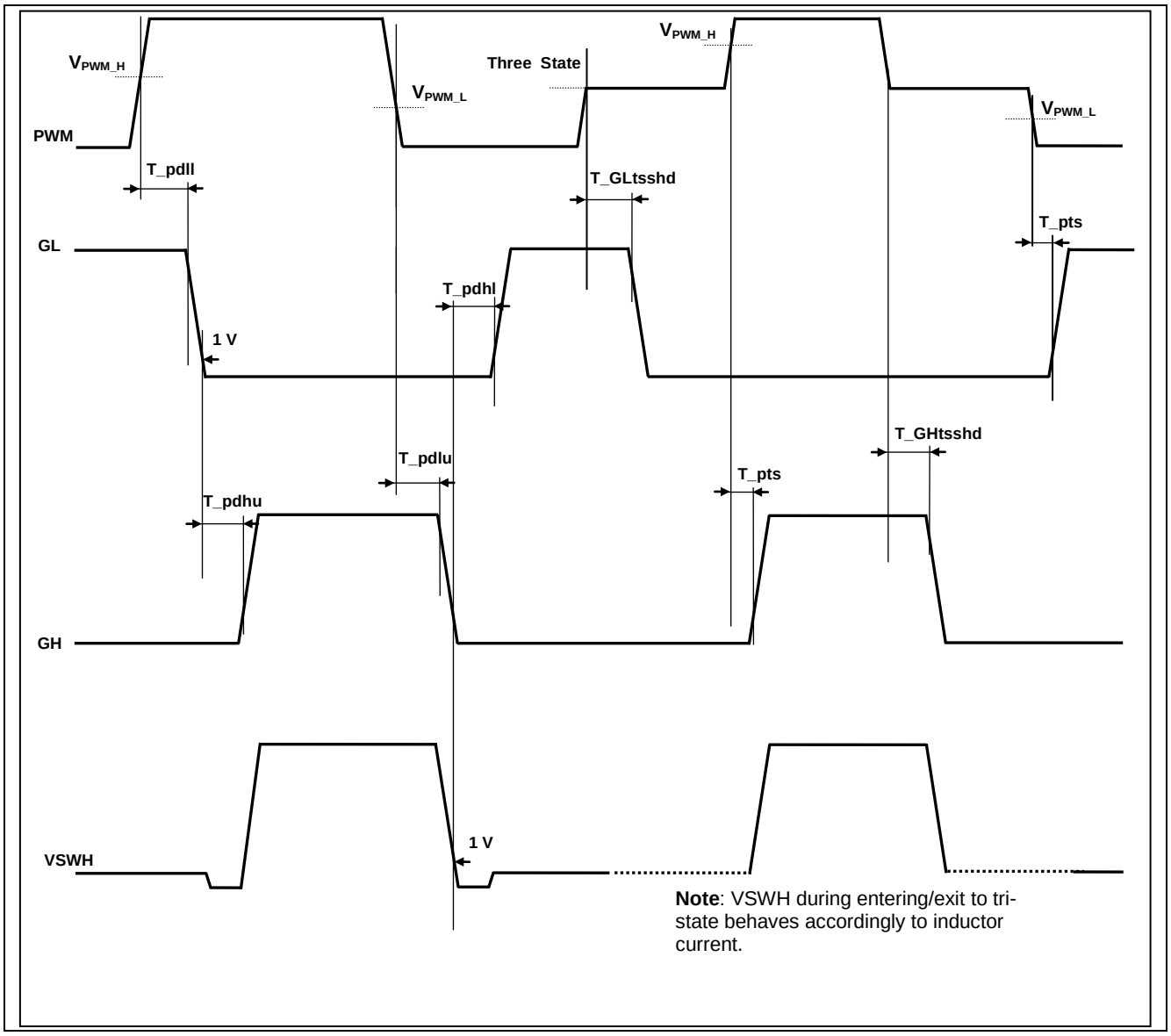


Figure 9 Adaptive Gate Driver Timing Diagram

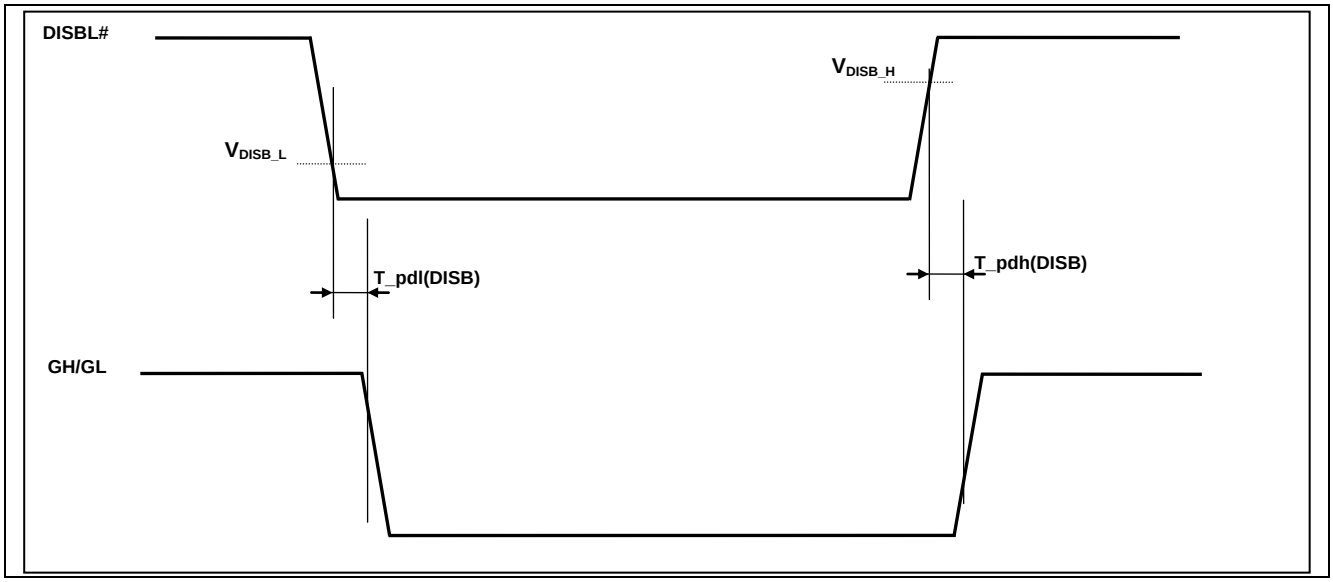


Figure 10 DISB# Timing Diagram

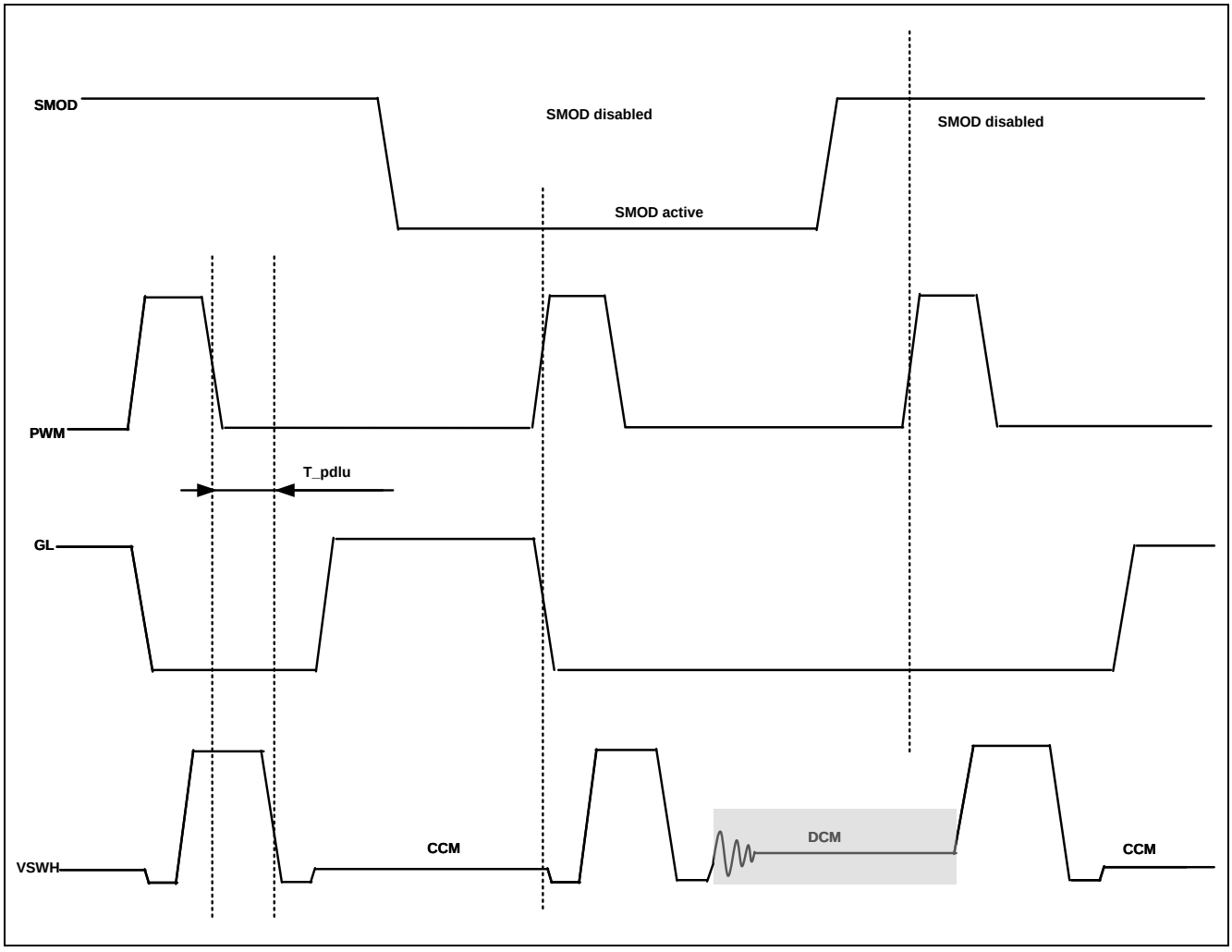


Figure 11 SMOD# Timing Diagram

8 Performance Curves – Typical Data

8.1 Efficiency and Power Loss versus Vout

Operating conditions (unless otherwise specified): VIN = +12 V, VCIN = VDRV = +5 V, VOUT = 0.8 V to 1.6 V, F_{SW} = 362 kHz, 210 nH inductor (Cooper-FPI1108, DCR (typ) = 0.29 mΩ) TA = 25° C, load line = 0 mΩ, airflow = 100LFM, no heatsink. Efficiency and Power Loss reported herein includes only TDA21220 losses. Data are taken after thermal equilibrium (~ 10 min for each current step) with unit in temperature chamber.

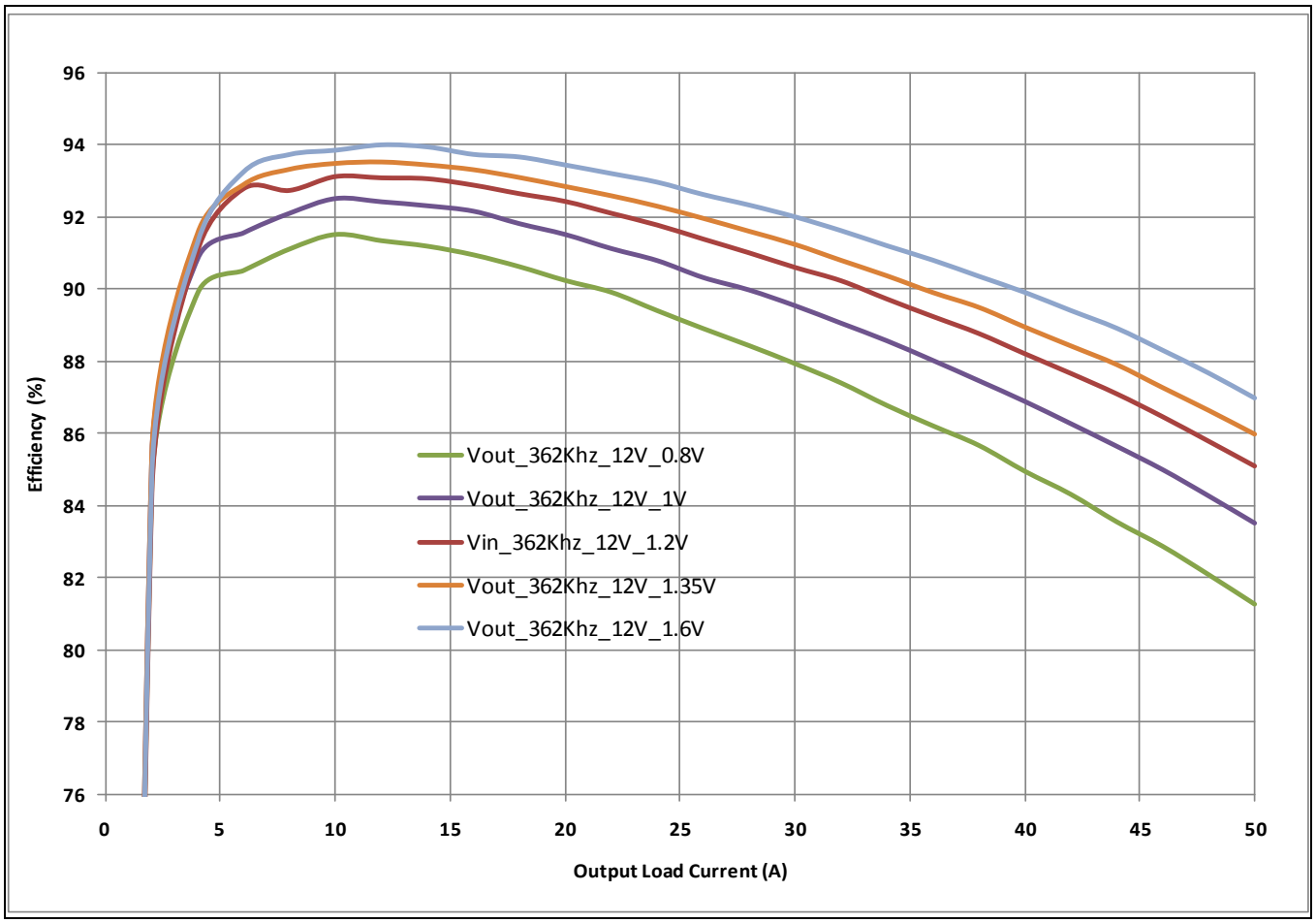


Figure 12 Efficiency vs. VOUT

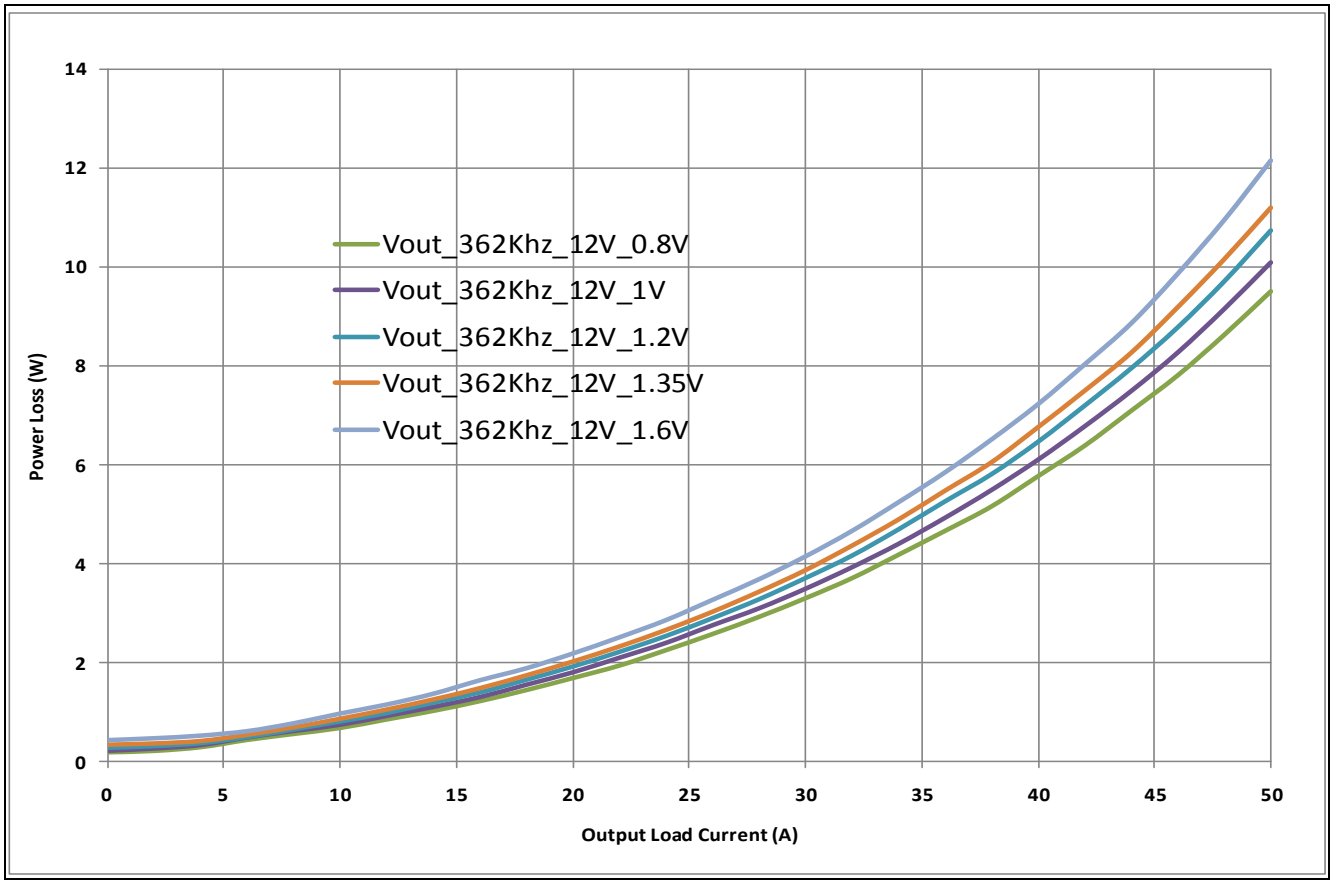


Figure 13 Power Loss vs. VOUT

8.2 Efficiency and Power Loss versus Vin

Operating conditions (unless otherwise specified): VIN = +10/12/14 V, VCIN = VDRV = +5 V, VOUT = 1.2 V, F_{SW} = 362 kHz, 210 nH inductor (Cooper-FPI1108, DCR (typ) = 0.29 mΩ) TA = 25° C, load line = 0 mΩ, airflow = 100LFM, no heatsink. Efficiency and Power Loss reported herein includes only TDA21220 losses. Data are taken after thermal equilibrium (~ 10 min for each current step) with unit in temperature chamber.

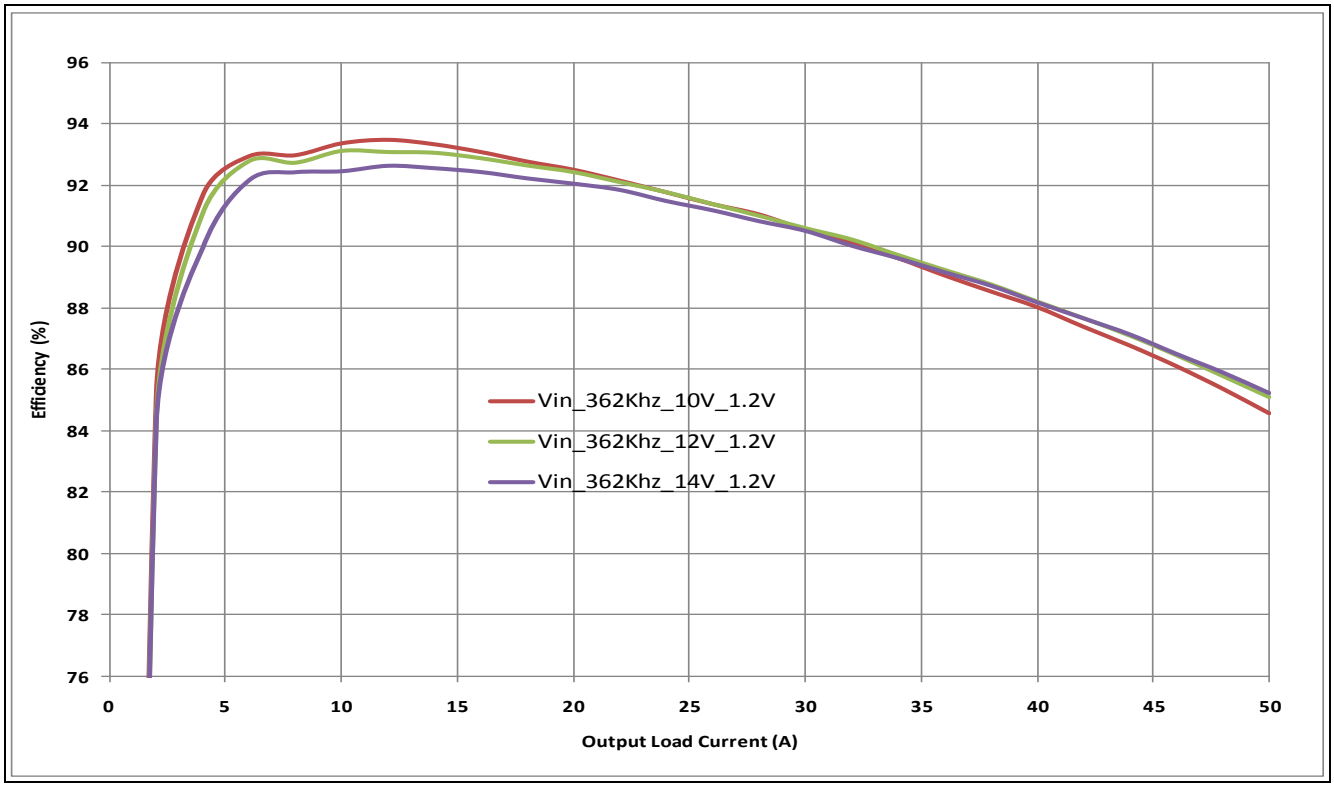


Figure 14 Efficiency vs. VIN

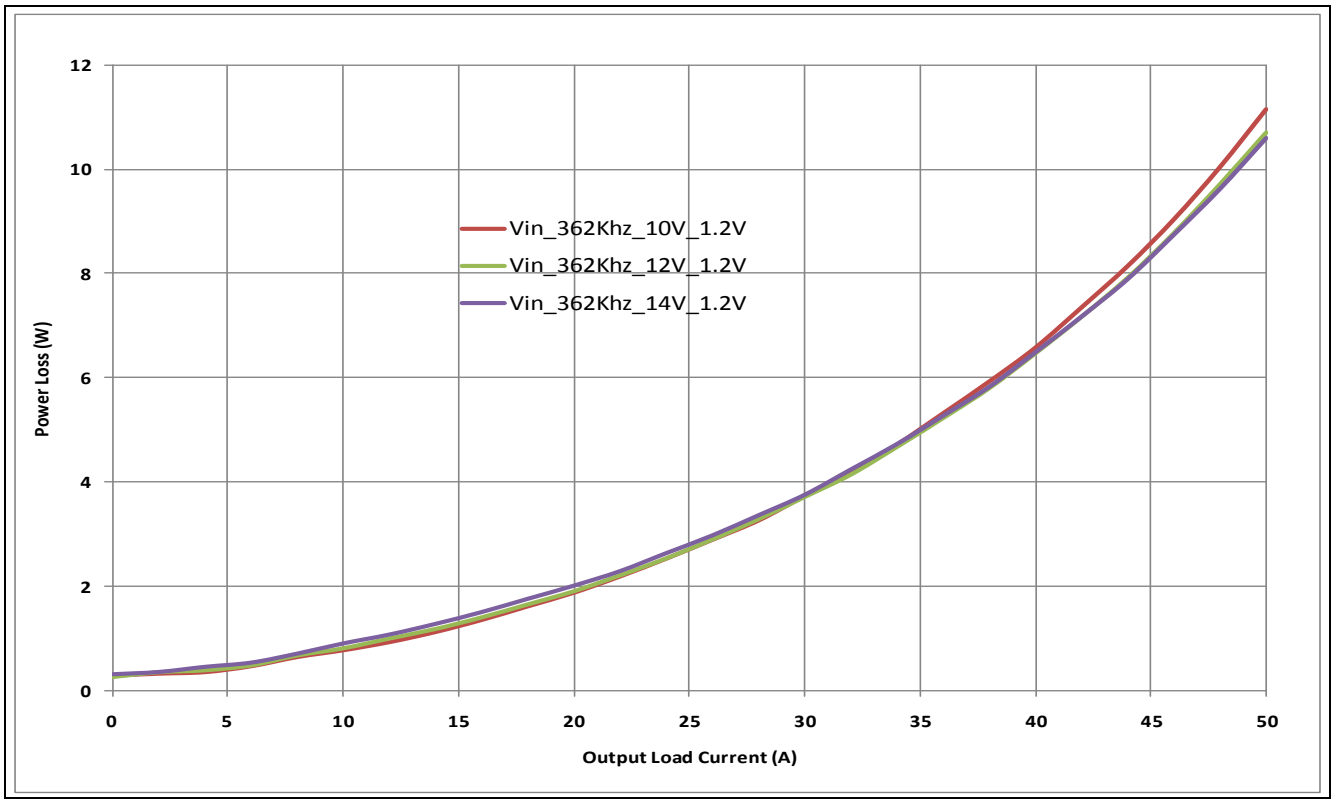


Figure 15 Power Loss vs. VIN

8.3 Efficiency and Power Loss versus Switching Frequency

Operating conditions (unless otherwise specified): VIN= +12 V, VCIN=VDRV= +5 V, VOUT=1.2 V, FSW = 296 kHz to F_{SW} = 592 kHz, 210 nH inductor (Cooper-FPI1108, DCR (typ) =0.29 mΩ) TA = 25° C, load line = 0 mΩ, airflow = 100LFM, no heatsink. Efficiency and Power Loss reported herein includes only TDA21220 losses. Data are taken after thermal equilibrium (~ 10 min for each current step) with unit in temperature chamber.

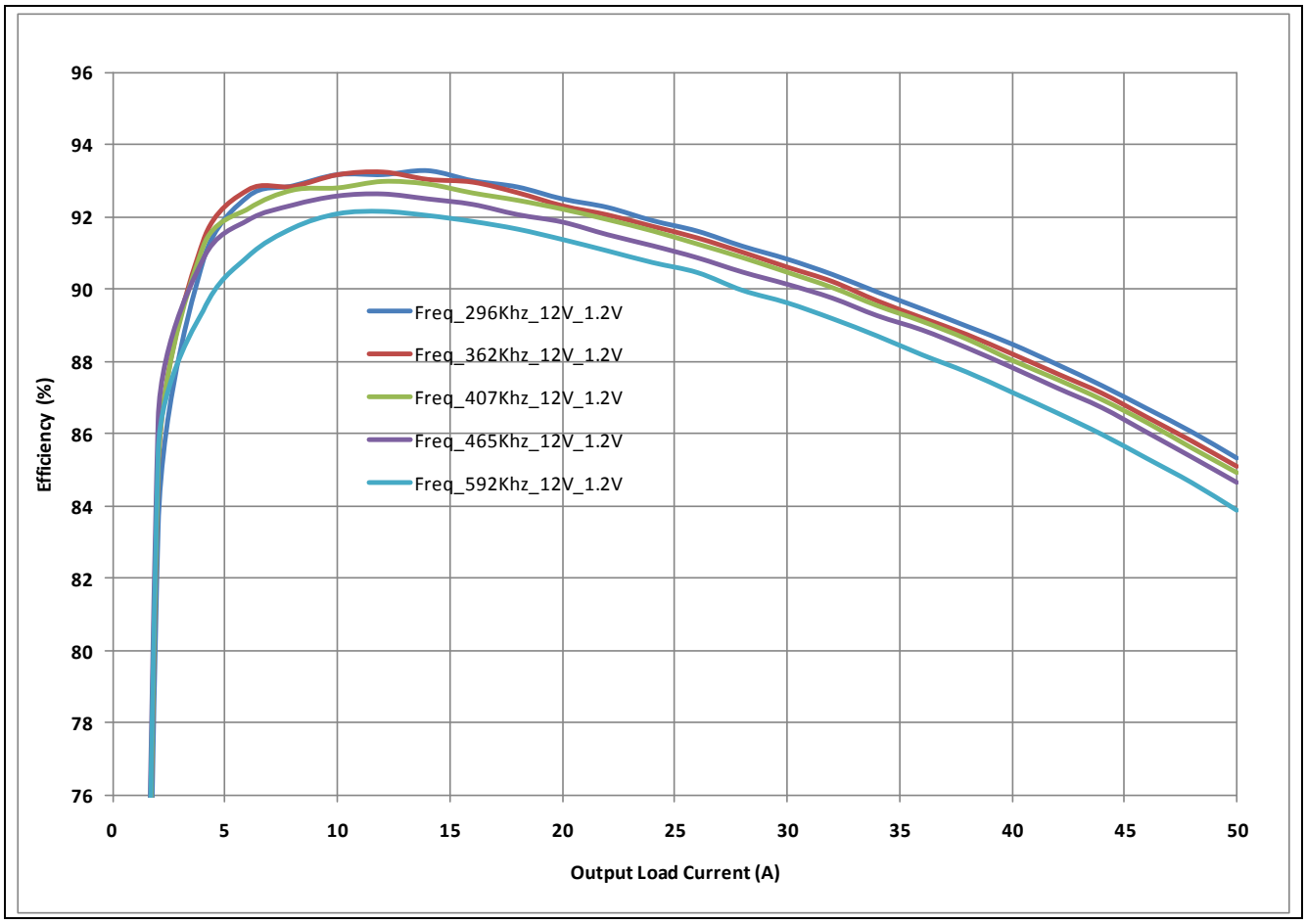


Figure 16 Efficiency vs. FSW

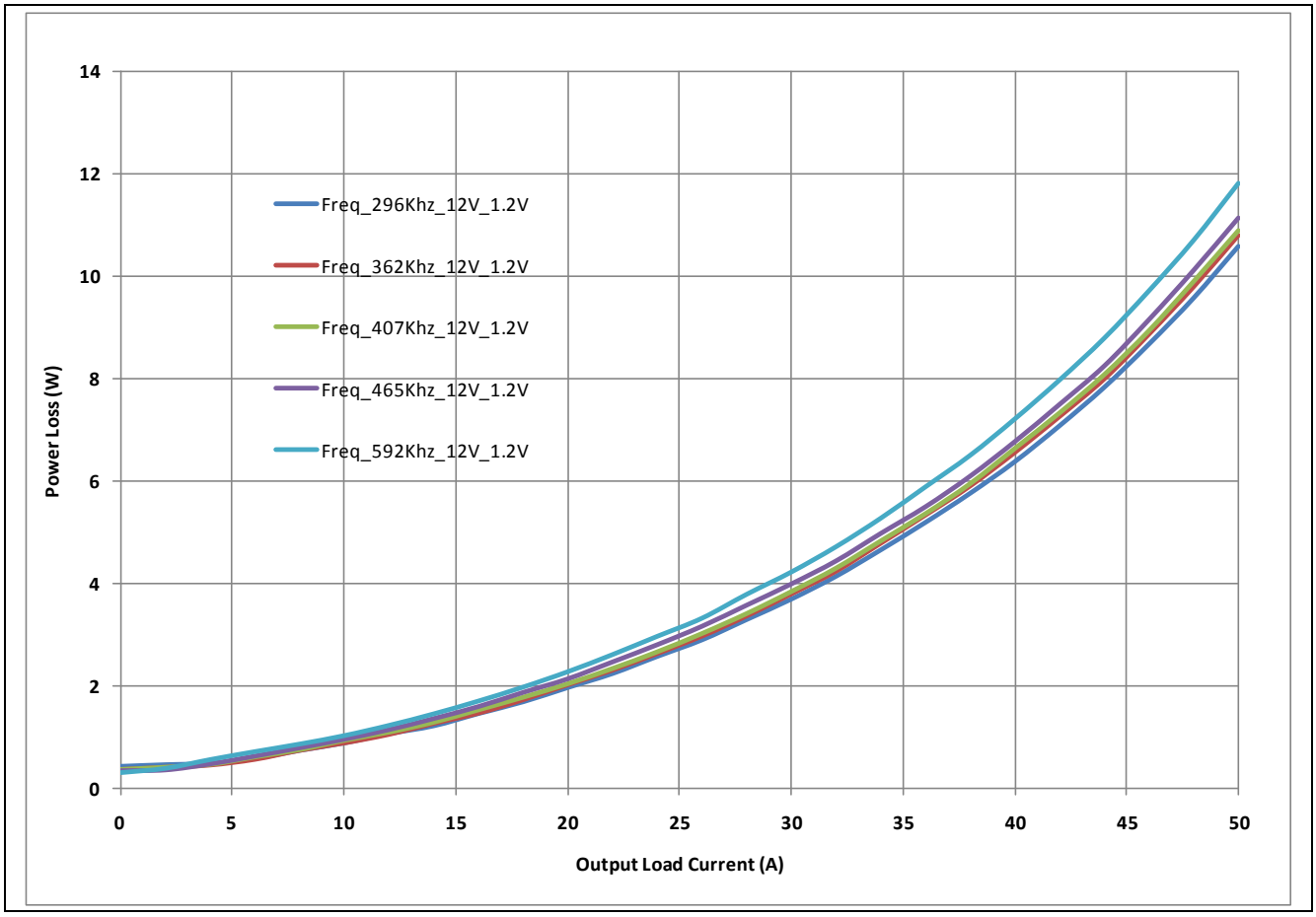


Figure 17 Power Loss vs. FSW

8.4 Driver Current versus Switching Frequency

Operating conditions (unless otherwise specified): VIN= +12 V, VCIN=VDRV= +5V, VOUT=1.2V, from F_{SW} = 296 kHz to F_{SW} = 592 kHz, 210 nH inductor (Cooper-FPI1108, DCR (typ) = 0.29 mΩ) TA = 25° C, load line = 0 mΩ, airflow = 100 LFM, no heatsink. Efficiency and Power Loss reported herein includes only TDA21220 losses. Data are taken after thermal equilibrium (~ 10 min for each current step) with unit in temperature chamber.

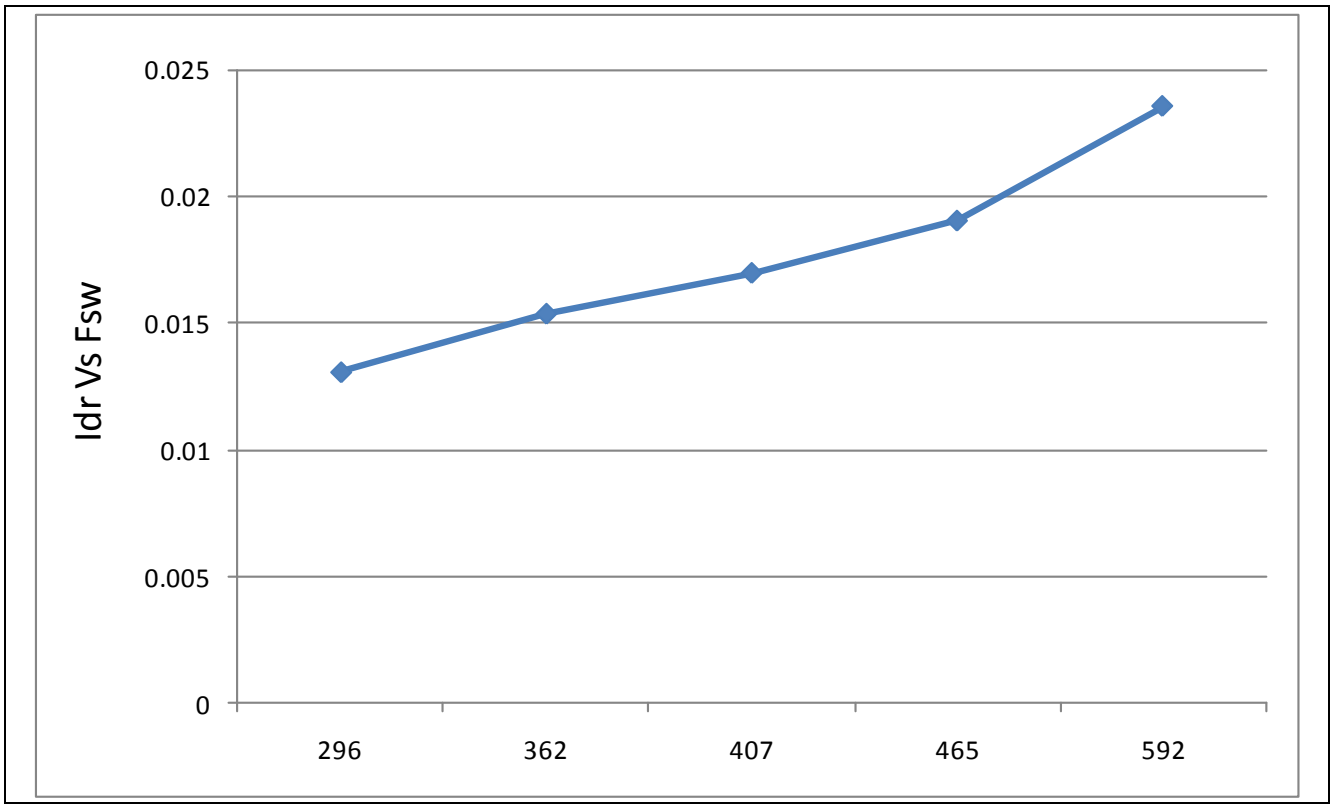
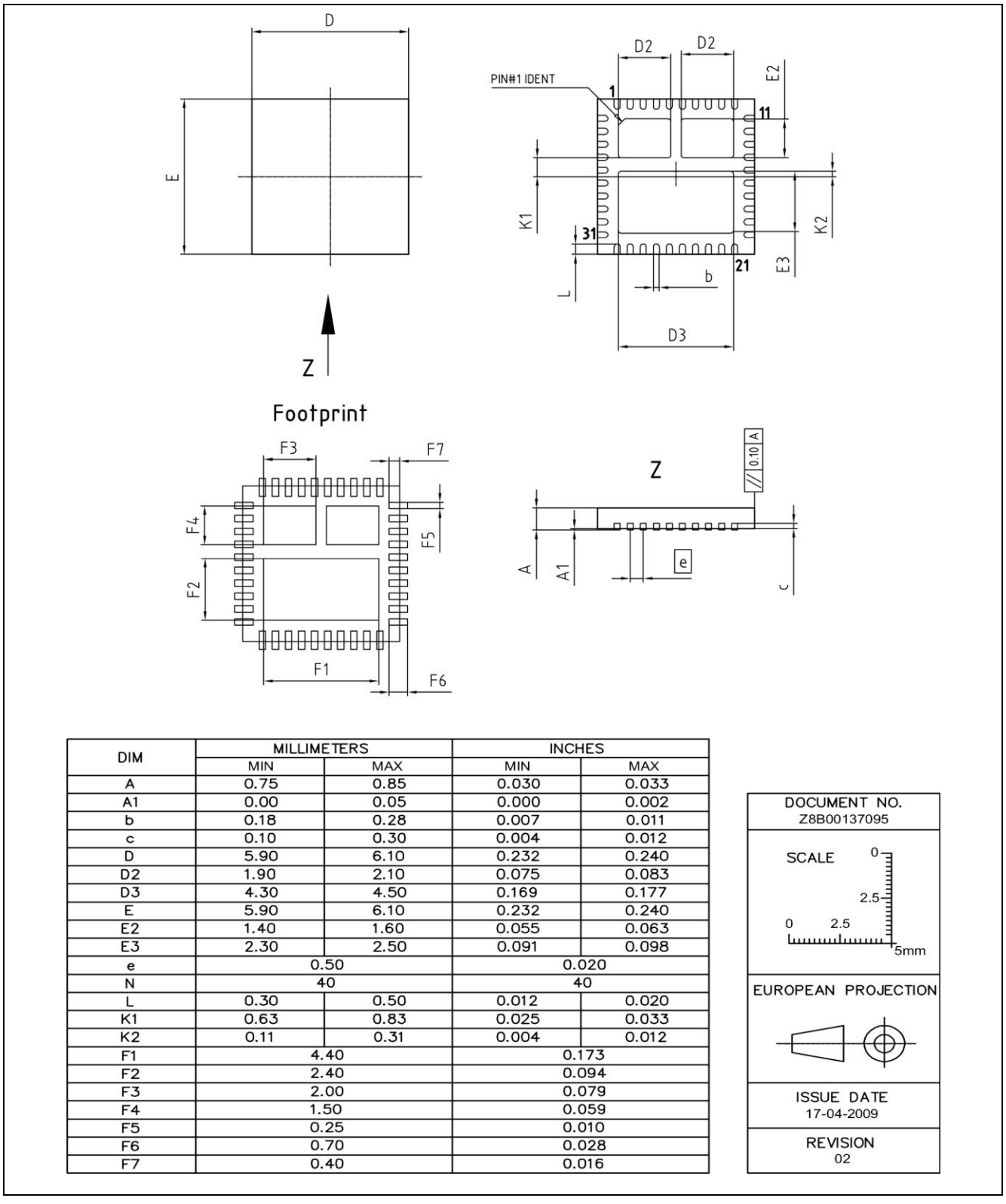


Figure 18 IDR Vs FSW

9 Mechanical Drawing



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.75	0.85	0.030	0.033
A1	0.00	0.05	0.000	0.002
b	0.18	0.28	0.007	0.011
c	0.10	0.30	0.004	0.012
D	5.90	6.10	0.232	0.240
D2	1.90	2.10	0.075	0.083
D3	4.30	4.50	0.169	0.177
E	5.90	6.10	0.232	0.240
E2	1.40	1.60	0.055	0.063
E3	2.30	2.50	0.091	0.098
e	0.50		0.020	
N	40		40	
L	0.30	0.50	0.012	0.020
K1	0.63	0.83	0.025	0.033
K2	0.11	0.31	0.004	0.012
F1	4.40		0.173	
F2	2.40		0.094	
F3	2.00		0.079	
F4	1.50		0.059	
F5	0.25		0.010	
F6	0.70		0.028	
F7	0.40		0.016	

DOCUMENT NO.
Z8B00137095

SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

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Figure 19 Mechanical Dimensions

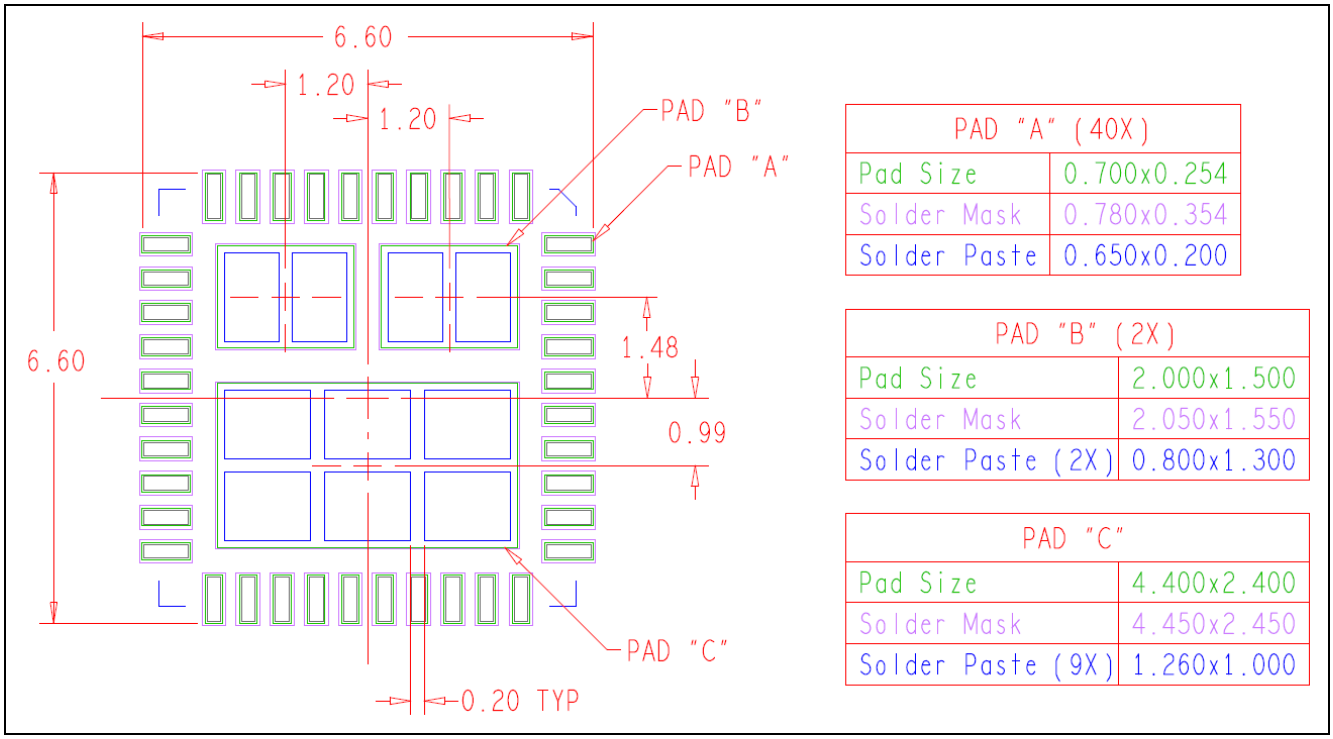

Figure 20 Footprint and Solder Stencil Recommendations

w w w . i n f i n e o n . c o m

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