

300-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64 GRAY SCALE)

DESCRIPTION

The μPD16634A is a source driver for TFT-LCDs capable of dealing with displays 64 gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ -corrected by an internal D/A converter and 5-by-2 external power modules. Because the

★ output dynamic range is as large as $V_{SS2}+0.1$ V to $V_{DD2}-0.1$ V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also to be able to deal with dot-line inversion when mounted on a single side, this source driver equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequent of 40 MHz when driving at 3.0 V, this driver is applicable to XGA-standard TFT-LCD panels.

FEATURES

- 300 outputs
- CMOS level input
- Input of 6 bits (gradation data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- ★ • Output dynamic range : $V_{SS2}+0.1$ V to $V_{DD2}-0.1$ V
- ★ • Logic part supply voltage (V_{DD1}) : 3.3 V \pm 0.3 V
- ★ • Driver part supply voltage (V_{DD2}) : 8.0 V \pm 0.5 V
- High-speed data transfer: $f_{MAX}=40$ MHz MIN.(internal data transfer rate when operating at 3.0 V)
- Output voltage polarity inversion is possible (POL)
- Display data inversion function (POL2)
- Single bank arrangement is possible(loaded with slim TCP).

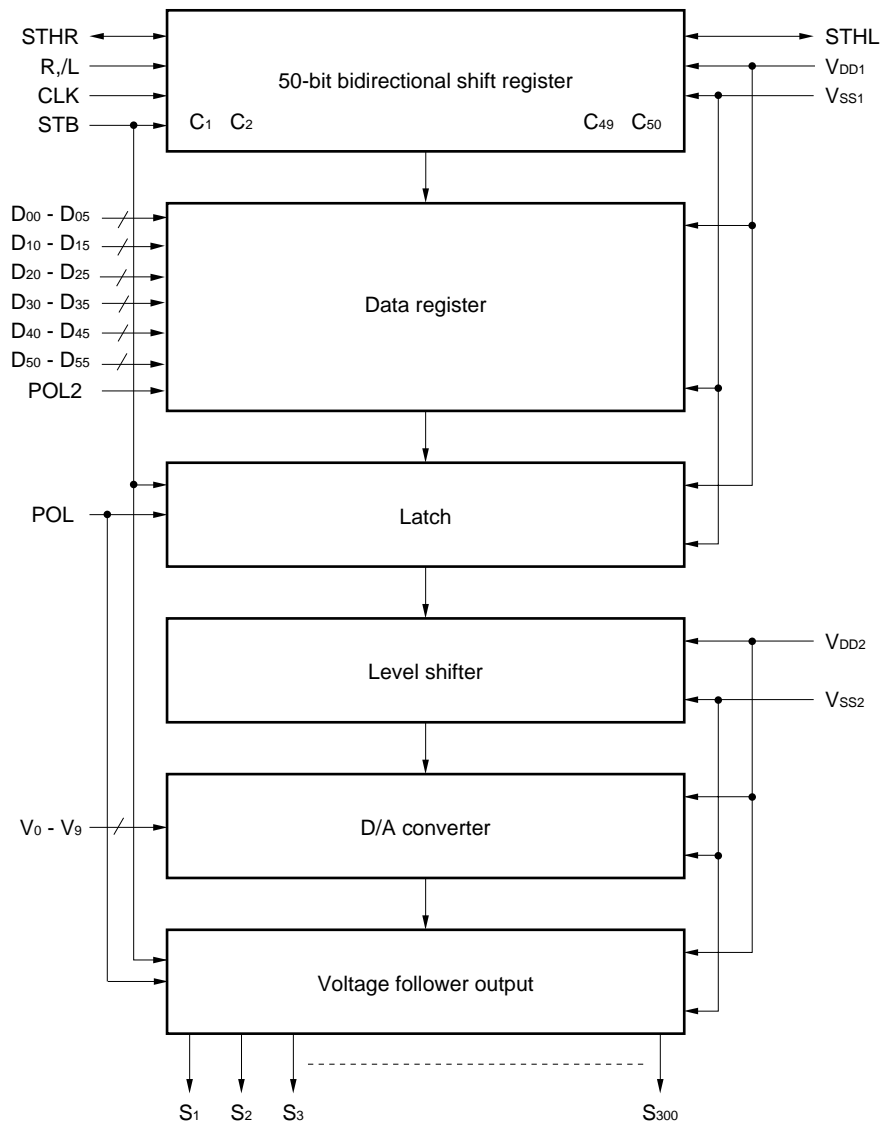
ORDERING INFORMATION

Part Number	Package
μPD16634AN-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

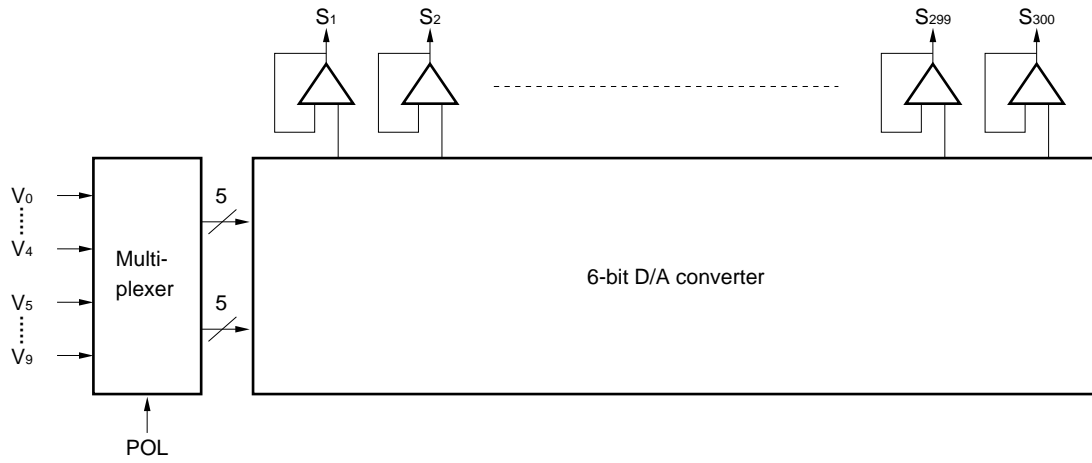
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1. BLOCK DIAGRAM

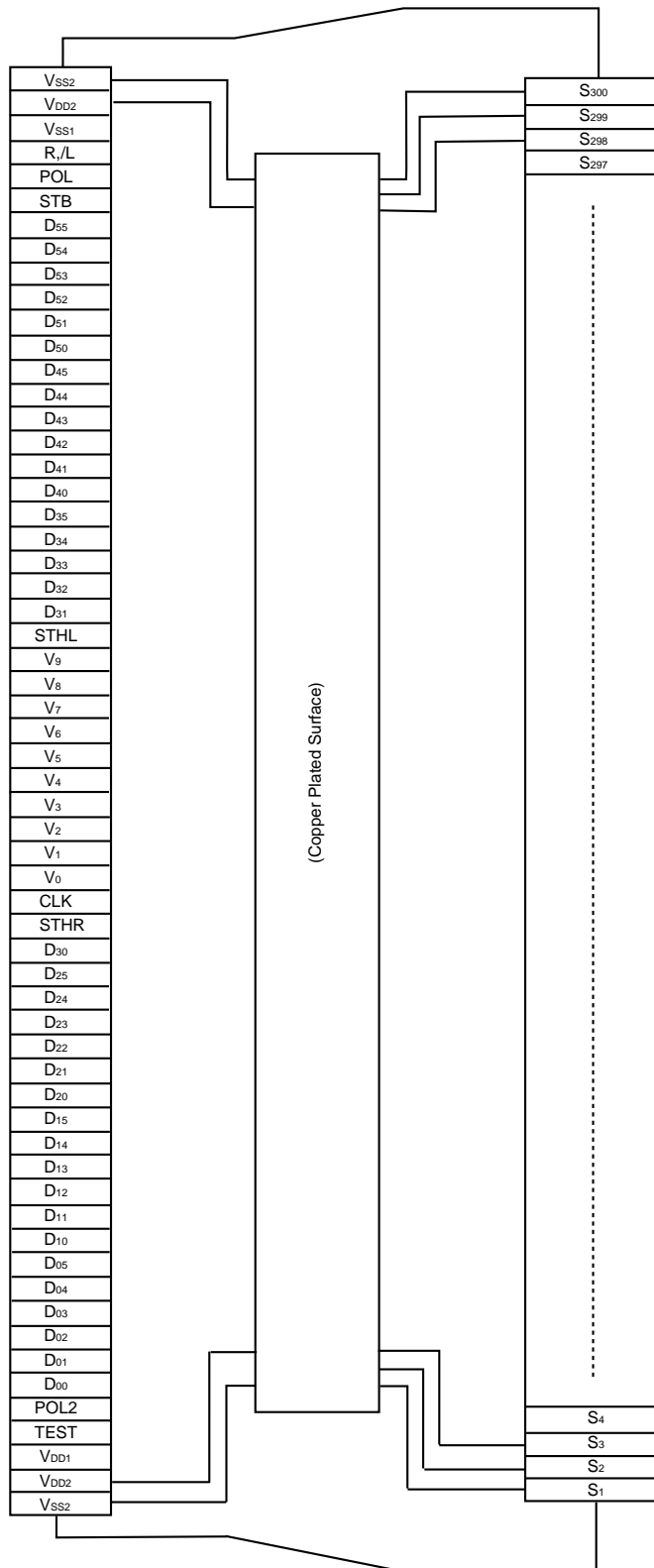


Remark /xxx indicates active low signal.

★ 2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16634AN-xxx)



Caution This figure does not specify the TCP package. Therefore POL2 pins can be reduced by opening or short-circuiting to Vss2 by TCP wiring. POL2 pin can short to Vss1 on TCP. So when you not use “data inversion function”, can reduce input pins.

4. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S ₁ to S ₃₀₀	Driver output	The D/A converted 64-gray-scale analog voltage is output
D ₀₀ to D ₀₅	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D _{x0} : LSB, D _{x5} : MSB
D ₁₀ to D ₁₅		
D ₂₀ to D ₂₅		
D ₃₀ to D ₃₅		
D ₄₀ to D ₄₅		
D ₅₀ to D ₅₅		
R _, /L	Shift direction switching input	These refer to the start pulse input/output pins when cascades are connected. The shift directions of the shift registers are as follows. R _, /L = H : STHR input, S ₁ →S ₃₀₀ , STHL output R _, /L = L : STHL input, S ₃₀₀ →S ₁ , STHR output
STHR	Right shift start pulse input/output	R _, /L = H : Becomes the start pulse input pin. R _, /L = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R _, /L = H : Becomes the start pulse input pin. R _, /L = L : Becomes the start pulse output pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 50th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. The initial-level driver's 50th clock becomes valid as the next-level driver's start pulse is input. If 52 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch input	The contents of the data register are transferred to the latch at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L ; The S _{2n-1} output uses V ₀ to V ₄ as the reference supply; and the S _{2n} output uses V ₅ to V ₉ as the reference supply. POL = H ; The S _{2n-1} output uses V ₅ to V ₉ as the reference supply; and the S _{2n} output uses V ₀ to V ₄ as the reference supply. S _{2n-1} indicates the odd output; and S _{2n} indicates the even output. Input of the POL signal is allowed the setup time (t _{POL-STB}) with respect to STB's rising edge.
POL2	Data inversion input	POL2 = H : Display data is inverted. POL2 = L : Display data is not inverted.
V ₀ to V ₉	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. V _{DD2} > V ₀ > V ₁ > V ₂ > V ₃ > V ₄ > V ₅ > V ₆ > V ₇ > V ₈ > V ₉ > V _{SS2}
TEST	Test pin	Set it to open.
V _{DD1}	Logic circuit power supply	3.3 V ± 0.3 V
V _{DD2}	Driver circuit power supply	8.0 V ± 0.5 V
V _{SS1}	Logic ground	Grounding
V _{SS2}	Driver ground	Grounding

- Cautions**
1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V₀ to V₉ in that order. Reverse this sequence to shut down.(Simultaneous power application to V_{DD2} and V₀ to V₉ is possible.)
 2. To stabilize the supply voltage, please be sure to insert 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increase precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals(V₀,V₁,V₂...,V₉) and V_{SS2}.
 3. We recommend to use Operational Amplifier to lower input impedance of γ-corrected voltage.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

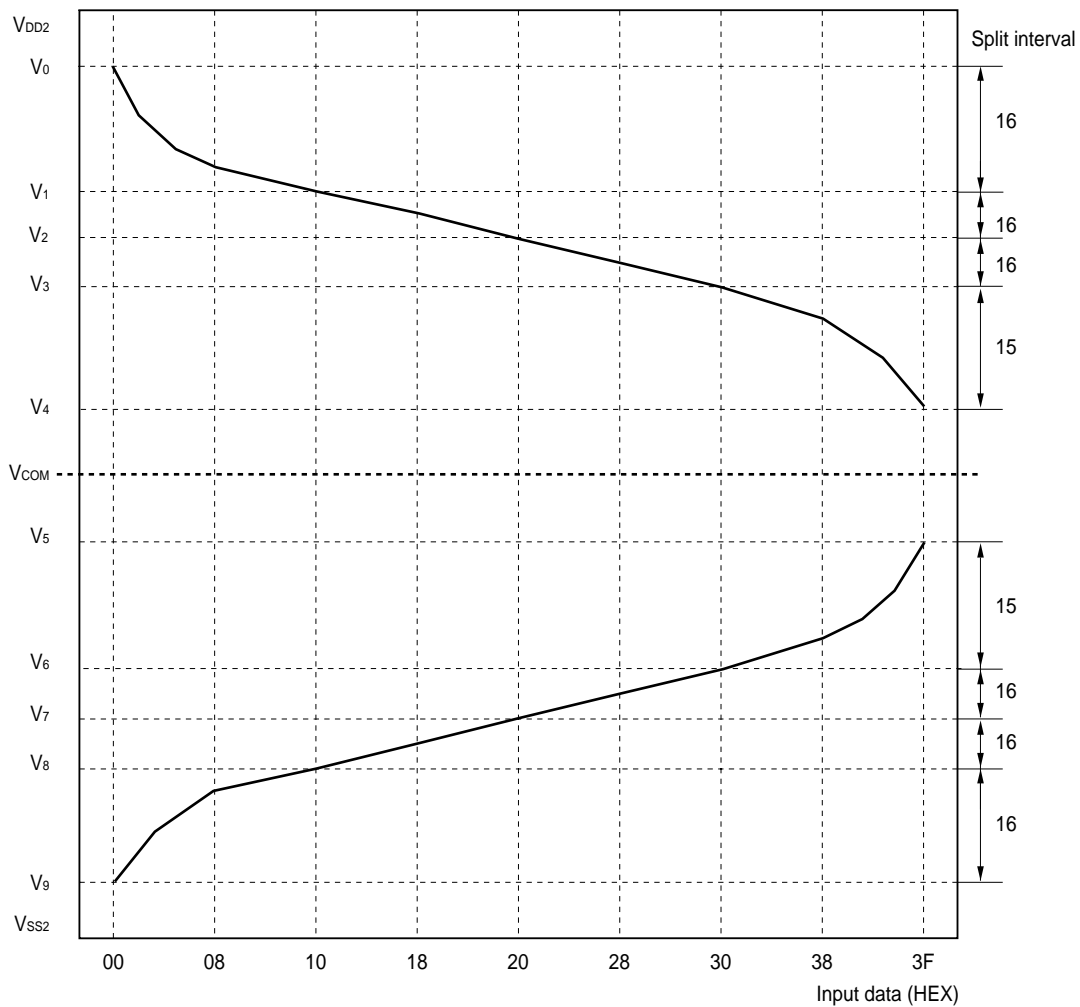
This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors r_0 to r_{62} are so designed that the ratios between the LCD panel's γ -corrected voltages and $V_{0'}$ to $V_{63'}$, $V_{0''}$ to $V_{63''}$ are roughly equal; and their respective resistance values are as shown in Table 6-1. Among the 5-by 2 γ -corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective five γ -corrected voltages of V_0 to V_4 and V_5 to V_9 . If fine gray scale voltage precision is not necessary, the voltage follower circuit supplied to the γ -corrected power supplies V_1 to V_3 and V_6 to V_8 can be deleted.

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2} , common electrode potential V_{COM} , and γ -corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$. Figure 6-1 and 6-2 show the relationship between the input data and the output data.

This driver IC is designed for single-sided mounting. Therefore, please do not use it for γ -corrected power supply level inversion in double-sided mounting.

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Figure 5-1. Relationship between Input Data and Output Voltage



6. RESISTOR STRINGS

Figure 6-1. Relationship Between Input Data and Output Voltage : $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5$, POL2 = L

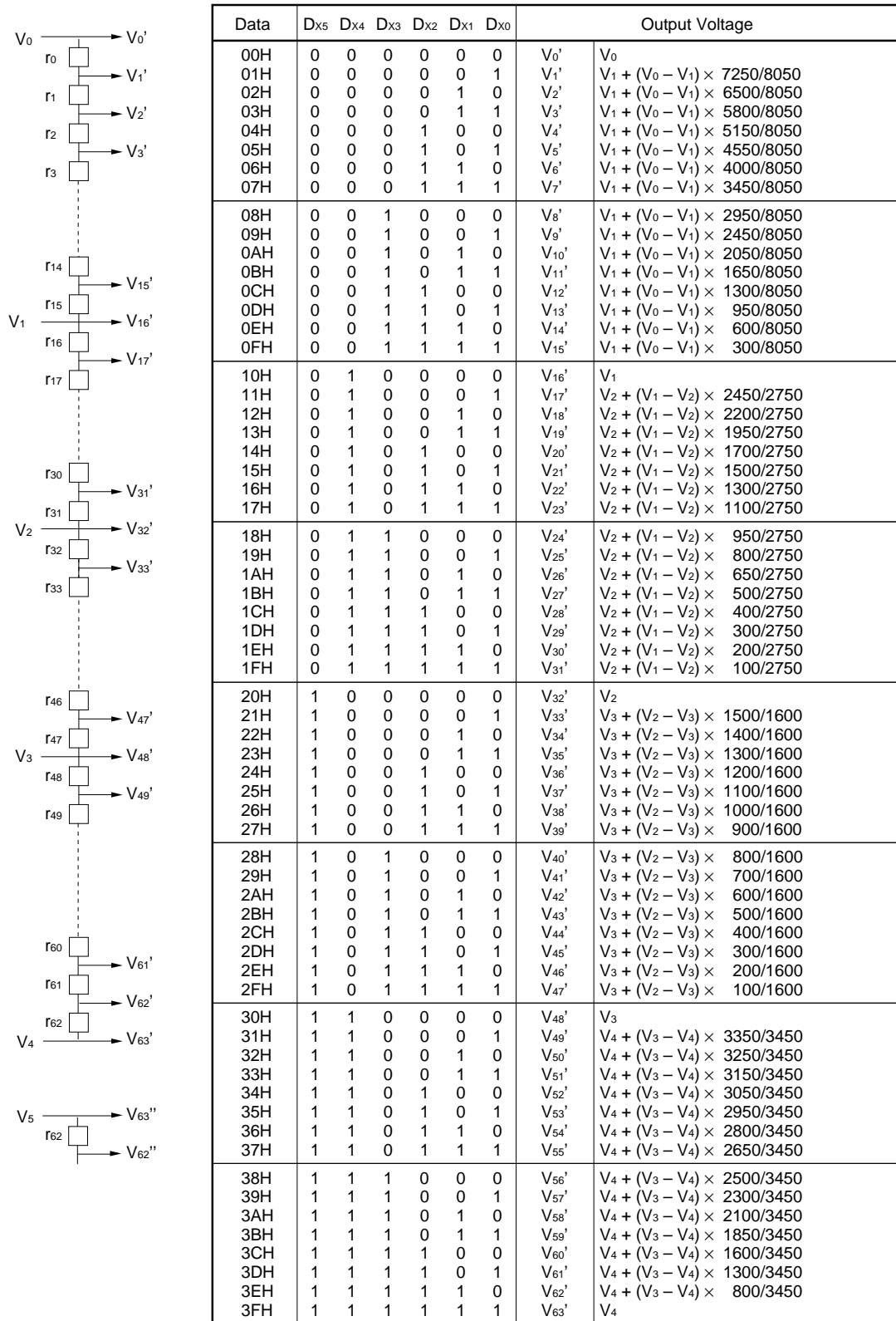


Figure 6-2. Relationship Between Input Data and Output Voltage : $V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$, POL2 = L

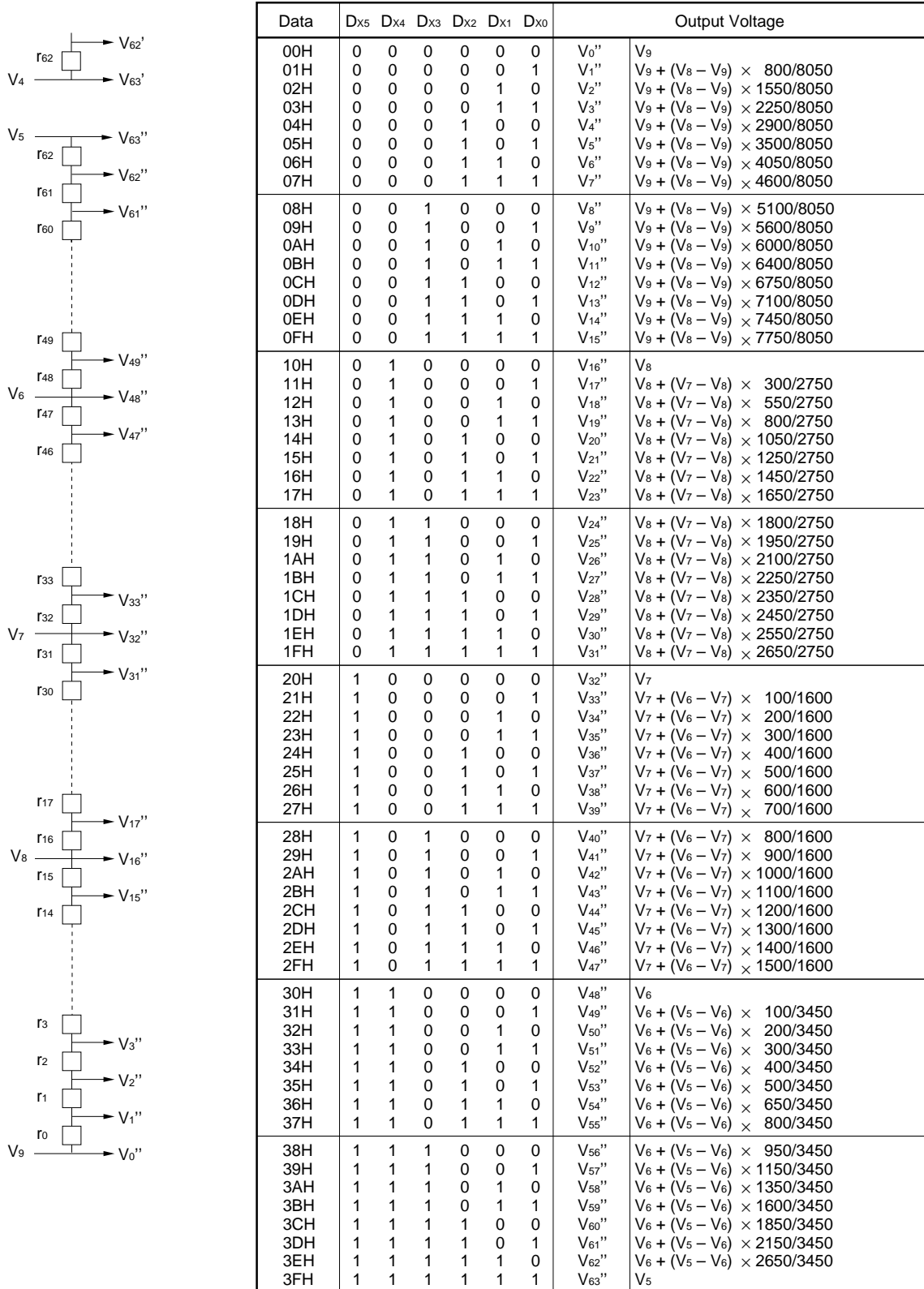


Table 6-1. Ladder Resistance Values (r₀ to r₆₂) : Reference Value

Resistor Name	Resistance Value (Ω)	Resistor Name	Resistance Value (Ω)
r ₀	800	r ₃₂	100
r ₁	750	r ₃₃	100
r ₂	700	r ₃₄	100
r ₃	650	r ₃₅	100
r ₄	600	r ₃₆	100
r ₅	550	r ₃₇	100
r ₆	550	r ₃₈	100
r ₇	500	r ₃₉	100
r ₈	500	r ₄₀	100
r ₉	400	r ₄₁	100
r ₁₀	400	r ₄₂	100
r ₁₁	350	r ₄₃	100
r ₁₂	350	r ₄₄	100
r ₁₃	350	r ₄₅	100
r ₁₄	300	r ₄₆	100
r ₁₅	300	r ₄₇	100
r ₁₆	300	r ₄₈	100
r ₁₇	250	r ₄₉	100
r ₁₈	250	r ₅₀	100
r ₁₉	250	r ₅₁	100
r ₂₀	200	r ₅₂	100
r ₂₁	200	r ₅₃	150
r ₂₂	200	r ₅₄	150
r ₂₃	150	r ₅₅	150
r ₂₄	150	r ₅₆	200
r ₂₅	150	r ₅₇	200
r ₂₆	150	r ₅₈	250
r ₂₇	100	r ₅₉	250
r ₂₈	100	r ₆₀	300
r ₂₉	100	r ₆₁	500
r ₃₀	100	r ₆₂	800
r ₃₁	100	Total	15850

7. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

(1) R,/L = H (right shift)

Output	S ₁	S ₂	S ₃	S ₄	S ₅	...	S ₂₉₉	S ₃₀₀
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	D ₄₀ to D ₄₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

(2) R,/L = L (left shift)

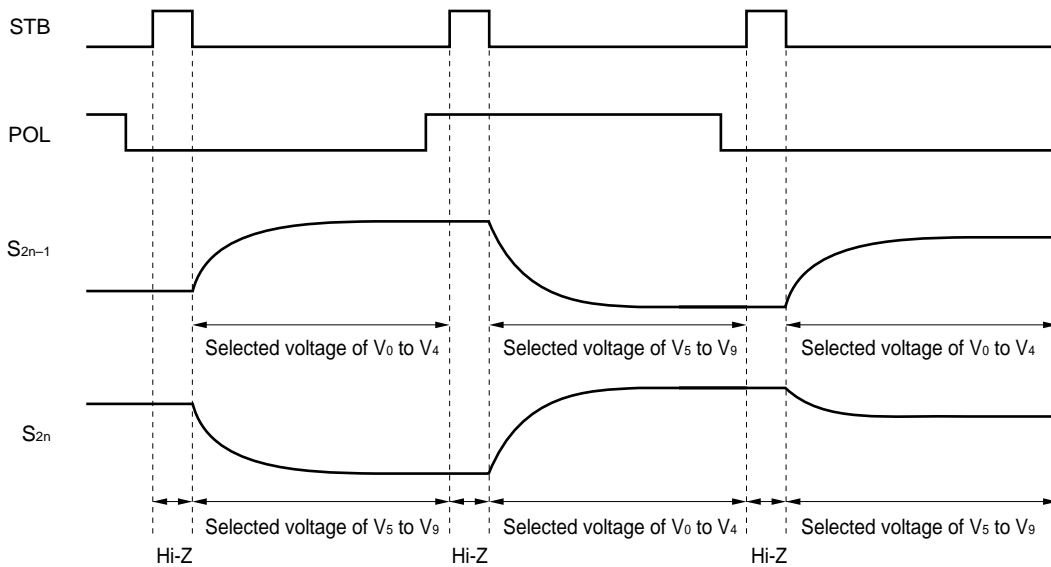
Output	S ₁	S ₂	S ₃	S ₄	S ₅	...	S ₂₉₉	S ₃₀₀
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	D ₄₀ to D ₄₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

POL	S _{2n-1}	S _{2n}
L	V ₀ to V ₄	V ₅ to V ₉
H	V ₅ to V ₉	V ₀ to V ₄

Remark S_{2n-1} (Odd output), S_{2n} (Even output)n = 1,2,.....,150

8. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

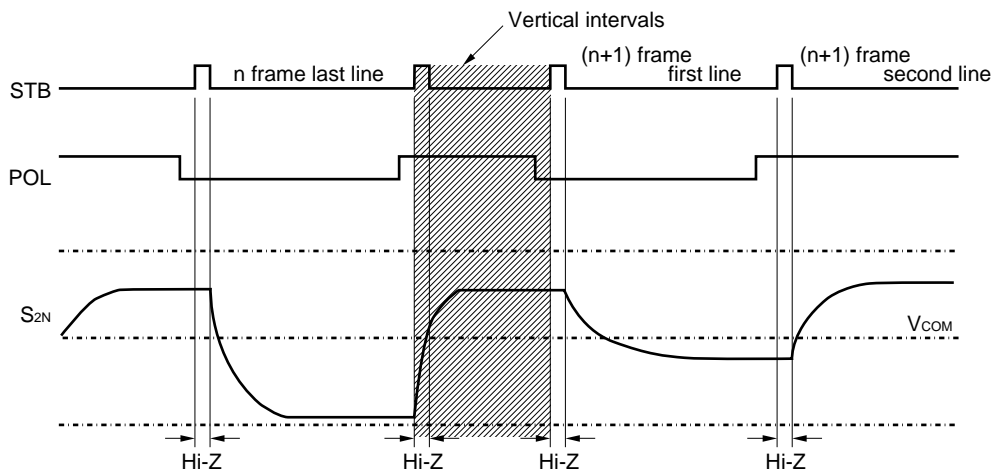
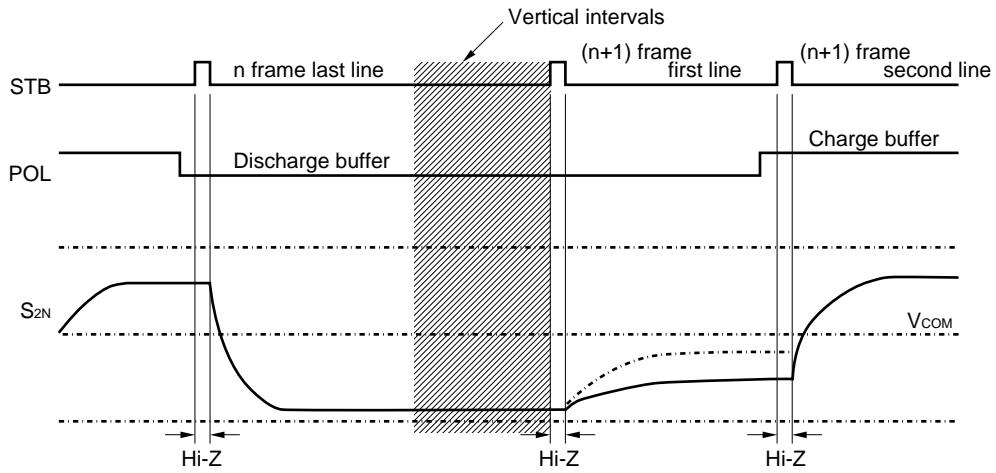


9. CAUTIONS ABOUT FRAME INVERSION

In the case of dot inversion, n frame last line and (n+1) frame first line is the same polarity. When write the same polarity twice; there are two cases as follows.

- (1) Last line output in n frame > First line output in (n+1) frame → Positive to write
- (2) Last line output in n frame < First line output in (n+1) frame → Not possible to write

μPD16634A has charge buffer and discharge buffer, so need to inversion polarity and write in the case of both ways.



10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ($T_A = 25\text{ }^\circ\text{C}, V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Ratings	Unit
Logic part supply voltage	V_{DD1}	-0.5 to +5.0	V
Driver part supply voltage	V_{DD2}	-0.5 to +10.0	V
Logic part input voltage	V_{I1}	-0.5 to $V_{DD1} + 0.5$	V
Driver part input voltage	V_{I2}	-0.5 to $V_{DD2} + 0.5$	V
Logic part output voltage	V_{O1}	-0.5 to $V_{DD1} + 0.5$	V
Driver part output voltage	V_{O2}	-0.5 to $V_{DD2} + 0.5$	V
Operating ambient temperature	T_A	-10 to +75	°C
Storage temperature	T_{stg}	-55 to +125	°C

- ★ **Caution** If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range ($T_A = -10\text{ to }+75\text{ }^\circ\text{C}, V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic part supply voltage	V_{DD1}	3.0	3.3	3.6	V
Driver part supply voltage	V_{DD2}	7.5	8.0	8.5	V
High-level input voltage	V_{IH}	$0.7V_{DD1}$		V_{DD1}	V
Low-level input voltage	V_{IL}	0		$0.3V_{DD1}$	V
γ-corrected supply voltage	$V_0\text{ to }V_9$	V_{SS2}		V_{DD2}	V
Driver part output voltage	V_O	$V_{SS2} + 0.1$		$V_{DD2} - 0.1$	V
Maximum clock frequency	$f_{MAX.}$	40			MHz

Electrical Characteristics (T_A = -10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 8.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I _{IL}				±1.0	μA
High-level output voltage	V _{OH}	STHR(STHL), I _o =0 mA	V _{DD1} -0.1			V
Low-level output voltage	V _{OL}	STHR(STHL), I _o =0 mA			0.1	V
γ-corrected supply current	I _γ	V ₀ -V ₉ = 8 V V ₀ , V ₉		0.3	0.6	mA
Driver output current	I _{VOH}	V _X =7 V, V _{OUT} =1 V ^{Note1}			-0.5	mA
	I _{VOL}	V _X =1 V, V _{OUT} =7 V ^{Note1}	0.5			mA
Output voltage deviation ^{Note2}	ΔV _O	Input data : 00H to 3FH		±5	±20	mV
Average output voltage variation ^{Note3}	ΔV _{AV}	Input data : 00H to 3FH		±10		mV
Output voltage range	V _O	Input data : 00H to 3FH	0.1		V _{DD2} -0.1	V
Logic part dynamic current consumption ^{Notes4,5}	I _{DD1}	V _{DD1} , when with no load		0.5	3.5	mA
★ Driver part dynamic current consumption ^{Notes4,5}	I _{DD2}	V _{DD2} , when with no load		2.2	8.0	mA

Notes 1. V_X refers to the output voltage of analog output pins S₁ to S₃₀₀.

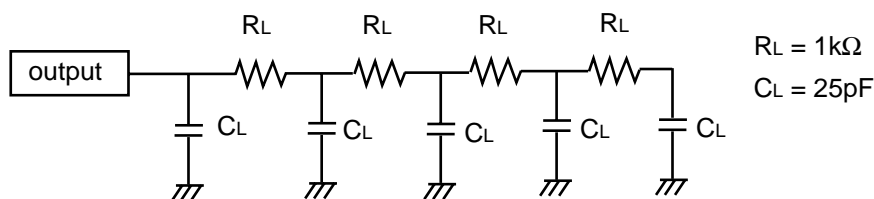
V_{OUT} refers to the voltage applied to analog output pins S₁ to S₃₀₀.

- The output voltage deviation refers to the voltage difference between adjoining output pins when the display data is the same (within the chip).
- The average output voltage variation refers to the average output voltage difference between chips. The average output voltage refers to the average voltage between chips when the display data is the same.
- The STB cycle is defined to be 20 μs at f_{CLK} = 40 MHz. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
- Refers to the current consumption per driver when cascades are connected under the assumption of SVGA single-sided mounting (10 units).

Switching Characteristics (T_A = -10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 8.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse delay time	t _{PLH1}	C _L = 25 pF		13	20	ns
Driver output delay time	t _{PHL2}	C _L = 125 pF, R _L = 4 kΩ ^{Note}		3.7	8	μs
	t _{PHL3}			5.3	14	μs
	t _{PLH2}			3.0	8	μs
	t _{PLH3}			5.3	14	μs
Input capacitance	C ₁	STHR,STHL excluded, T _A = 25 °C		5.4	15	pF
	C ₂			7.6	15	pF

Note Load condition

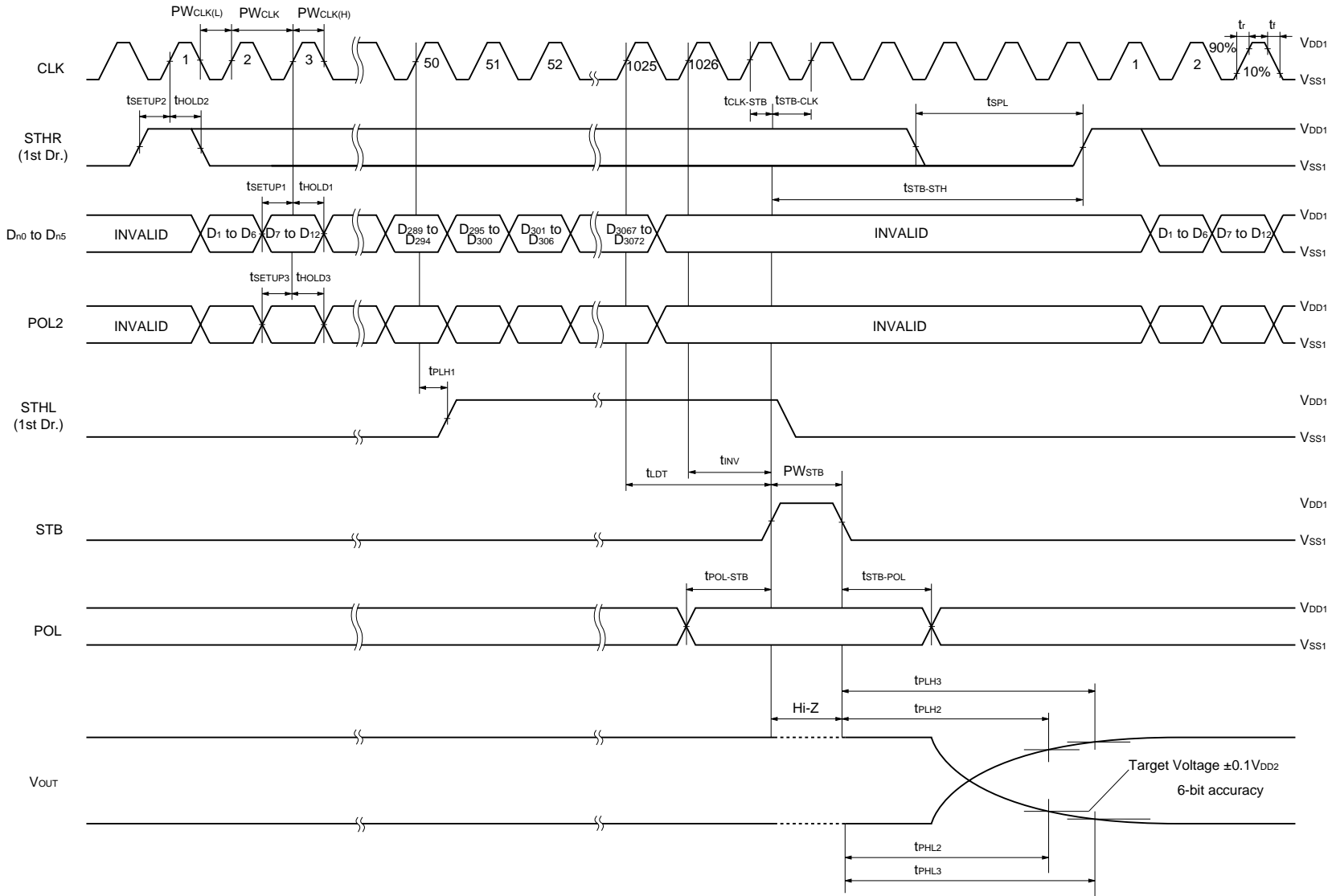


Timing Requirements ($T_A = -10$ to $+75$ °C, $V_{DD1} = 3.3$ V \pm 0.3 V, $V_{SS1} = V_{SS2} = 0$ V, $t_r = t_f = 8.0$ ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW _{CLK}		25			ns
Clock pulse low period	PW _{CLK (L)}		6			ns
Clock pulse high period	PW _{CLK (H)}		6			ns
Data setup time	t _{SETUP1}		6			ns
Data hold time	t _{HOLD1}		6			ns
Start pulse setup time	t _{SETUP2}		5			ns
Start pulse hold time	t _{HOLD2}		5			ns
Start pulse low period	t _{SPL}		6			ns
POL2 setup time	t _{SETUP3}		6			ns
POL2 hold time	t _{HOLD3}		6			ns
STB pulse width	PW _{STB}		1			μs
Data invalid period	t _{INV}		1			CLK
Final data timing	t _{LDT}		2			CLK
★ CLK-STB time	t _{CLK-STB}	CLK↑→STB↑	6			ns
★ STB-CLK time	t _{STB-CLK}	STB↑→CLK↑	6			ns
Time between STB and start pulse	t _{STB-STH}	STB↓→CLK↑	60			ns
POL-STB time	t _{POL-STB}	POL↑or↓→STB↑	-5			ns
STB-POL time	t _{STB-POL}	STB↓→POL↑or↓	6			ns

★ 11. SWITCHING CHARACTERISTIC WAVEFORM(R,/L= H)

Unless otherwise specified, the input level is defined to be 0.5 V_{DD1}.



12. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16634A.

For more details, refer to the **Semiconductor Device Mounting Technology Manual(C10535E)**.

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16634AN-xxx : TCP(TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C, heating for 2 to 3 sec ; pressure 100g(per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100 °C ; pressure 3 to 8 kg/cm ² ; time 3 to 5 sec. Real bonding 165 to 180 °C pressure 25 to 45 kg/cm ² time 30 to 40secs(When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents**NEC Semiconductor Device Reliability/Quality Control System(C10983E)****Quality Grades to NEC's Semiconductor Devices(C11531E)**

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