DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
μPD16780A

300 OUTPUT TFT-LCD SOURCE DRIVER

DESCRIPTION

The μPD16780A is a source driver for 300-output TFT-LCDs, providing support for only striped pixel array LDCs..

The driver consists of a shift register for generating the sampling timing and sample & hold circuits for sampling the analog voltage. The high picture quality obtained by the alternate sample & hold execution of the two types of on-chip sample & hold circuits enables employment in applications such as car navigation panels.

FEATURES

- 5.0 V Drive (Dynamic range 4.6 V_{P-P}, V_{DD2} = 5.0 V)
- 300 Output channel
- f_{CLK} = 20 MHz MAX. (V_{DD1} = 3.0 V)
- 1-phase/3-phase sampling clocks supported
- Corresponds only to LCD of Stripe array color filter
- Two on-chip sample-and-hold circuits
- Small output deviation between pins (deviation between chip pins: ±20 mV MAX.)
- Switch between right and left shift using the R,/L pin
- Logic power supply voltage (V_{DD1}): 3.0 to 5.5 V
- Driver power supply voltage(V_{DD2}): 5.0 ± 0.5 V

ORDERING INFORMATION

Part Number	Package
μPD16780AN-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, so please contact one of out sales representatives.

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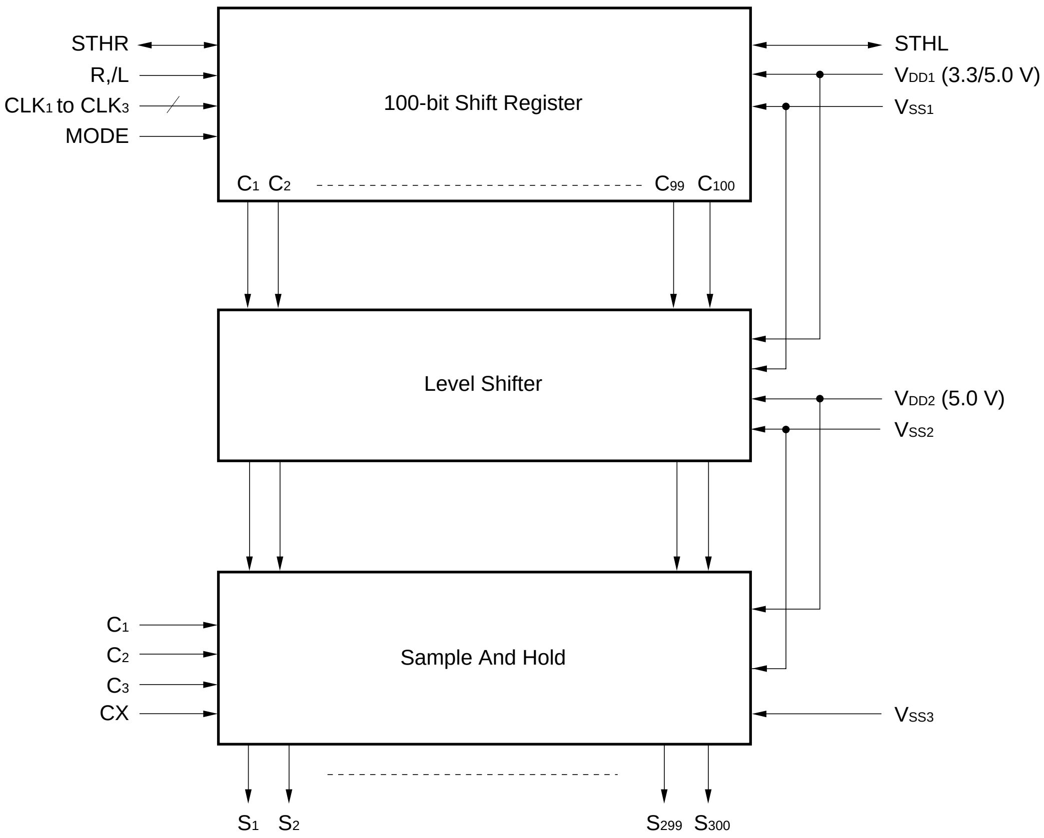
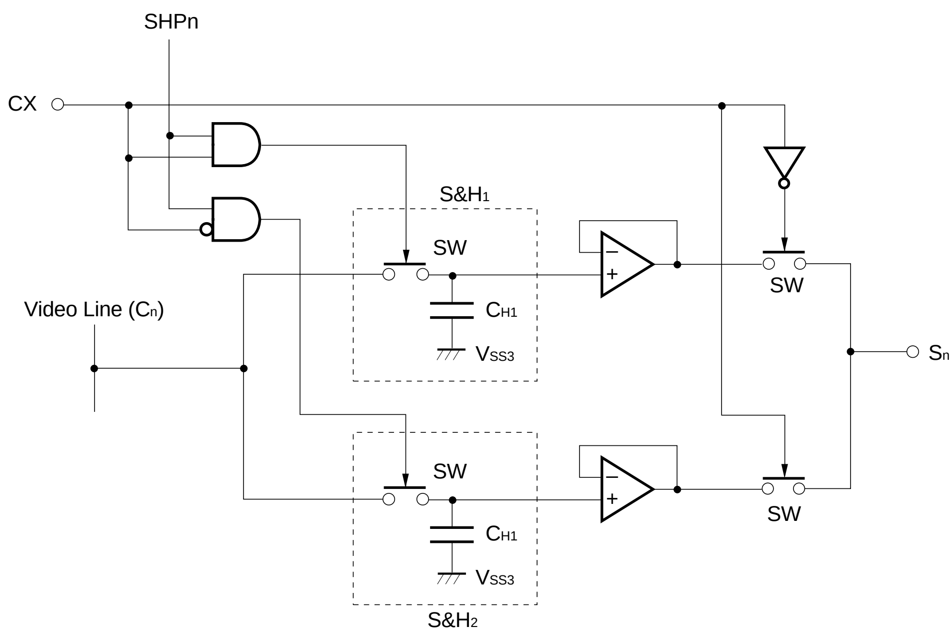
The mark ★ shows major revised points.

1. BLOCK DIAGRAM

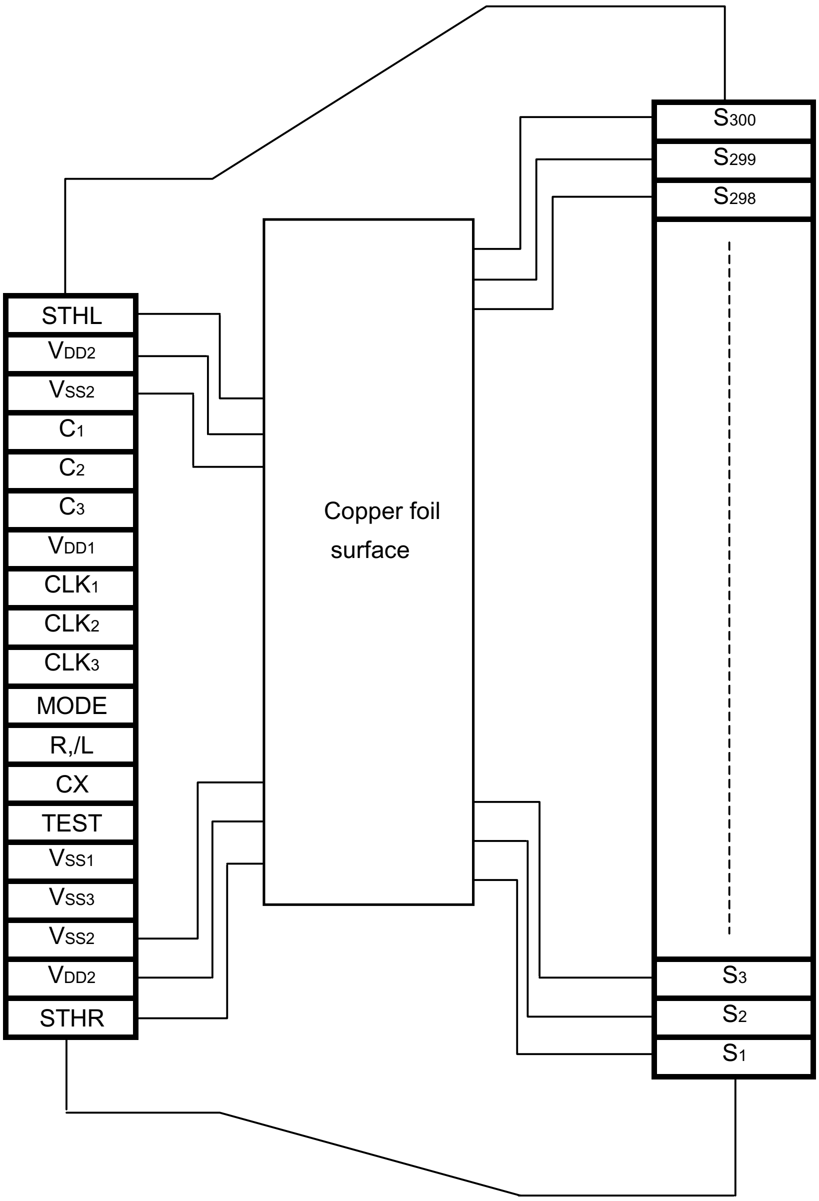


Remark /xxx indicates active low signal.

2. SAMPLE-AND HOLD CIRCUIT AND OUTPUT CIRCUIT



3. PIN CONFIGURATION (μPD16780AN-xxx) (COPPER FOIL SURFACE, FACE UP)



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
C_1, C_2, C_3	Video signal input	These pins are input video signals R,G, and B.
S_1 to S_{300}	Video signal output	These pins are output video signals, which have been sampled and hold. The relationship between the video signal input (C_1, C_2, C_3) and video signal output is shown below. C_1: S_{3n-2} (n = 1, 2, ··········100) C_2: S_{3n-1} C_3: S_{3n}
STHR, STHL	Cascade I/O	These pins are inputs/outputs for the start pulse for sample and hold timing. High level of STHR/STHL is read at rising edge of CLK and start sampling video signal. STHR serves as the input pin and STHL serves as output pin for the right shift. For left shift, STHL serves as the input pins and STHR serves as the output pin.
R,/L	Shift direction switching input	The shift directions of the shift registers are as follows. R,/L = H: STHR input, $S_1 \rightarrow S_{300}$, STHL output. R,/L = L: STHL input, $S_{300} \rightarrow S_1$, STHR output.
CLK_1 to CLK_3	Shift clock input	The start pulse is read at rising edge of CLK. The sampling pulse SHPn is generated at rising edge of CLK. For details, refer to **6. TIMING CHART**. The relationship between the clocks and the output pins is shown below. (1) When MODE = L or open (sequential sampling) CLK_1 R,/L = H: S_{3n-2} R,/L = L: S_{3n} CLK_2 :S_{3n-1} CLK_3 R,/L = H: S_{3n} R,/L = L: S_{3n-2} (1) When MODE = H (simultaneous sampling) CLK_1: S_{3n-2}, S_{3n-1}, S_{3n} (n = 1,2,·····100) CLK_2: Connect V_{DD1} or V_{SS1} CLK_3: Connect V_{DD1} or V_{SS1}
MODE	Mode select signal input pin	This pin is used to select whether the three analog input signals, C_1, C_2, and C_3 are sampled simultaneously or sequentially (This pin is pulled down in the IC). MODE = H: Simultaneous sampling MODE = L or open: Sequential sampling
CX	Hold capacitance control input	Two Sample & hold circuits are switched. CX = H S&H1: Sampling, S&H2: Output CX = L S&H1: Output, S&H2: Sampling
TEST	Test pin	Fix this pin to the L level.
V_{DD1}	Logic power supply	3.0 to 5.5 V
V_{DD2}	Driver power supply	5.0 V ± 0.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding
V_{SS3}	Sample & hold ground	It is ground of Sample & hold capacitance. Supply this terminal with the stable GND.

Cautions 1. To prevent latch-up-breakdown, the power should be turned on in order V_{DD1}, Logic input V_{DD2}, video signal input. It should be turned off in the opposite order. This relationship should be followed during transition periods as well.

2. The sampling of the video signal of this IC is only the simultaneous 3 output sampling of C_1, C_2, C_3. Incidentally, it is designing abound of the input of the video signal in 10 MHz MAX.
If a video signal with a higher frequency is input, the data may not be correctly displayed.

3. Recommend a bypass capacitor of about 0.1 μF with good high-frequency characteristics between V_{DD1} and V_{SS1}, and V_{DD2} and V_{SS2} in each driver IC.

4. If noise is superimposed on the start pulse pin, the data may not be displayed. For this reason, be sure to input CX signal during the vertical blanking period.

5. If the start pulse width is extended by half the clock or longer, the sampling start timing SHP1 does not change from normal timing; therefore, the sampling operation is performed normally.

5. FUNCTION DESCRIPTION

5.1 Switching of Sample & Hold Circuits

Two sample-and-hold circuits are switched.

CX	Output	Sample & hold operation
L	Sample & Hold Circuit 1 ($S\&H_1$)	Sample & Hold Circuit 2 ($S\&H_2$)
H	Sample & Hold Circuit 2 ($S\&H_2$)	Sample & Hold Circuit 1 ($S\&H_1$)

5.2 Sample & Hold and Output

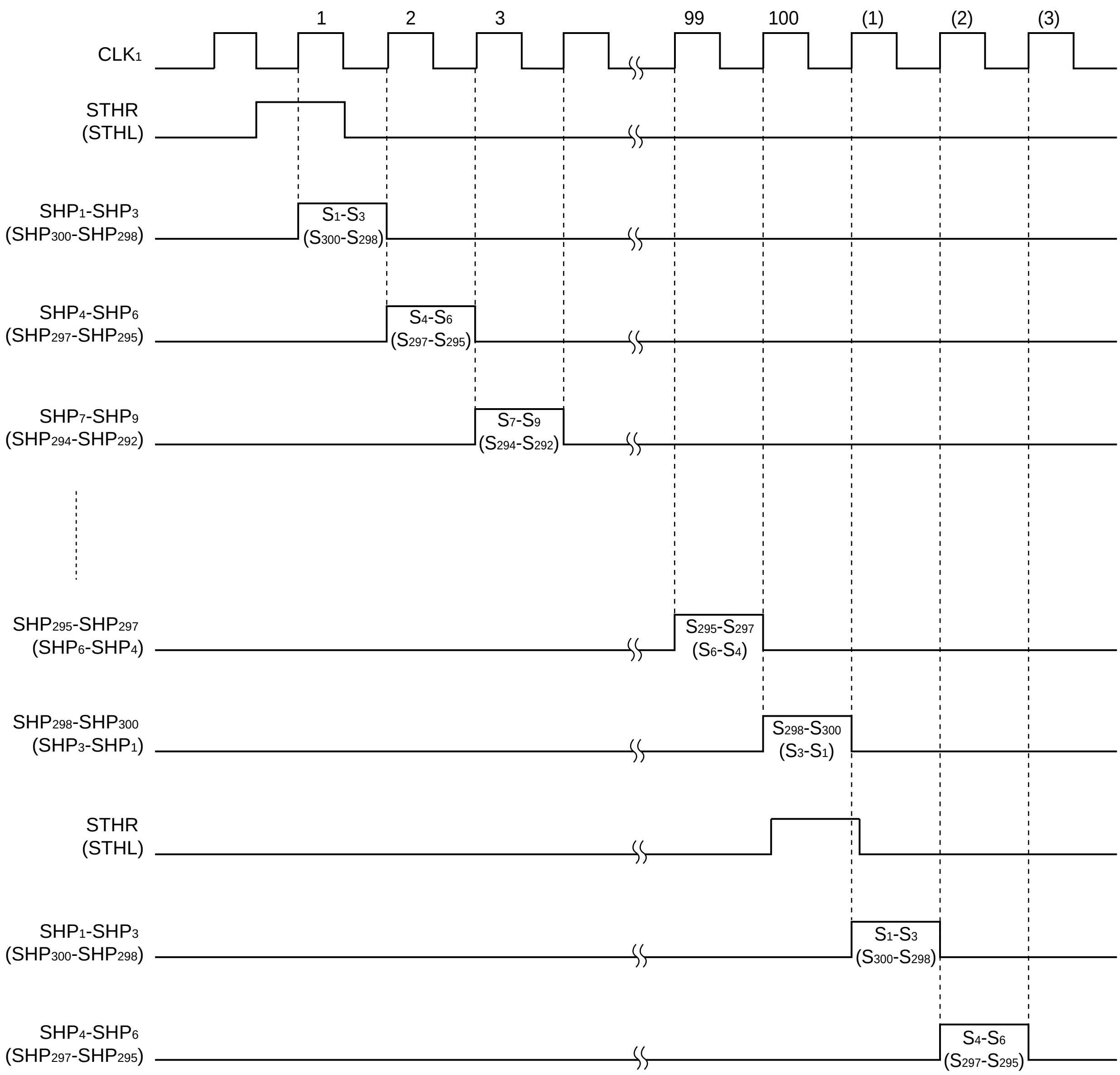
Relation between video signals C_1, C_2 and C_3 and output pins and two sample & hold circuits.

CX		S_1 (S_{300})	S_2 (S_{299})	S_3 (S_{298})	S_4 (S_{297})	···	S_{299} (S_2)	S_{300} (S_1)
L	Sampling	C_{1-2} (C_{3-2})	C_{2-2} (C_{2-2})	C_{3-2} (C_{1-2})	C_{1-2} (C_{3-2})	···	C_{2-2} (C_{2-2})	C_{3-2} (C_{1-2})
	Output	C_{1-1} (C_{3-1})	C_{2-1} (C_{2-1})	C_{3-1} (C_{1-1})	C_{1-1} (C_{3-1})	···	C_{2-1} (C_{2-1})	C_{3-1} (C_{1-1})
H	Sampling	C_{1-1} (C_{3-1})	C_{2-1} (C_{2-1})	C_{3-1} (C_{1-1})	C_{1-1} (C_{3-1})	···	C_{2-1} (C_{2-1})	C_{3-1} (C_{1-1})
	Output	C_{1-2} (C_{3-2})	C_{2-2} (C_{2-2})	C_{3-2} (C_{1-2})	C_{1-2} (C_{3-2})	···	C_{2-2} (C_{2-2})	C_{3-2} (C_{1-2})

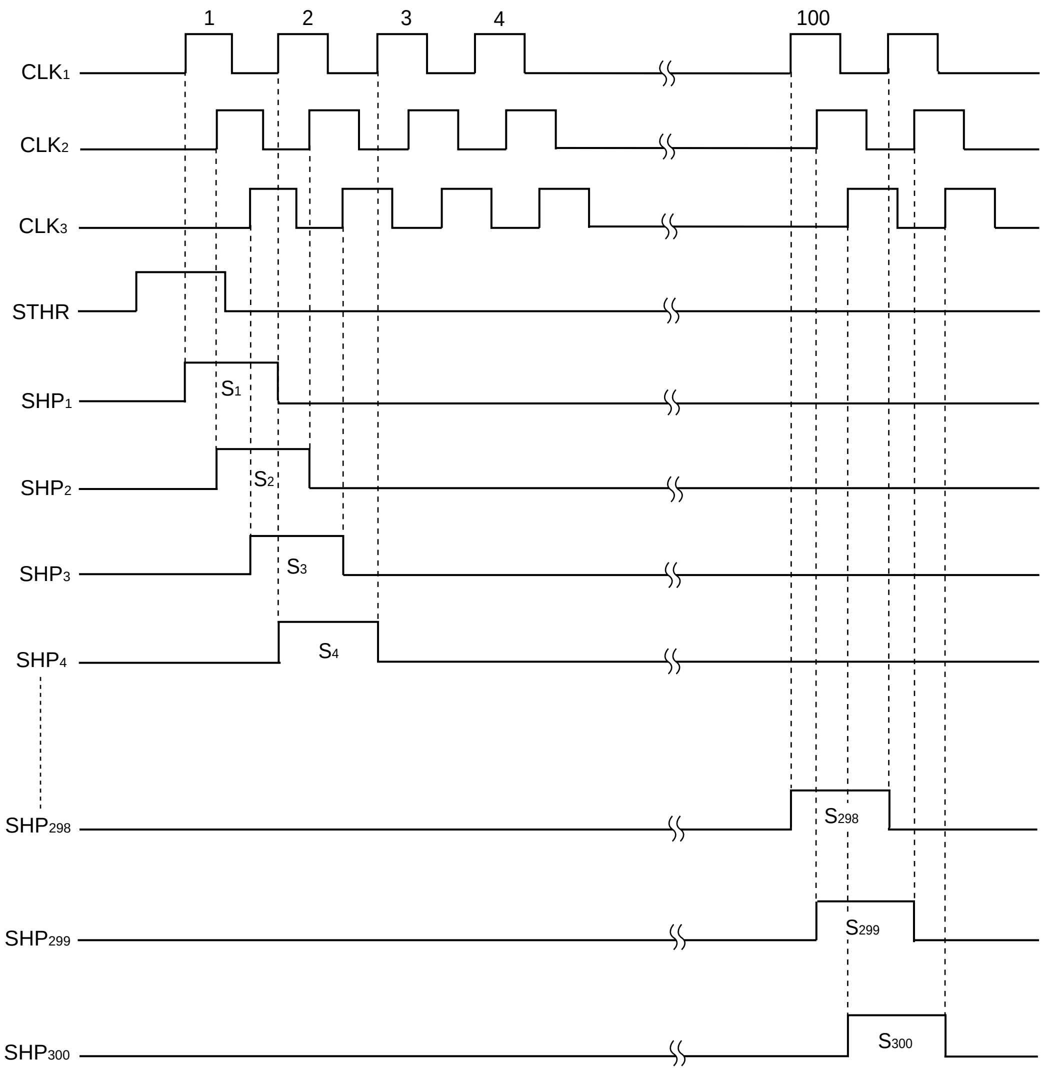
Remark C_{m-n} = m: Video input, n: Sample & Hold

6. TIMING CHART

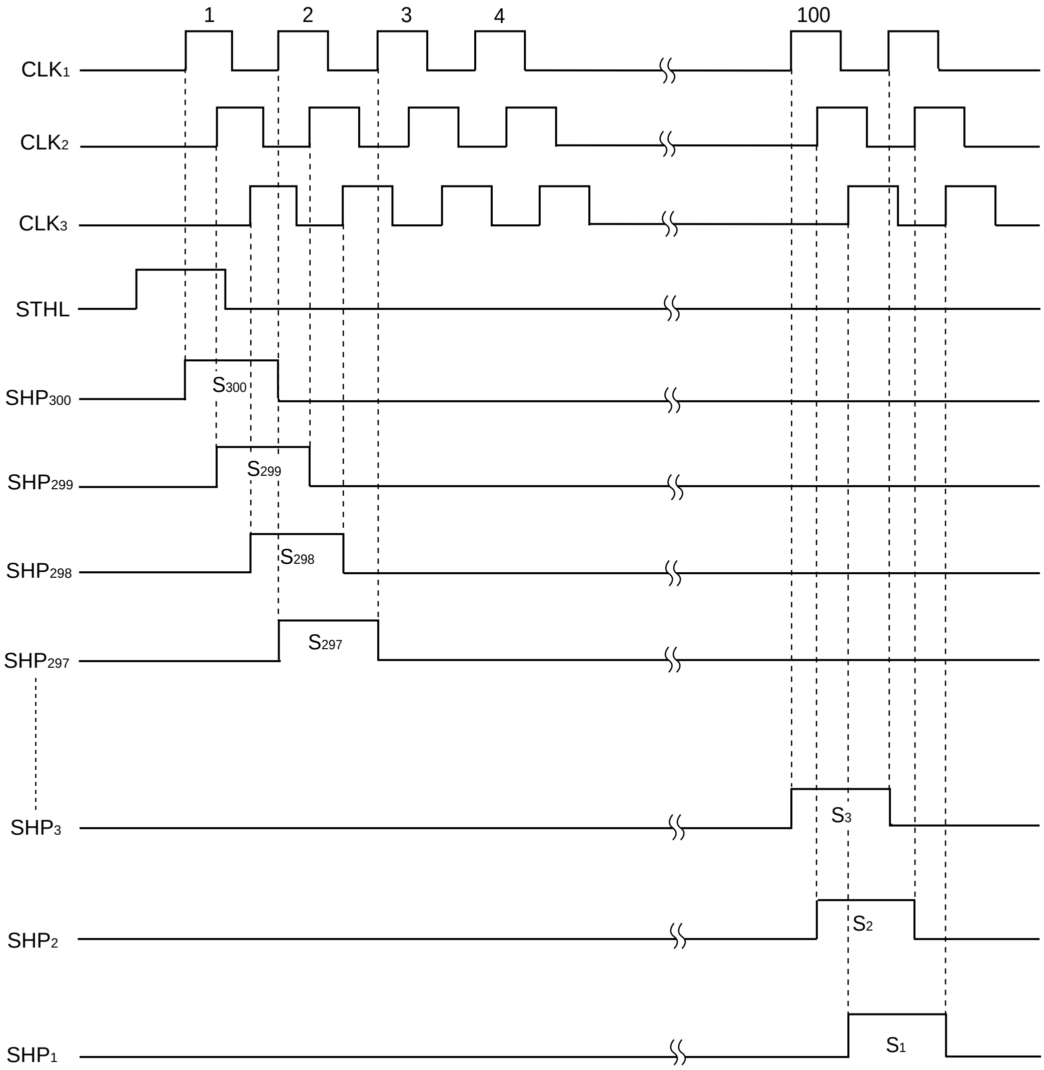
6.1 1-Phase simultaneous sampling



6.2 3-phase sequential sampling, right shift



6.3 3-phase sequential sampling, left shift



7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.3 to +7.0	V
Driver Part Supply Voltage	V_{DD2}	–0.3 to +7.0	V
Input Voltage	V_I	–0.3 to $V_{DD1/2}$ + 0.3	V
Output Voltage	V_O	–0.3 to $V_{DD1/2}$ + 0.3	V
Operating Ambient Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –30 to +85°C, $V_{DD2} \geq V_{DD1}$, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		3.0		5.5	V
Driver Part Supply Voltage	V_{DD2}		4.5	5.0	5.5	V
Video Input Voltage	V_{VI}		V_{SS2} + 0.2		V_{DD2} – 0.2	V
Driver Part Output Voltage	V_{O2}		V_{SS2} + 0.2		V_{DD2} – 0.2	V
Maximum Clock Frequency	f_{CLK}	CLK_1 to CLK_3			20	MHz
Output Load Capacitance	C_L	1 output			50	pF

Electrical Characteristics (T_A = –30 to +85°C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, $V_{DD2} \geq V_{DD1}$, $V_{SS1} = V_{SS2}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-Level Driver Part Output Voltage	V_{VOL}	S_1 to S_{300}				V_{SS2} + 0.2	V
High-Level Driver Part Output Voltage	V_{VOH}			V_{DD2} – 0.2			V
★ High-Level Input Voltage	V_{IH}	CLK, STHR (L), R,/L, CX, MODE		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}			V_{SS1}		0.3 V_{DD1}	V
Input Leak Current	I_{IL}	Except for MODE pin		–1.0		+1.0	μA
		MODE pin	V_I = 0 V	–10		+10	μA
			$V_I = V_{DD1}$ = 5 V	30		300	μA
High-Level Output Voltage	V_{LOH}	STHR (STHL), I_{OH} = –1.0 mA		0.85 V_{DD1}			V
Low-Level Output Voltage	V_{LOH}	STHR (STHL), I_{OL} = +1.0 mA				0.15 V_{DD1}	V
Reference Voltage	V_{REF1}	V_{DD2} = 5.0 V, V_{VI} = 0.5 V, T_A = 25°C			0.5		V
	V_{REF2}	V_{DD2} = 5.0 V, V_{VI} = 2.5 V, T_A = 25°C			2.5		V
	V_{REF3}	V_{DD2} = 5.0 V, V_{VI} = 4.5 V, T_A = 25°C			4.5		V
Output Voltage Deviation	ΔV_{VO1}	V_{DD2} = 5.0 V, V_{VI} = 0.5 V, T_A = 25°C				±20	mV
	ΔV_{VO2}	V_{DD2} = 5.0 V, V_{VI} = 2.5 V, T_A = 25°C				±20	mV
	ΔV_{VO3}	V_{DD2} = 5.0 V, V_{VI} = 4.5 V, T_A = 25°C				±20	mV
Logic Dynamic Current Consumption	I_{DD1}	V_{DD1} = 5.0 V with no load[Note]			1.0	3.5	mA
Driver Dynamic Current Consumption	I_{DD2}	V_{DD2} = 5.0 V with no load[Note]			7.0	10.0	mA

Note f_{CLK} = 15 MHz, f_{CX} = 17 kHz.

Switching Characteristics (T_A = –30 to +85°C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, $V_{DD2} \geq V_{DD1}$, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PHL1}	C_L = 20 pF	7		43	ns
	t_{PLH1}	CLK → STHL(STHR)	7		43	ns
Driver Output Delay Time	t_{PLH2}	V_{DD2} = 5.0 V			8	μs
	t_{PLH3}	R_L = 2 kΩ			16	μs
	t_{PHL2}	C_L = 25 pF x 2			8	μs
	t_{PHL3}				16	μs
Input Capacitance	C_{I1}	STHR(STHL), T_A=25°C		10	20	pF
	C_{I2}	C_1,C_2,C_3, T_A=25°C		40	60	pF
	C_{I3}	STHR(STHL),C_1,C_2,C_3 excluded input, T_A=25°C		7	15	pF

Timing Requirement (T_A = –30 to +85°C, V_{DD1} = 3.0 to 5.5 V, V_{SS1} = 0 V)

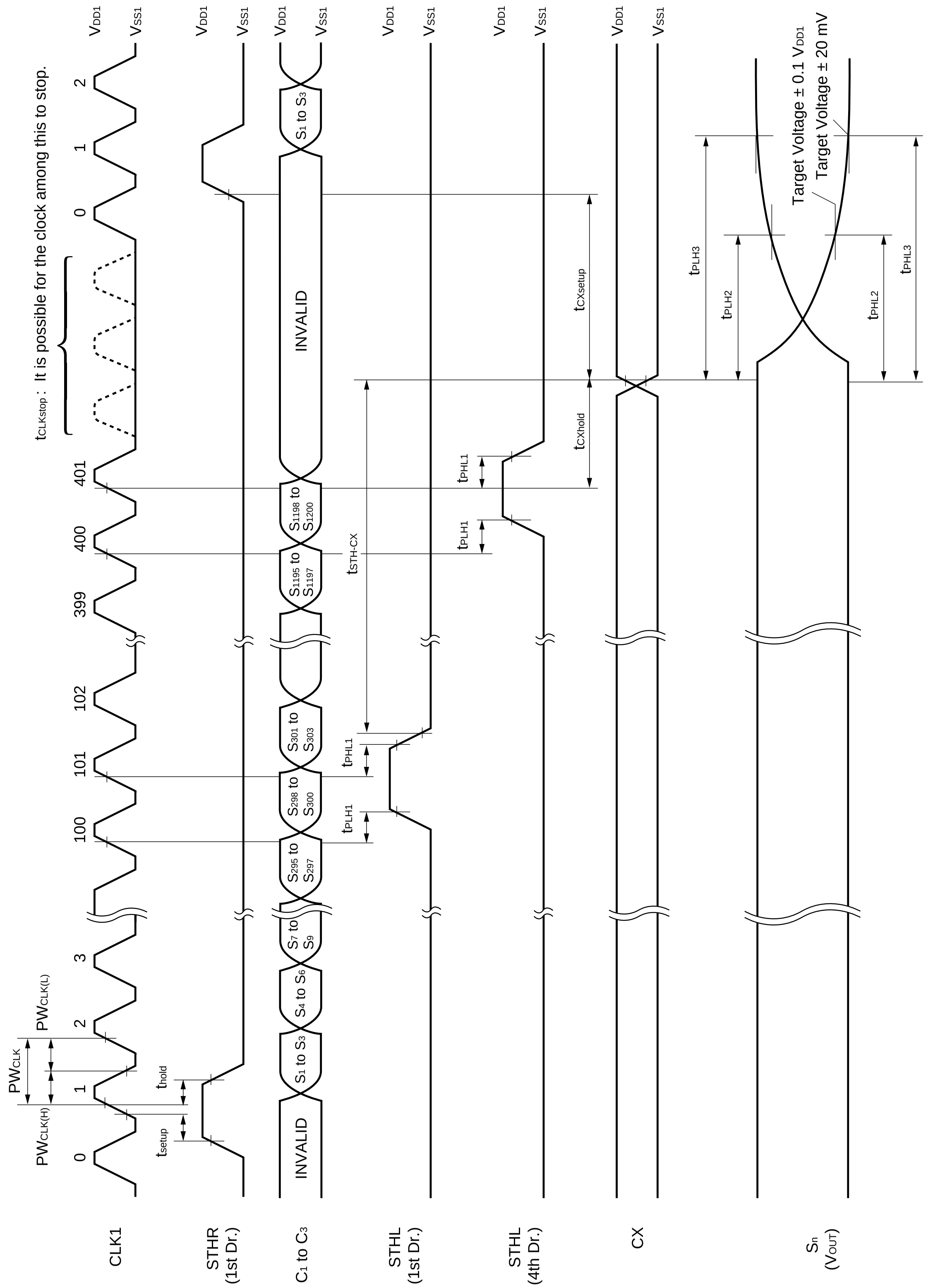
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}	CLK_1 to CLK_3	50			ns
Clock Pulse High Period	$PW_{CLK(H)}$		15			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		15			ns
★ Clock Delay Time	t_{CL1-2} t_{CL2-3}		16.6		$\frac{PW_{CLK}}{2}$	ns
Start Pulse Setup Time	t_{setup}		7			ns
Start Pulse Setup Time	t_{hold}		7			ns
Start Pulse – CX Time	t_{STH-CX}		50			ns
CX Setup Time	$t_{CXsetup}$		1.0			μs
CX Hold Time	t_{CXhold}		50			ns
CLK Stop Period	$t_{CLKstop}$		Refer to **8. SWITHING CHARACTERISTICS WAVEFORM.**			

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

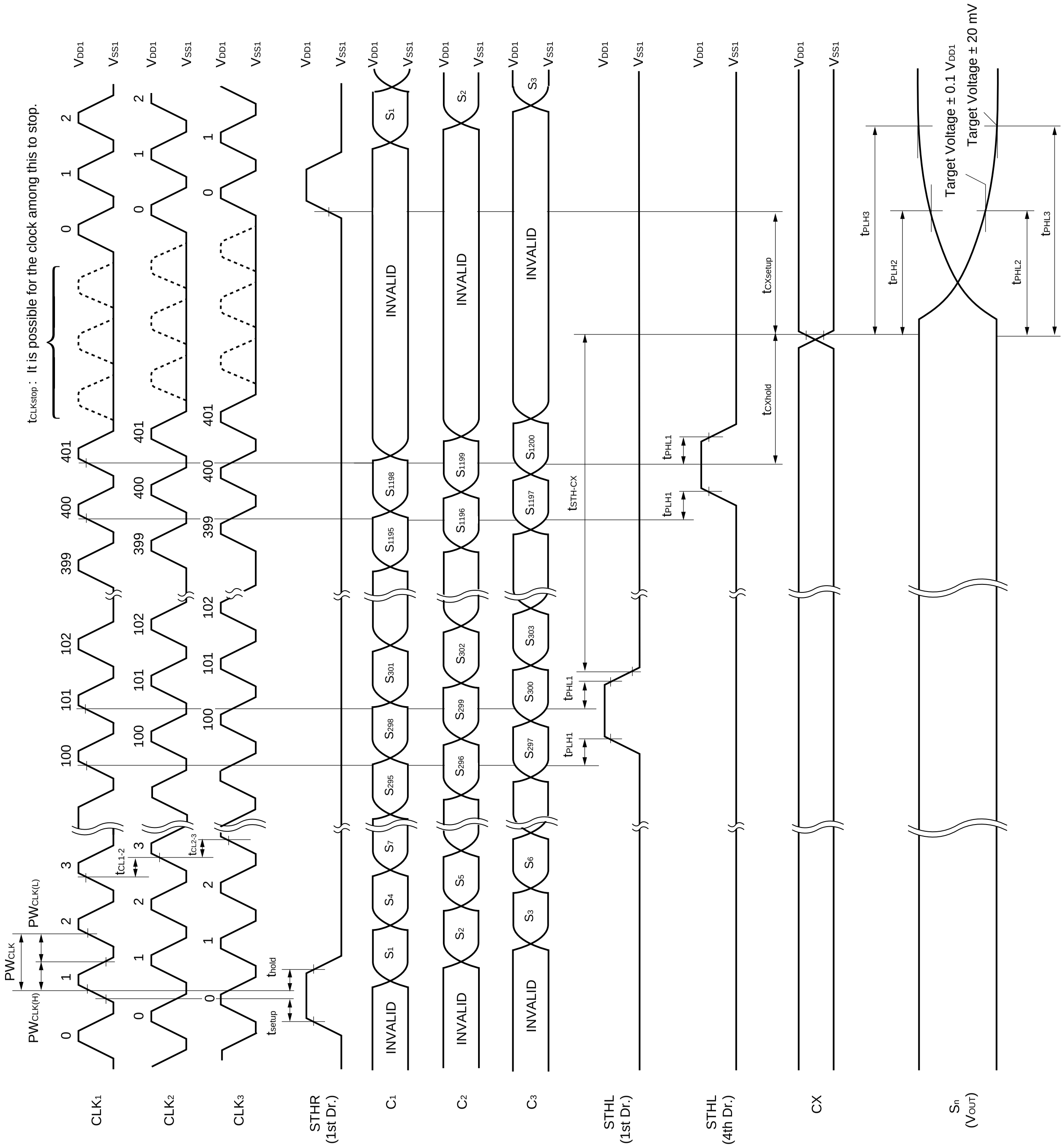
8. SWITCHING CHARACTERISTICS WAVEFORM (R,/L=H)

Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7\ V_{DD1}$, $V_{IL} = 0.3\ V_{DD1}$.

8.1 1-Phase simultaneous sampling



★ 8.2 3-phase sequential sampling



9. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16780A.
For more details, refer to the **Semiconductor Device Mounting Technology Manual(C10535E).**
Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16780AN-xxx : TCP(TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec ; pressure 100g(per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C ; pressure 3 to 8 kg/cm2; time 3 to 5 sec. Real bonding 165 to 180°C pressure 25 to 45 kg/cm2 time 30 to 40 secs (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System(C10983E)

Quality Grades to NEC's Semiconductor Devices(C11531E)