AP9A106

64K x 18 CMOS Static RAM

Features

- Fast access times: 17*, 20, 25, 35 ns
- Wide Word (18-bits) for:
  - Improved performance
  - Reduced component count
  - 9-bit byte for parity
- Transparent address latch
- Reduced loading on address bus
- Low-power stand-by mode when deselected
- TTL-compatible I/O
- 5 V ± 10% supply
- JEDEC-standard pinout
- 2V data retention
- 52-pin PLCC package

Functional Description

The Aptos AP9A106 is a high speed, 1-Megabit, CMOS static RAM organized as a 64K x 18. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells. The AP9A106 is available in a compact 52-pin PLCC, which along with six pairs of supply terminals, provide for reliable operation.

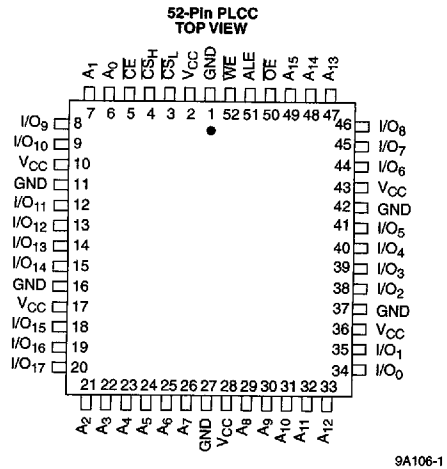
The control signals include Write Enable ($\overline{WE}$), Chip Enable ($\overline{CE}$), High and Low Byte Select ($\overline{CS}_L$ and $\overline{CS}_H$), Output Enable ($\overline{OE}$), and Address Latch Enable (ALE). The wide word provides for reduced component count, improved density, reduced Address bus loading and improved performance. The wide word also allows for byte parity with no additional RAM required.

This RAM is fully static in operation. The chip enable control permits read and write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). The byte-select controls are also used to enable or disable Read and Write operations on the high and low bytes. The address latches are transparent when ALE is HIGH (for applications not requiring a latch), an are latched when ALE is LOW. The address latches and the wide word help to eliminate the need for external address bus buffers and/or latches.

Write cycles occur when chip enable, byte-select controls, and write enable are LOW. The byte-select signals can be used for byte-write operations by disabling the other byte during the Write operation. Data is transferred from the I/O pins to the memory location specified by the 16 address lines. The proper use of the output enable control can prevent bus contention.

When $\overline{CE}$ and either $\overline{CS}_H$ or $\overline{CS}_L$ are LOW and $\overline{WE}$ is HIGH, a static read will occur at the memory location specified by the address lines. $\overline{OE}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new read cycles can be performed by simply changing the address with ALE HIGH.

Pin Configuration

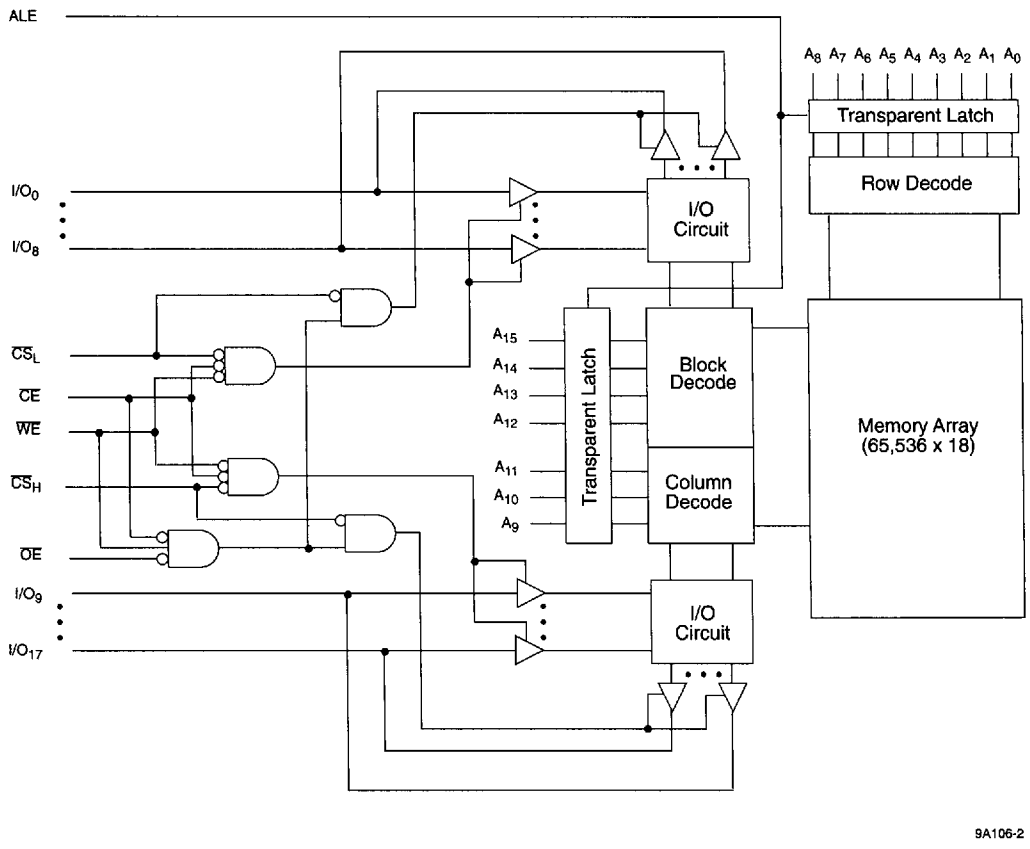


Selection Guide

	AP9A106-17*	AP9A106-20	AP9A106-25	AP9A106-35
Maximum Access Time (ns)	17	20	25	35
Maximum Operating Current (mA)	300	300	300	300
Maximum Standby Current (mA)	50	50	50	50

*Preliminary

Block Diagram



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....-65° C to +150 ° C
V_{CC} Supply Relative to GND .....-0.5 V to +7.0 V

Short Circuit Output Current[1].....±40 mA
Voltage on any Pin Relative to GND....-0.5 to V_{CC} +0.5 V
Power Dissipation.....2.0 W

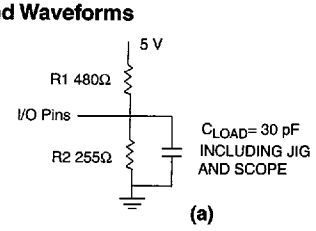
Electrical Characteristics Over the Operating Range ($0°C \le T_A \le 70°C$, V_{CC} = 5V ±10%)

Symbol	Parameter	Test Conditions	9A106-17		9A106-20		9A106-25		9A106-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Operating Current[2]			300		300		300		300	mA
I_{SB1}	Standby Current	$\overline{CE} \ge V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}		50		50		50		50	mA
I_{SB2}	Standby Current	$\overline{CE} \ge V_{CC}$ -0.2 V, $V_{IN} \ge V_{CC}$ -0.2 V or $V_{IN} \le 2.0$ V, f=0		4		4		4		4	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	-2	2	-2	2	-2	2	-2	2	µA
I_{LO}	Output Leakage Current	V_{IN} = 0 V to V_{CC}	-2	2	-2	2	-2	2	-2	2	µA
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage[3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

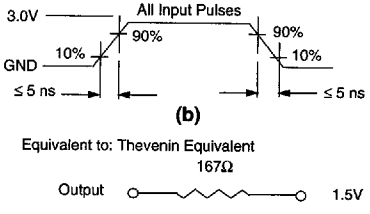
Capacitance[4, 5]

Symbol	Description	Max.	Unit
C_{IN}	Input Capacitance	5	pF
C_{IO}	I/O Capacitance	7	pF

AC Test Loads and Waveforms



(a)



(b)

Notes:

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.
3. Negative undershoot of up to 3.0 V is permitted once per cycle.
4. Capacitances are maximum values at 25°C measured at 1 MHz with V_{CC} = 5.0V.
5. Guaranteed but not tested.

Switching Characteristics Over the Operating Range ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$) [7]

Parameter	Description	9A106-17		9A106-20		9A106-25		9A106-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	17		20		25		35		ns
t_{AA}	Address Access Time		17		20		25		35	ns
t_{ASL}	Address Set-up to Latch Enable	2		2		2		2		ns
t_{AHL}	Address Hold from Latch Enable	3		4		4		4		ns
t_{LEA}	Latch Enable to Valid Data		18		21		26		36	ns
t_{LHM}	Latch Enable High Pulse Width	5		5		5		5		ns
t_{OHA}	Output Hold Time	4		4		4		4		ns
t_{LH}	Output Hold from Latch High	4.5		4.5		4.5		4.5		ns
t_{ACE}	$\overline{CE}$ LOW to Valid Data		17		20		25		35	ns
t_{LZCE}	$\overline{CE}$ to LOW Output Active [8, 9]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ to High-Z Output [8, 9]		10		10		12		20	ns
t_{CSA}	$\overline{CS}$ LOW to Valid Data		8		10		12		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Output Active	2		2		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High-Z Output		10		10		12		20	ns
t_{OEA}	$\overline{OE}$ LOW to Valid Data		8		9		12		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Output Active [8, 9]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z Output [8, 9]		8		8		10		20	ns
t_{RCS}	Read Set-up from $\overline{WE}$ HIGH	0		0		0		0		ns
t_{RCH}	Read Hold from $\overline{WE}$ LOW	0		0		0		0		ns
t_{PU}	$\overline{CE}$ LOW to Power Up [8]	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down [8]		17		20		25		35	ns
t_{WA}	Access Time from $\overline{WE}$ HIGH		19		20		25		35	ns
Write Cycle										
t_{WC}	Write Cycle Time	17		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		13		20		30		ns
t_{CSW}	$\overline{CS}$ LOW to End of Write	8		10		20		30		ns
t_{AW}	Address Valid to End of Write	12		13		20		30		ns
t_{HA}	Address Hold to Write End	0		0		0		0		ns
t_{SA}	Address Set-up to Write Time	0		0		0		0		ns
t_{ASL}	Address Set-up to Latch Enable	2		2		2		2		ns
t_{AHL}	Address Hold from Latch Enable	3		4		4		4		ns
t_{LHWE}	Latch Hold from $\overline{WE}$ HIGH	0		0		0		0		ns
t_{LHP}	Latch Enable HIGH Pulse Width	5		5		5		6		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		13		20		30		ns
t_{SD}	Data Set-up to Write End	8		9		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z Outputs [8, 9]		8		8		10		14	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output [8, 9]	3		3		3		3		ns

Notes:

7. AC Electrical Characteristics specified at 'AC Test Conditions' levels.

8. Active output-to-High-Z and High-Z-to-output active tests specified to a ±500 mV transition from steady state levels into the testload. $C_{LOAD} = 5$ pF.

9. Guaranteed but not tested.

Pin Definitions

V_{CC} - Positive Supply Voltage Terminals

GND - Reference Terminals

A_0 - A_{15} - Address Bus, Input
The address bus is decoded to select one 18-bit word out of the total 64K words for read and write operations.

$\overline{CE}$ - Chip Enable, Active LOW Input
Chip Enable is used to enable the device for read and write operations. When HIGH, both read and write operations are disabled and the device is in a reduced-power state. When LOW, a read or write operation is enabled.

$\overline{WE}$ - Write Enable, Active LOW Input
Write enable is used to select either read or write operations when the device is enabled. When write enable is HIGH and the device is enabled, a read operation is selected. When write enable is LOW and the device is enabled, a write operation is available by using the Byte-select controls.

$\overline{CS}_H$, $\overline{CS}_L$ - Chip Select HIGH, Chip Select LOW, Active LOW Inputs
The Chip Select HIGH and Chip Select LOW signals, in conjunction with the chip enable and write enable signals, allow the selection of the individual bytes for read and write operations. When HIGH, the Select signal will deselect its byte and prevent read or write operations. When the dhip select signal is LOW and chip enable is LOW, a read or write operation is performed at the location determined by the contents of the address bus. When chip enable is HIGH, the chip select signals are Don't Care. $\overline{CS}_L$ is assigned to I/O_0 - I/O_8 and $\overline{CS}_H$ is assigned to I/O_9 - I/O_{17}.

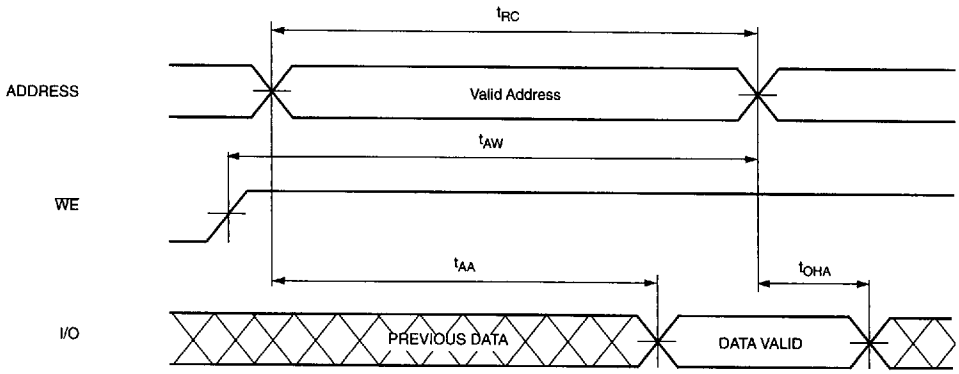
ALE - Address Latch Enable, Active HIGH Input
The Address Latch Enable signal is used to control the transparent latches on the address bus. The latches are transparent when HIGH and are latched when LOW. If not required, address latchenable may be tied HIGH, leaving the address bus in a transparent condition.

I/O_0 - I/O_{17} - Data Bus, Input/Output
I/O_0 - I/O_{17} comprise the Low byte, selected by $\overline{CS}_L$, and I/O_9 - I/O_{17} comprise the High data byte, selected by $\overline{CS}_H$. The data bus is in a high impedance input mode during write operations and standby. The data bus is in a low-impedance output mode during read operations.

$\overline{OE}$ - Output Enable, Active LOW Input
The output enable signal is used to control the output buffers on the data input/output bus. When $\overline{OE}$ is HIGH, all output buffers are forced to a high-impedance condition. When $\overline{OE}$ is LOW, the output buffers will become active only during a read operation ($\overline{CE}$ and $\overline{CS}_H$/$\overline{CS}_L$ are LOW, $\overline{WE}$ is HIGH).

Switching Waveforms

Read Cycle No. 1[10] (Unlatched Address Controlled Read, ALE is HIGH, $\overline{CE}$ and $\overline{OE}$ are LOW)



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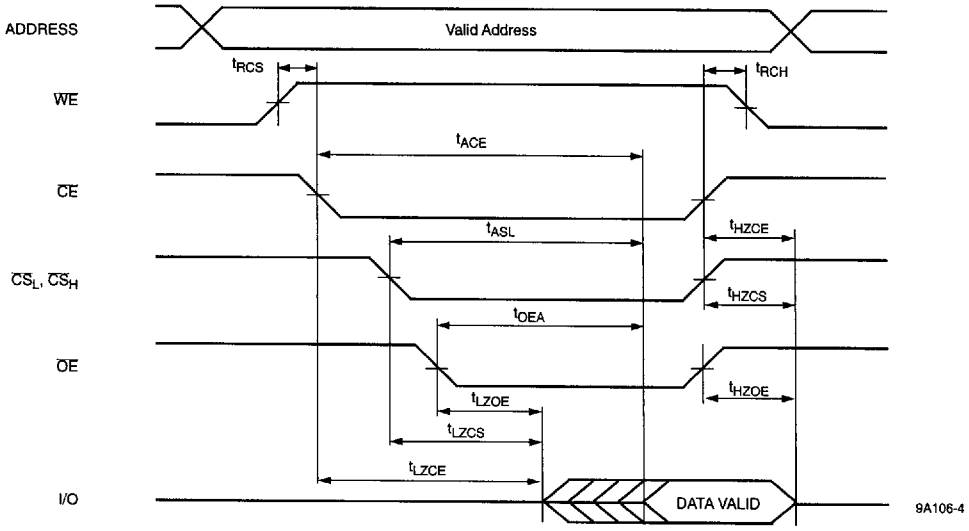
Read Cycle No. 2[11] (Unlatched Chip Enable Controlled Read, ALE is HIGH)



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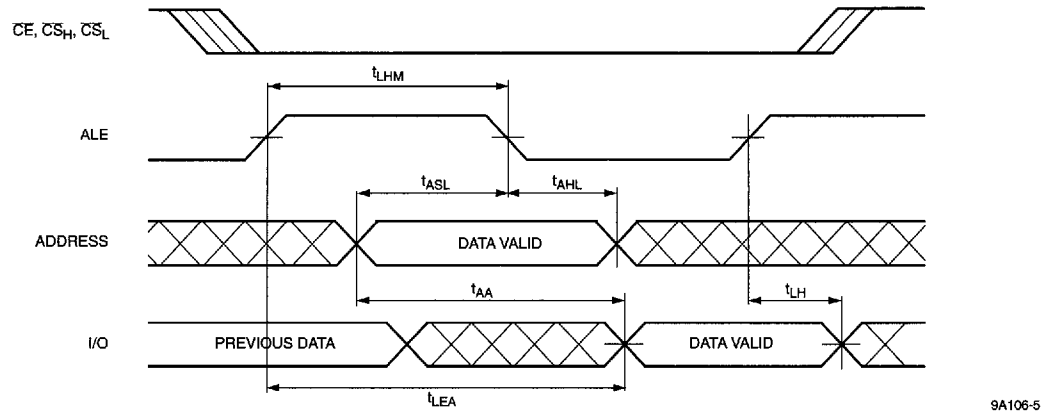
Notes:

10. Read cycle timing is referenced from when all addresses are stable until the first address transition. Following $\overline{WE}$-controlled Write cycle, t_{WA} and t_{AA} must both be satisfied to ensure valid data. Cross hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

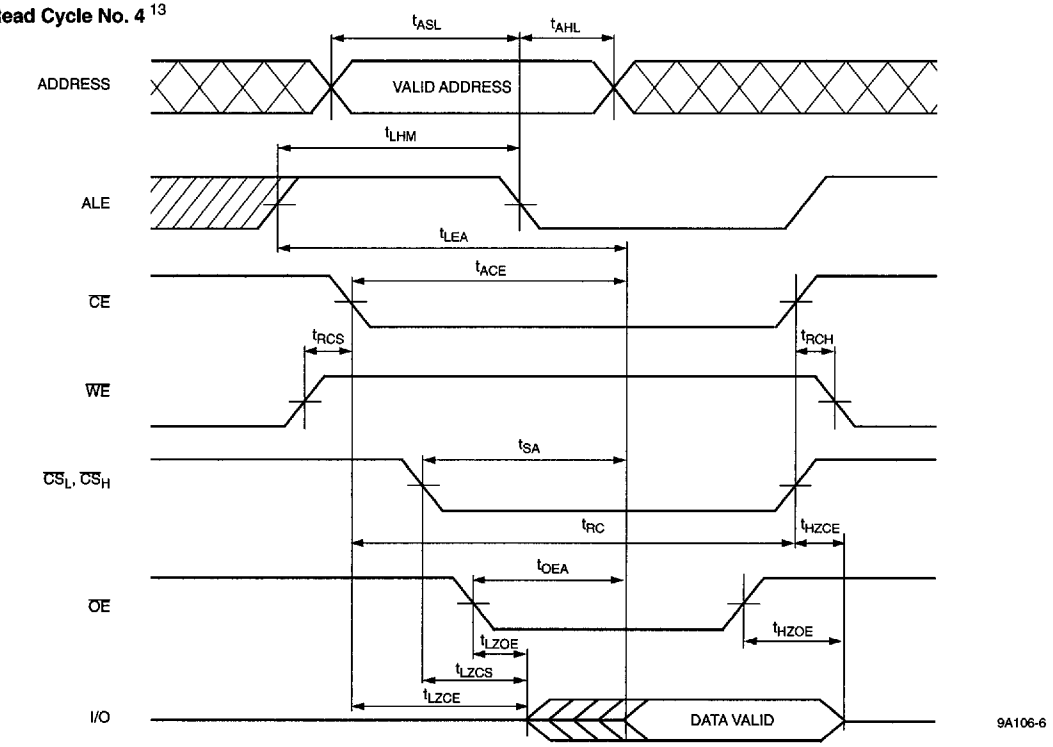
11. Read cycle timing is referenced from when $\overline{CE}$, $\overline{CS}$ and $\overline{OE}$ are stable until the first address transition. Cross hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid.

Switching Waveforms (continued)

Read Cycle No. 3 [12] (Latched Address Controlled Read, $\overline{WE}$ is HIGH, $\overline{CE}$, $\overline{CS}_H$, $\overline{CS}_L$ and $\overline{OE}$ are LOW)



Read Cycle No. 4 [13]



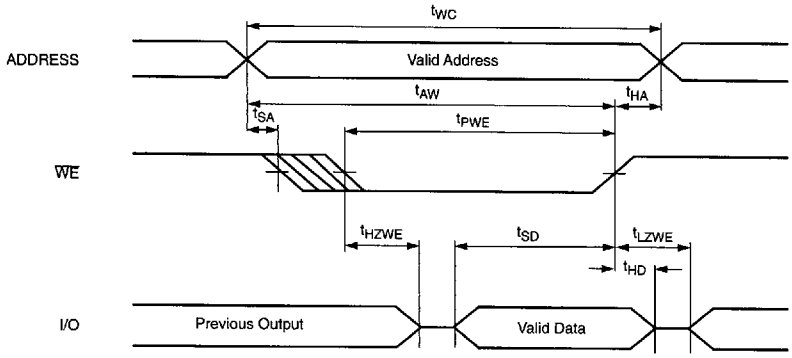
Notes:

12. Both t_{AA} and t_{LEA} must be met before valid data is available. If the address is valid prior to the rising edge of ALE, then the access time is t_{LEA}. If the address is valid after ALE is HIGH (or if ALE is tied HIGH) then the access time is t_{AA}. Crosshatched portion of the data out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

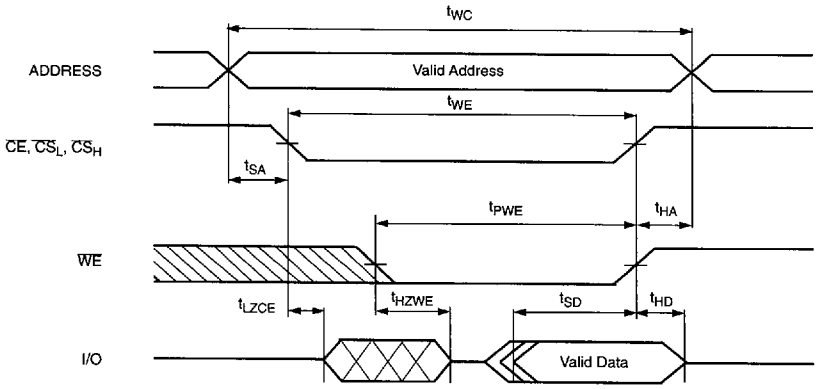
13. Timing illustrated for the case when addresses are valid before $\overline{CE}$ goes LOW. Data out is not specified to be valid until t_{EA}, t_{SA}, and t_{OEA}, but may become asserted as early as t_{LZCE}, t_{LZCS}, or t_{LZOE}.

Switching Waveforms (continued)

Write Cycle No. 1 (Unlatched $\overline{WE}$ controlled write, $\overline{CE}$, $\overline{OE}$, $\overline{CS}_H$ and $\overline{CS}_L$ are LOW and ALE is HIGH)[14, 15]



Write Cycle No.2 ($\overline{WE}$, $\overline{CS}_L$, $\overline{CS}_H$ Controlled Write, $\overline{OE}$ is LOW) [14, 16]



Notes:

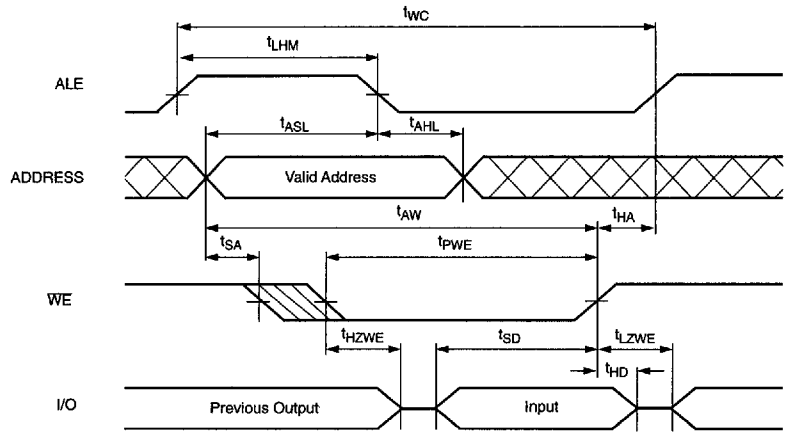
14. Addresses must be stable during unlatched Write cycles. The outputs will remain in the High-Z state if $\overline{WE}$ is LOW when $\overline{CE}$ and $\overline{CS}_H$ and $\overline{CS}_L$ go LOW. If $\overline{OE}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{OE}$ active, it is recommended that $\overline{OE}$ be held HIGH for all Write cycles. This will prevent the outputs from being asserted, preventing bus contention and reducing system noise.

15. Using only $\overline{WE}$ to control Write cycles may not offer the best performance since both t_{HZWE} and t_{SD} timing specifications must be met.

16. I/O lines may transition to Low-Z if the falling edge of $\overline{WE}$ occurs after the falling edge of $\overline{CE}$, $\overline{CS}_H$, $\overline{CS}_L$ if $\overline{OE}$ is LOW.

Switching Waveforms (continued)

Write Cycle No.3 (Latched $\overline{WE}$ controlled write, $\overline{CE}$, $\overline{OE}$, $\overline{CS}_H$ and $\overline{CS}_L$ are LOW)[14]



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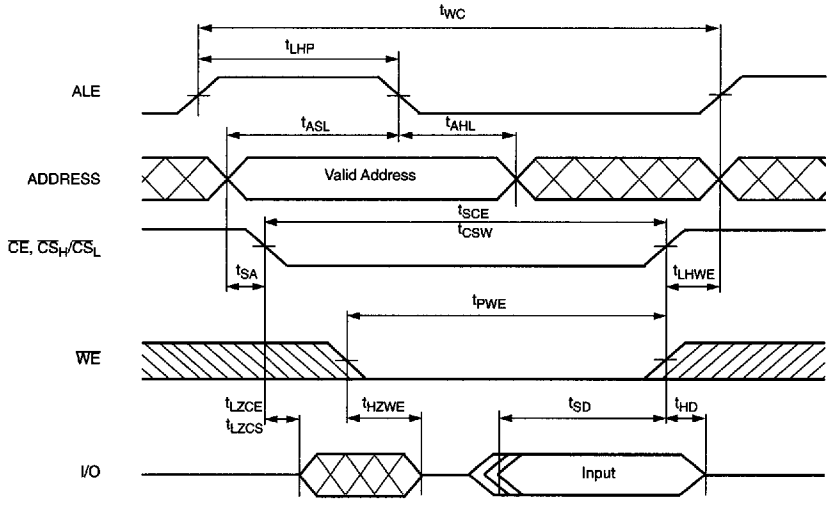
Write Cycle No.4 ($\overline{WE}$ controlled, $\overline{OE}$ is LOW) [14, 16]



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Note:

17. I/O lines may transition to Low-Z if the falling edge of $\overline{WE}$ occurs after the falling edges of $\overline{CE}$ and $\overline{CS}_H/\overline{CS}_L$.

Byte Operations

Byte Read

To read individual bytes, the device must be enabled ($\overline{CE}$ is LOW), $\overline{WE}$ must be HIGH, the outputs must be enabled ($\overline{OE}$ is LOW), and the addresses must be either stable or latched with ALE. The following byte read diagram shows one example of the byte read capabilities of this device. The example shows two read operations. The first is a read of the high byte of the current memory location and the second is a read of the low byte of the memory location.

(a) At the beginning of the cycle, both $\overline{CS}_L$ and $\overline{CS}_H$ are HIGH.

(b) $\overline{CS}_H$ goes LOW initiating a read on the upper byte I/O_{9-17}. $\overline{CS}_L$ remains HIGH keeping the lower byte (I/O_{0-8}) disabled and in a high-impedance mode.

(c) $\overline{CS}_L$ goes LOW, activating I/O_{0-8}. Valid data is available in t_{SLA} following $\overline{CS}_L$ going LOW.

(d) When $\overline{CS}_H$ goes HIGH, I/O_{9-17} remains valid for t_{HZCS} before returning to a high-impedance mode.

(e) Finally, the Read for the lower byte is terminated by deasserting $\overline{CS}_L$ (HIGH). I/O_{0-8} remains active for t_{HZCS} following $\overline{CS}_L$ going HIGH.

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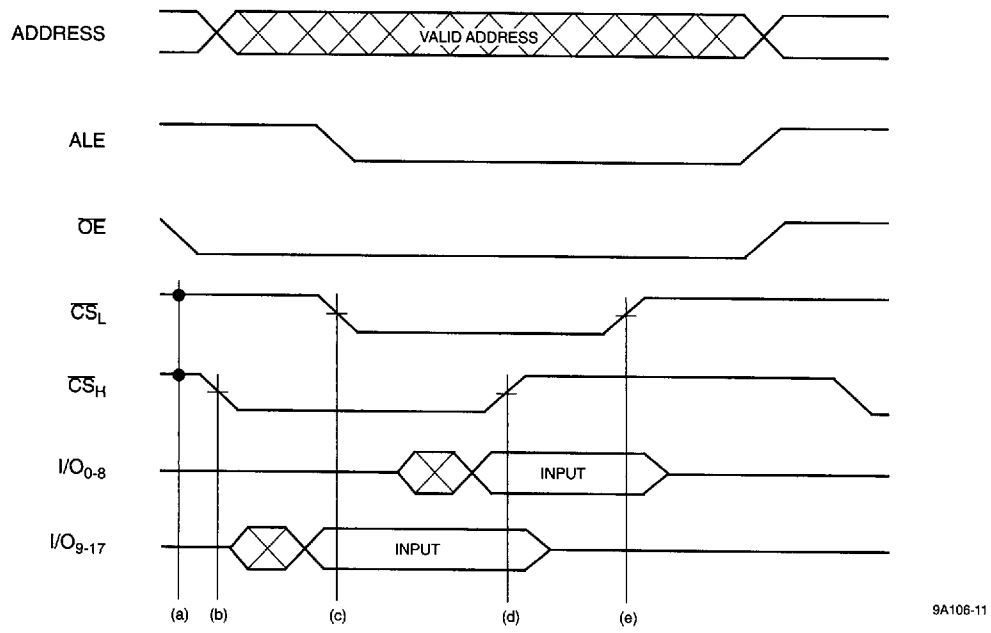
Switching Waveforms (continued)

Byte Read Operation ($\overline{CE}$ is LOW and $\overline{WE}$ is HIGH)



Byte Operations (continued)

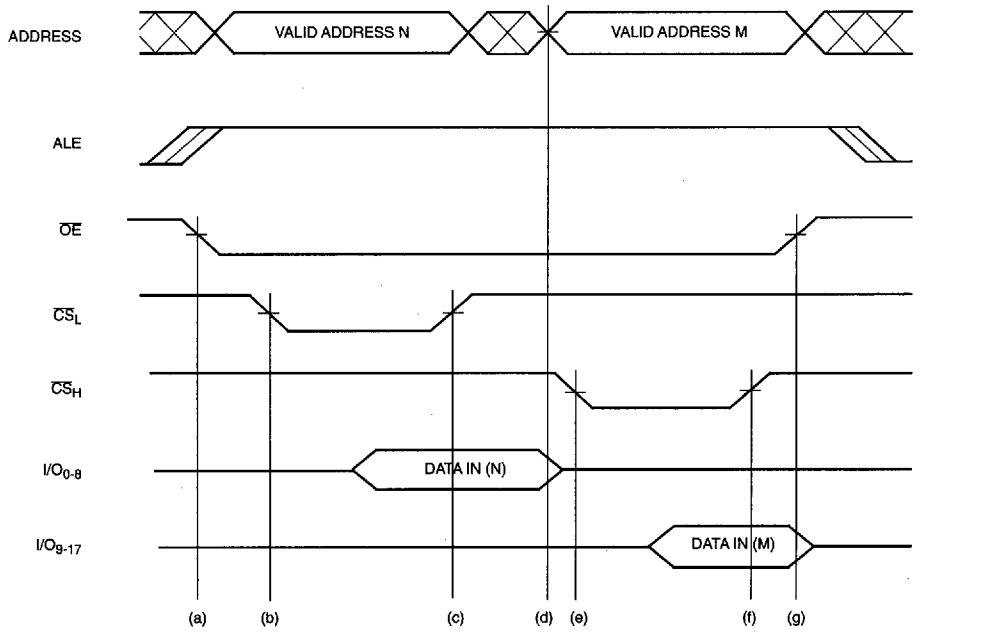
Byte Write

To do individual byte-write operations, the device must be enabled ($\overline{CE}$ is LOW, $\overline{OE}$ is don't care) and addresses must be either stable or latched. The following diagram shows an example of the byte-write capabilities of this device. It illustrates two write operations with unlatched addresses. The first is a write to the low byte of memory location N and the second is a write to the high byte of memory location M.

(a) $\overline{WE}$ goes LOW while $\overline{CS}_L$ and $\overline{CS}_H$ remain HIGH.
(b) $\overline{CS}_L$ goes LOW initiating a write into the lower byte I/O_{0-8} of memory location N. $\overline{CS}_H$ remains HIGH preventing a write into the upper byte I/O_{9-17} of memory location N.
(c) $\overline{CS}_L$ goes HIGH, terminating the write operation on the lower byte of memory location N.
(d) Address N is changed to M.
(e) The write operation is now initiated on the upper byte I/O_{9-17} by bringing $\overline{CS}_H$ LOW. $\overline{CS}_L$ remains HIGH preventing a write operation from occurring in the lower byte I/O_{0-8} of memory location N+1.
(f) $\overline{CS}_H$ now goes HIGH, terminating the write operation on the upper byte of address M.
(g) $\overline{WE}$ goes HIGH, ending the write operation.

Switching Waveforms (continued)

Byte Write Operation ($\overline{CE}$ is LOW)



Truth Table

Mode	$\overline{CE}$	$\overline{CS_H}$	$\overline{CS_L}$	ALE	$\overline{OE}$	$\overline{WE}$	I/O_{0-8}	I/O_{9-17}	I_{CC}	Address
Standby	H	X	X	H	X	X	High-Z	High-Z	Standby	Don't Care
Read	L	L	H	H	L	H	Active	High-Z	Active	Valid
Read	L	H	L	H	L	H	High-Z	Active	Active	Valid
Read	L	L	L	H	L	H	Active	Active	Active	Valid
Read	L	L	L	H	H	H	High-Z	High-Z	Active	Valid
Read	L	L	L	L	L	H	Data Out	Data Out	Active	Don't Care
Write, low byte	L	L	H	H	X	L	Data In	Don't Care	Active	Valid
Write, high byte	L	H	L	H	X	L	Don't Care	Data In	Active	Valid
Write, both bytes	L	L	L	H	X	L	Data In	Data In	Active	Valid
Write, inhibited	L	H	H	H	X	L	Don't Care	Don't Care	Active	Valid
Write, both bytes	L	L	L	L	X	L	Data In	Data In	Active	Don't Care

Ordering Information

Speed	Part Number	Package Name	Package Type
17*	AP9A106-17JC	P52.1	52-Pin PLCC
20	AP9A106-20JC	P52.1	52-Pin PLCC
25	AP9A106-25JC	P52.1	52-Pin PLCC
35	AP9A106-35JC	P52.1	52-Pin PLCC

*Preliminary

Document # DS-00002-Rev**