Features

- **Fully Compatible with the ITU Industry Standards H.263, G.723**
- **The AT76C3XX is Highly Optimized for the Following Platforms:**
  - **Videophones**
  - **Set-top Boxes**
  - **Personal Computer & Workstation**
- **The Single Chip Video Conferencing Accelerator Integrates:**
  - **Video Compression & Decompression**
  - **Audio Compression & Decompression**
  - **Acoustic Echo Cancellation**
- **Generates up to 30 Frames Per Second @ QCIF Resolution**
- **Accepts 16-bit Digital YUV Data (CCIR656)**
  - **Direct Interface to NTSC/PAL Decoder**
- **Outputs 8-bit Digital YUV Data (CCIR656)**
  - **Displays Images at sQCIF, QCIF, CIF and Full Screen Resolutions**
  - **Support Picture in Picture Display (PIP)**
  - **Still Image Display Capability**
- **Provides Direct Interface to Modem, Microcontroller**
- **Full-color OSD Strip Buffer**
- **Operates at 3.3 Volts with Standard 3/5V I/O**
- **208-pin PQFP Package**

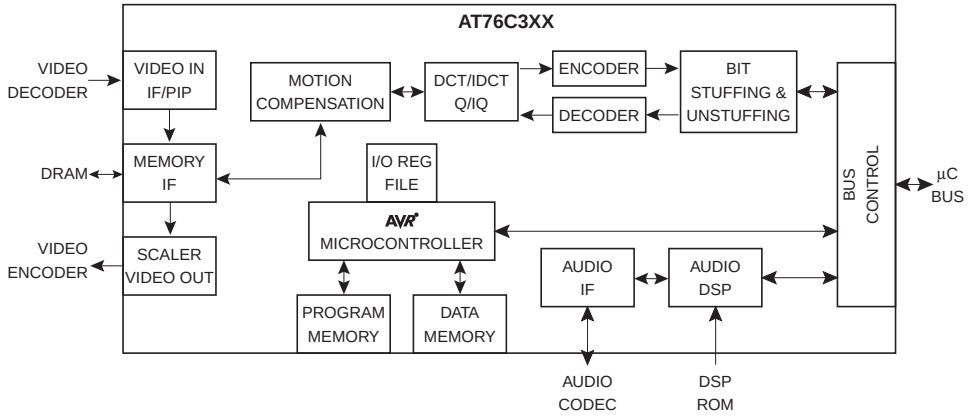
Description

The AT76C3XX is a single chip solution which is fully compatible with the ITU's industry standards H.263 and G.723. These standards enable video conferencing over the widely utilized twisted pair telephone lines. The AT76C3XX can be used to implement video conferencing in various platforms such as: stand-alone units, set-top boxes, and personal computers.

The AT76C3XX is a highly economical solution for the videoconferencing market that also offers high performance while maintaining superior display quality.

To address market demands for economical solutions, the AT76C3XX integrates the compression and decompression for the video and audio data, therefore requiring minimal external components. To maintain low system cost, the AT76C3XX uses a single 256K x 16 DRAM for its frame buffer. It interfaces directly to the digital camera or NTSC/PAL decoder, NTSC/PAL encoder, audio codec, modem, and microcontroller.

To meet the high performance and display quality required, the AT76C3XX generates and displays up to 30 frames per second. The chip integrates video post processing with up to 4x zoom capability. The AT76C3XX is capable of displaying sQCIF, QCIF, CIF and full screen resolution. It provides support for picture in picture (PIP), and still image display modes.



A High-Performance Video Conferencing Accelerator

AT76C3XX Summary

A complete datasheet is available under NDA. Please contact:

Richard Bisset
Product Marketing Director
Tel: (919) 462-6542
Fax: (919) 462-0300
e-mail: rbisset@atmel.com

Rev. 1135AS–09/98

The AT76C3XX is a high-performance video/audio codec chip, suitable for video-conferencing applications over a variety of data communications channels ranging from Public Switched Telephone Networks (PSTN) (33.6K bits/sec) to local area networks (1.5M bits/sec). The AT76C3XX is a full-duplex single-chip solution capable of simultaneously compressing outgoing and decompressing incoming video and audio signals according to the H.263 and G.723 ITU standards. It can be used to implement H.324 terminals using an external microcontroller capable of implementing the H.245 (call control) and H.223 (multiplexing protocol). The AT76C3XX uses a 4 Mbit DRAM or VRAM as working memory.

The AT76C3XX accepts 4:2:2 CCIR 656 video data, scaled down to QCIF resolution (176 x 144), and compresses it at a maximum frame rate of 30 frames/sec. It also captures audio data and compresses it at either 5.3K or 6.2K bps according to the G.723 standard. The AT76C3XX then stores compressed video and audio data in an external SRAM. An external microcontroller multiplexes audio and video data according to the H.223 standard, and handles all communications with a modem. Incoming data (control, compressed video, and compressed audio) is demultiplexed by the microcontroller, and audio/video data is written to the input segment of the SRAM. The AT76C3XX reads audio and video data from the SRAM, decompresses it, and supplies the uncompressed data to the video encoder and the audio codec.

Hardware Resources

- Video input interface capable of capturing either QCIF or CIF images from an external video decoder, or an external digital camera
- Motion compensation accelerator capable of performing full-search with programmable search ranges in both vertical and horizontal dimensions
- Data transform and quantization block responsible for performing the Discrete Cosine Transform (DCT), the quantization (Q), as well as their inverse operations (IDCT/IQ)
- Hardware encoder/decoder, bit-stuffer/bit-unstuffer
- A high-performance 8-bit Advanced Virtual RISC (AVR) microcontroller for implementing the high-level control functions
- NTSC/PAL video output interface
- Interface to 4-Mbit DRAM or VRAM memory
- High-performance, multi-tap scaler for sizing the output video up to 4x resolution
- Microprocessor/microcontroller access bus
- 16-bit general purpose DSP for audio compression/decompression and echo cancellation
- Audio controller interface that performs the μ/a-law to linear PCM conversion and vice-versa

Features

- QCIF and CIF video input resolutions
- Output video size: User-defined starting from sQCIF to full-screen resolution
- Standby mode for low power consumption (leakage current only)
- 208-pin PQFP package
- Internal Oscillators/PLLs for all input clocks (no need for external oscillators)
- 27 MHz master clock, 28.64 MHz video decoder input clock, 6.144 MHz audio input clock, and 34 MHz DSP clock
- Independent PIP positioning anywhere in the screen at either sQCIF or QCIF resolutions
- NTSC and PAL output video, scaled up to 4x
- On-Screen-Display
- Still-image compression and transmission
- Audio mute capabilities
- JTAG boundary scan IEEE 1149.1 standard

Advanced Capabilities

- Full-search motion compensation for both full and 1/2 pel resolutions
- Automated optimization of frame-rate/frame-quality ratio based on amount of motion and the available bit-rate
- Dynamic buffer control to allow transmission of compressed data at different bit-rates ranging from 14.4K bps (noisy PSTN lines) to 1.5M bps (T1 lines)