microelectronics group

Lucent Technologies
Bell Labs Innovations

LUCL8560 Low-Power SLIC with Ringing for ISDN TA, Pair Gain and Cable Telephony

Features

- Ideal for ISDN terminal adaptors, pair gain, and cable telephony applications
- Low active power (typical 167 mW during on-hook transmission)
- Sleep state for low idle power (88 mW)
- Quiet TIP/RING polarity reversal
- Auxiliary input for second battery, and internal switch to enable its use to save power in short telephone loops
- Per line ringing available for short loops
- Supports meter pulse injection
- Spare op amp (44-pin PLCC package only)
- –24 V to –65 V power supply operation
- Distortion-free full duplex from 0 mA dc loop current on-hook transmission
- Convenient operating states:
  — Forward powerup
  — Polarity reversal powerup
  — Forward sleep
  — Ground start
  — Disconnect
- Adjustable supervision functions:
  — Off-hook detector with longitudinal rejection
  — Ground key detector with longitudinal rejection
  — Ring trip detector
- Independent, adjustable, dc and ac parameters:
  — dc feed resistance (44-pin PLCC version)
  — Loop current limit
  — Termination impedance
- Thermal protection
- 32-pin PLCC or 44-pin PLCC packaging

Description

The LUCL8560 full-feature, low-power subscriber loop interface circuit (SLIC) is optimized for low-power consumption while providing an extensive set of features. This part is ideal for ISDN terminal adaptors applications and short loop power sensitive applications such as pair gain and cable telephony. This part is also designed for PBX, DLC, or CO applications.

The SLIC includes an auxiliary battery input and a battery switch. In short loop applications, they can be used in high battery to present a high on-hook voltage, then switched to low battery to reduce off-hook power.

To help minimize the required auxiliary battery voltage, the dc feed resistance and overhead voltage are set at 55 ohms and 6.7 V, respectively. This allows an undistorted on-hook transmission of a 3.14 dBm signal into a 900 Ω loop impedance.

The device offers the reverse battery function. Using the reverse battery, the device can provide a balanced power ring signal to Tip and Ring. In this mode of operation, the battery switch is used to apply a high-voltage battery during ringing and a lower voltage battery during the talk and idle states. Also included in the LUCL8560 is a dc current limit switch, which increases the dc current limit during power ringing. In addition, dc overhead voltage is reduced during the ring state. With the battery and current limit switches, and overhead reduction, the LUCL8560 can provide sufficient power to ring a true North America 5 REN load of 1380 Ω + 40 µF.

The device offers ring trip and loop closure supervision. It also includes the ground start state and ring ground detection. A summing node for meter pulse injection to 2.2 Vrms is also included. The 44-pin PLCC version also has a spare uncommitted op-amp, which may be used for ac gain setting or meter pulse filtering.

The LUCL8560 requires +5 V and battery to operate. The LUCL8560 does not require an additional –5 V supply. It is built in a 90 V complementary bipolar process. The device is available in a 32-pin PLCC or a 44-pin PLCC package.

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Description (continued)

Figure 1. Functional Diagram

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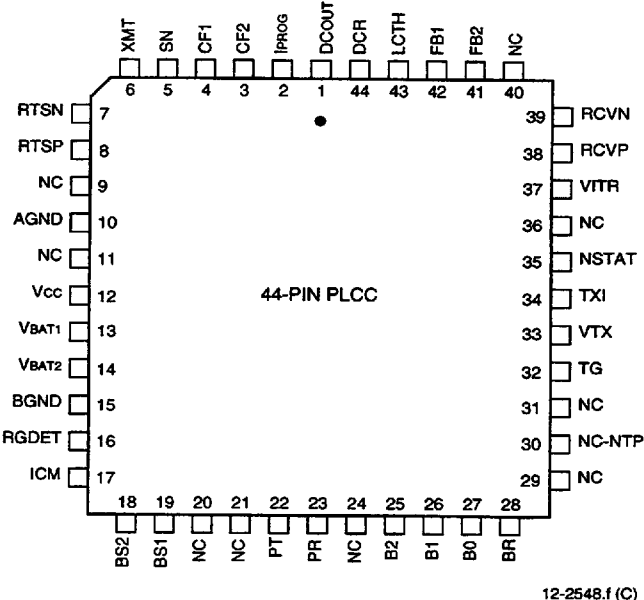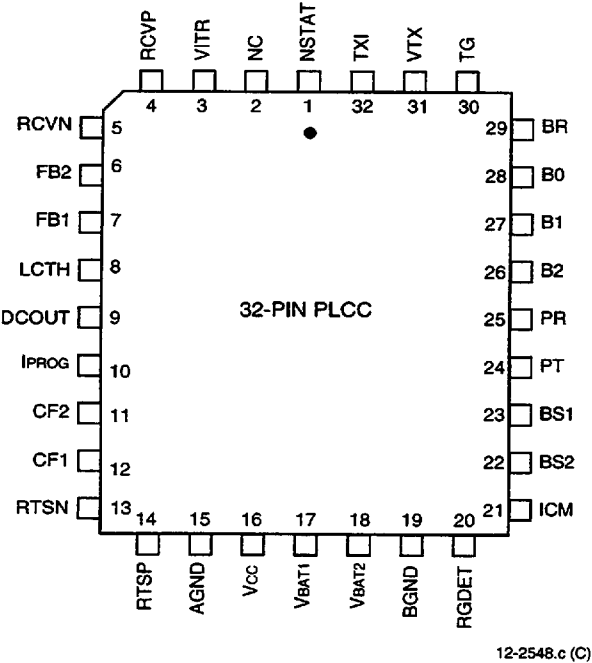
Pin Information

Figure 2. 32-Pin Diagram (PLCC Chip)

Figure 3. 44-Pin Diagram (PLCC Chip)

Table 1. Pin Descriptions

32-Pin	44-Pin	Symbol	Type	Description
9	1	DCOUT	O	This output is a voltage that is directly proportional to the absolute value of the differential TIP/RING current.
10	2	IPROG	I	**Current-Limit Program Input.** A resistor to DCOUT sets the dc current limit of the device.
11	3	CF2	—	**Filter Capacitor 2.** Connect a 0.1 µF capacitor from this pin to AGND.
12	4	CF1	—	**Filter Capacitor 1.** Connect a 0.47 µF capacitor from this pin to pin CF2.
—	5	SN	I	**Summing Node.** The inverting input of the uncommitted operational amplifier. A resistor or network to XMT sets the gain (44-pin PLCC only).
—	6	XMT	O	**Transmit ac Output Voltage.** The output of the uncommitted operational amplifier (44-pin PLCC only).
13	7	RTSN	I	**Ring Trip Sense Negative.** Connect this pin to the ringing generator signal through a high-value resistor.
14	8	RTSP	I	**Ring Trip Sense Positive.** Connect this pin to the ring relay and the ringer series resistor through a high-value resistor.
—	9	NC	—	**No Connection.** May be used as a tie point.
15	10	AGND	—	**Analog Signal Ground.**
—	11	NC	—	**No Connection.** May be used as a tie point.
16	12	Vcc	—	**5 V Power Supply.**
17	13	VBAT1	—	**Battery Supply.** Negative high-voltage battery, higher in magnitude than VBAT2.

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Pin Information (continued)

Table 1. Pin Descriptions (continued)

32-Pin	44-Pin	Symbol	Type	Description
18	14	VBAT2	—	**Auxiliary Battery Supply.** Negative high-voltage battery, lower in magnitude than VBAT1, used to reduce power dissipation on short loops.
19	15	BGND	—	**Battery Ground.** Ground return for the battery supply.
20	16	RGDET	O	**Ring Ground Detect.** When high, this open-collector output indicates the presence of a ring ground. To use, connect a 100 kΩ resistor to VCC.
21	17	ICM	I	**Common-Mode Current Sense.** To program ring ground sense threshold, connect a resistor to VCC and connect a capacitor to AGND to filter 50/60 Hz. If unused, the pin should be connected to ground.
22	18	BS2	—	**Battery Switch Slowdown.** Connect a 0.1 µF capacitor to pin BS1.
23	19	BS1	—	**Battery Switch Slowdown.** Connect a 0.1 µF capacitor to pin BS2.
—	20	NC	—	**No Connection.** May be used as a tie point.
—	21	NC	—	**No Connection.** May be used as a tie point.
24	22	PT	I/O	**Protected Tip.** The output of the tip driver amplifier and input to loop sensing. Connect to loop through overvoltage protection.
25	23	PR	I/O	**Protected Ring.** The output of the ring driver amplifier and input to loop sensing circuitry. Connect to loop through overvoltage protection.
—	24	NC	—	**No Connection.** May be used as a tie point.
26	25	B2	I	**State Control Input.** B0, B1, B2, and BR determine the state of the SLIC. See Table 2.
27	26	B1	I	**State Control Input.** B0, B1, B2, and BR determine the state of the SLIC. See Table 2.
28	27	B0	I	**State Control Input.** B0, B1, B2, and BR determine the state of the SLIC. See Table 2.
29	28	BR	I	**State Control Input.** B0, B1, B2, and BR determine the state of the SLIC. See Table 2.
—	29	NC	—	**No Connection.** May be used as a tie point.
—	30	NC-NTP	—	**No Connection.** May NOT be used as a tie point.
—	31	NC	—	**No Connection.** May be used as a tie point.
30	32	TG	—	**Transmit Gain.** Connect a 4320 Ω resistor from this pin to VTX.
31	33	VTX	O	The voltage at this pin is directly proportional to the differential TIP/RING current.
32	34	TXI	—	**ac/dc Separation.** Connect a 0.1 µF capacitor from this pin to VTX.
1	35	NSTAT	O	**Loop Detector Output/Ring Trip Detector Output.** This output is a "wired or" of the NLC/NRDET outputs. When low, this logic output indicates that an off-hook condition exists or that ringing has been tripped.
3	37	VITR	O	This output is a voltage that is directly proportional to the differential ac TIP/RING current.
4	38	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls the ac differential voltage on TIP and RING.
5	39	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls the ac differential voltage on TIP and RING.
—	40	NC	—	**No Connection.** May be used as a tie point.

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Pin Information (continued)

Table 1. Pin Descriptions (continued)

32-Pin	44-Pin	Symbol	Type	Description
6	41	FB2	—	**Polarity Reversal Slowdown.** Connect a capacitor to ground.
7	42	FB1	—	**Polarity Reversal Slowdown.** Connect a capacitor to ground.
8	43	LCTH	I	**Loop Closure Threshold Input.** Connect a resistor to DCOUT to set off-hook threshold.
—	44	DCR	I	**dc Resistance.** Short to analog ground for dc feed resistance of 55 Ω. The dc feed resistance can be increased to a nominal 760 Ω by shorting DCR to DCOUT. Intermediate values can be set by a simple resistor divider from DCOUT to ground with the tap at DCR (44-pin PLCC only).

Functional Description

Table 2. Input State Coding

B0	B1	B2	BR	State/Definition
1	1	0	1	**Powerup, Forward Battery.** Pin PT is positive with respect to PR. VBAT2 is applied to the TIP/RING drive amplifiers. On-hook transmission capability. All supervision active—an off-hook condition or a ring trip causes output NSTAT to go low. Current limit set per Rprop = 0.555 ILIM.
1	0	0	1	**Powerup, Reverse Battery.** Pin PR is positive with respect to pin PT. VBAT2 is applied to the TIP/RING drive amplifiers. On-hook transmission capability. All supervision active—an off-hook condition or a ring trip causes output NSTAT to go low. Current limit set per Rprop = 0.555 ILIM.
1	1	1	1	**Powerup, Forward Battery.** Pin PT is positive with respect to PR. VBAT1 is applied to the TIP/RING drive amplifiers. On-hook transmission capability. All supervision active—an off-hook condition or a ring trip causes output NSTAT to go low. Current limit set per Rprop = 0.555 ILIM.
1	0	1	1	**Powerup, Reverse Battery.** Pin PR is positive with respect to pin PT. VBAT1 is applied to the TIP/RING drive amplifiers. On-hook transmission capability. All supervision active—an off-hook condition or a ring trip causes output NSTAT to go low. Current limit set per Rprop = 0.555 ILIM.
0	1	1	1	**Ground Start.** Tip drive amplifier is turned off. The device presents a high impedance (>100 K) to pin PT and a current limited battery (VBAT1) to pin PR. Output pin RGDET indicates current flowing in the ring lead.
0	0	1	1	**Low Power Scan.** Except for off-hook supervision, all circuits are shutdown to conserve power. Only the off-hook detector affects output pin NSTAT. VBAT1 is applied to the TIP/RING drive amplifiers. Pin PT is positive with respect to pin PR. On-hook transmission is disabled.
0	0	0	1	**Forward Disconnect.** The TIP and RING amplifiers are turned off and the SLIC goes into a high impedance state (>100 K). VBAT2 is applied to the SLIC.
1	1/0	1	0	**Ring State.** SLIC is powered up. VBAT1 is applied to the TIP and RING amplifiers. Current limit is increased (and set per RPROG = 0.198 ILIM). Overhead voltage is reduced to approximately 1.5 V. These conditions are necessary to supply sufficient power to drive a true North American 5 REN ringing load (1860 Ω + 40 μF). Loop closure detector is disabled—only the Ring Trip detector affects output pin NSTAT. To apply a balanced ring signal to pins PR and PT apply a 0 V to 5 V square wave to input pin B1. Ringing frequency is the frequency of the input wave at B1. To shape the ring signal at pins PR and PT, connect a capacitor from Pin FB1 to ground and from pin FB2 to ground.

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Functional Description (continued)

Table 3. Supervision Coding

Pin NSTAT	Pin RGDET
0 = off-hook or ring trip	1 = ring ground
1 = on-hook and no ring trip	0 = no ring ground

Absolute Maximum Ratings (T$_A$ = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Value	Unit
5 V Power Supplies	V$_{CC}$	7.0	V
Battery (Talking) Supplies	V$_{BAT1}$, V$_{BAT2}$	−70	V
V$_{BAT2}$ Magnitude	lV$_{BAT2}$l	lV$_{BAT1}$l + 0.4	V
Logic Input Voltage	—	−0.5 to +7.0	V
Analog Input Voltage	—	−7.0 to +7.0	V
Maximum Junction Temperature	T$_J$	165	°C
Storage Temperature Range	T$_{stg}$	−40 to +125	°C
Relative Humidity Range	R$_H$	5 to 95	%
Ground Potential Difference (BGND to AGND)	—	±3	V
PT or PR Fault Voltage (dc)	V$_{PT}$, V$_{PR}$	(V$_{BAT1}$ − 5) to +3	V
PT or PR Fault Voltage (10 x 1000 μs)	V$_{PT}$, V$_{PR}$	(V$_{BAT1}$ − 15) to +15	V
Current into Ring Trip Inputs	I$_{RTSP}$, I$_{RTSN}$	±240	μA

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. Some of the known examples of conditions that cause such potentials during powerup are 1) an inductor connected to TIP and RING can force an overvoltage on VBAT through the protection devices if the VBAT connection chatters, and 2) inductance in the VBAT lead could resonate with the VBAT filter capacitor to cause a destructive overvoltage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature	−40	—	85	°C
Loop Closure Threshold-Detection Programming Range	5	10	I$_{LIM}$	mA
dc Loop Current-limit Programming Range	5	40	50	mA
On- and Off-hook 2-wire Signal Level (@ Z$_{LOOP}$ = 200 Ω)	—	—	2.2	V$_{RMS}$
ac Termination Impedance Programming Range	150	600	1300	Ω
V$_{BAT1}$	−24	−48	−65	V
V$_{BAT2}$	−16	−28	V$_{BAT1}$	V
V$_{CC}$	4.5	5.0	5.5	V
dc Feed Resistance Programming Range (excl. RP)	55	55	760	Ω

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Electrical Characteristics

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are
the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing
requirements. Minimum and maximum values apply across the entire temperature range (–40 °C to +85 °C)
and entire battery range unless otherwise specified. Typical is defined as 25 °C, V_{CC} = 5.0 V, V_{BAT1} = –48 V,
V_{BAT2} = –25.5 V. Positive currents flow into the device. Test circuit is Figure 5 unless noted.

Table 4. Power Supply

Parameter	Min	Typ	Max	Unit
Power Supply Rejection 500 Hz to 3 kHz (See Figures 5, 6, 15, and 16.)[1]				
V_{CC} (1 kHz)	35	—	—	dB
V_{BAT1}, V_{BAT2} (500 Hz—3 kHz)	45	—	—	dB
Thermal Protection Shutdown (T_{jc})	—	165	—	°C
Thermal Resistance, Junction to Ambient (θ_{JA}) Still Air 44-pin PLCC	—	47	—	°C/W
Thermal Resistance, Junction to Ambient (θ_{JA}) Still Air 32-pin PLCC	—	60	—	°C/W
Power Supply—Powerup, No Loop Current, dc Supplies at Typical Values				
I_{CC}	—	6.3	7.2	mA
I_{BAT1} (B2 = 1)	—	2.8	3.3	mA
I_{BAT2} (B2 = 0)	—	2.6	3.2	mA
Power Supply—Low-power Scan, Forward Bat, No Loop Current				
I_{CC}	—	4.5	5.2	mA
I_{BAT} (V_{BAT} = –48 V)	—	1.3	1.6	mA
Power Dissipation (V_{BAT} = –48 V)	—	88	103	mW

1. This parameter is not tested in production. It is guaranteed by design and device characterization.

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Electrical Characteristics (continued)

Table 5. 2-Wire Port

Parameter	Min	Typ	Max	Unit
TIP or RING Drive Current = dc + Longitudinal + Signal Currents	65	—	—	mA
Signal Current	15	—	—	mArms
Longitudinal Current Capability per Wire[1]	8.5	15	—	mArms
dc Loop Current Limit[2] R_{LOOP} = 100 Ω Programmability Range Accuracy (20 mA < I_{LIM} < 40 mA) BR = +5 V	— 5 —	I_{LIM} — —	— 50 ±12	mA mA %
Powerup Open Loop Voltage Levels Differential Voltage – V_{BAT2} Differential Voltage – V_{BAT1}, (V_{BAT1} = –48 V)	$\|V_{BAT2} + 7.2\|$ $\|V_{BAT1} + 7.6\|$	$\|V_{BAT2} + 6.7\|$ $\|V_{BAT1} + 7.1\|$	$\|V_{BAT2} + 6.0\|$ $\|V_{BAT1} + 6.1\|$	V V
Ground Start State PT Resistance	100	—	—	$k\Omega$
dc Feed Resistance (for I_{LOOP} below current limit)	—	55	80	Ω
Loop Resistance Range (3.17 dBm overload into 600 Ω; not including protection) I_{LOOP} = 20 mA at V_{BAT1} = –48 V I_{LOOP} = 20 mA at V_{BAT2} = –24 V	 1940 760	 — —	 — —	 Ω Ω
Longitudinal Balance, R_P Mismatched by 1.4 Ω, $R_P \geq 30$ Ω	49	—	—	dB
Longitudinal to Metallic Balance—*IEEE*[3] Std 455 (See Figure 7.)[4] 50 Hz to 1 kHz 1 kHz to 3.4 kHz	 64 58	 75 70	 — —	 dB dB
Metallic to Longitudinal Balance 200 Hz to 4kHz	46	—	—	dB
RFI Rejection (See Figure 9.)[5] 0.5 Vrms, 50 Ω Source, 30% AM Mod 1 kHz 500 kHz to 100 MHz	 —	 –55	 –45	 dBV

1. The longitudinal current is independent of dc loop current.
2. Current-limit I_{LIM} is programmed by a resistor, R_{PROG}, from pin IPROG to AGND. I_{LIM} is specified at the loop resistance where current limiting begins (see Figure 22). Select R_{PROG} (kΩ) = 0.555 x I_{LIM} (mA) with input BR high. When input BR is low, use R_{PROG} (kΩ) = 0.198 x I_{LIM} (mA).
3. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
4. Longitudinal balance of circuit card will depend on loop series resistance matching.
5. This parameter is not tested in production. It is guaranteed by design and device characterization.

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Electrical Characteristics (continued)

Table 6. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
Differential PT/PR Current Sense (DCOUT)				
Gain (PT/PR to DCOUT)	—	−41.7	—	V/A
Offset Voltage @ I_{LOOP} = 0	−200	—	200	mV
Loop Closure Detector Threshold[1]				
Programming Accuracy at 10 mA	—	—	±20	%
Ring Ground Detector Threshold[2]				
R_{ICM} = 83 kΩ	3	6	10	kΩ
Programming Accuracy	—	—	±25	%
Ring Trip Comparator				
Input Offset Voltage	—	—	±10	mV
RCVN, RCVP				
Input Bias Current	—	−0.2	−1	μA
Loop Closure Detector Hysteresis	1.7	2	2.3	mA
THD[3] at $V_{PT/PR}$ = 2.2 Vrms, V_{OH} = 12 V, Z_T = 200 Ω (Not tested in production)	—	–	-35	dB
VITR Output Impedance	—	5	—	Ω
VITR Output Offset Voltage	—	20	—	mV

1. Loop closure threshold is programmed by resistor RLCTH from pin LCTH to pin DCOUT.
2. Ring ground threshold is programmed by resistor RICM2 from pin ICM to VCC.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.

Table 7. Uncommitted Op Amp Characteristics (44-Pin PLCC only)

Parameter	Min	Typ	Max	Unit
Input Offset Voltage	—	±5	—	mV
Input Offset Current	—	±10	—	nA
Input Bias Current	—	200	—	nA
Differential Input Resistance	—	1.5	—	MΩ
Output Voltage Swing (R_L = 10 kΩ)	—	±3.5	—	Vpk
Output Resistance (A_{VCL} = 1)	—	2.0	—	Ω
Small Signal GBW	—	700	—	kHz

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Electrical Characteristics (continued)

Table 8. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]	150	—	1300	Ω
Longitudinal Impedance	—	0	—	Ω

Total Harmonic Distortion—200 Hz to 4 kHz[2]
  Off-hook
  On-hook
	
	—
	—
		
		—
		—
			
			0.3
			1.0
				
				%
				%

Transmit Gain, f = 1 kHz (PT/PR to VITR; see Figure 11.) Transmit Accuracy in dB (powerup, 600 Ω termination)	−392 −0.18	−400 0	−408 0.18	V/A dB
Receive + Gain, f = 1 kHz, (RCVP to PT/PR Receive − Gain, f = 1 kHz, (RCVN to PT/PR) Receive Accuracy in dB Receive Gain Accuracy RCVC	7.76 −7.76 −0.25 −0.38	8.00 −8.00 0 0	8.24 −8.24 0.25 0.38	− − dB dB

Gain Accuracy (25 °C, 600 Ω termination, V$_{BAT}$ = −48 V)
  Transmit (close loop, powerup)
  Receive
	
	−0.15
	−0.2
		
		0
		0
			
			0.15
			0.2
				
				dB
				dB

Group Delay
  Transmit, Powerup
  Receive
	—
	
		1
		0.5
			—
			
				μs
				μs

Gain vs. Frequency (transmit and receive)
  (600 Ω termination; reference 1 kHz, 1 Vrms)[2]
  200 Hz to 300 Hz
  300 Hz to 3.4 kHz
  3.4 kHz to 16 kHz
  16 kHz to 266 kHz
	
	−1.00
	−0.3
	−3.0
	—
		
		0.0
		0.0
		−0.1
		—
			
			0.05
			0.05
			0.3
			2.5
				
				dB
				dB
				dB
				dB

Gain vs. Level (transmit and receive)(reference 0 dBV)[2] −50 dB to +3 dB	 −0.05	 0	 0.05	 dB
Return Loss[3]; 200 Hz to 500 Hz 500 Hz to 3400 Hz	20 26	24 29	— —	dB dB

2-wire Idle-channel Noise (600 Ω termination)
  Psophometric
  C-message
  3 kHz Flat
	
	—
	—
	—
		
		−87
		2
		10
			
			−77
			12
			20
				
				dBmp
				dBrnC
				dBrn

4-wire Idle-channel Noise; Psophometric
  C-message
  3 kHz flat
	
	—
	—
		−82
		7
		15
			−77
			12
			20
				dBmp
				dBrnC
				dBrn

Transhybrid Loss[3]
  200 Hz to 500 Hz
  500 Hz to 3400 Hz
	
	21
	26
		
		24
		29
			
			—
			—
				
				dB
				dB

1. Set by external components. Any complex impedance R1 + R2 II C between 150 Ω and 1300 Ω can be synthesized.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Return loss and transhybrid loss are functions of device gain accuracies and the external hybrid circuit. Guaranteed performance assumes 1% tolerance external components.

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Electrical Characteristics (continued)

Table 9. Logic Inputs and Outputs

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages					
Low Level (permissible range)	V_{IL}	−0.5	0.4	0.7	V
High Level (permissible range)	V_{IH}	2.0	2.4	Vcc	V
Input Currents					
Low Level (Vcc = 5.25 V, V_I = 0.4 V)	I_{IL}	−75	−115	−200	μA
High Level (Vcc = 5.25 V, V_I = 2.4 V)	I_{IH}	−40	−60	−100	μA
Output Voltages (open collector with internal pull-up resistor)					
Low Level (Vcc = 4.75 V, I_{OL} = 360 μA)	V_{OL}	0	0.2	0.4	V
High Level (Vcc = 4.75 V, I_{OH} = −20 μA)	V_{OH}	2.4	—	Vcc	V

Ring Trip Requirements

- Ringing signal:
  - Voltage, minimum 35 V_{RMS}, maximum 100 V_{RMS}.
  - Frequency, 17 Hz to 23 Hz.
  - Crest factor, 1.4 to 2.

- Ringing trip:
  - ≤100 ms (typical), ≤250 ms (V_{BAT} = −33 V, loop length = 530 Ω).

- Pretrip:
  - The circuits in Figure 4 will not cause ringing trip.
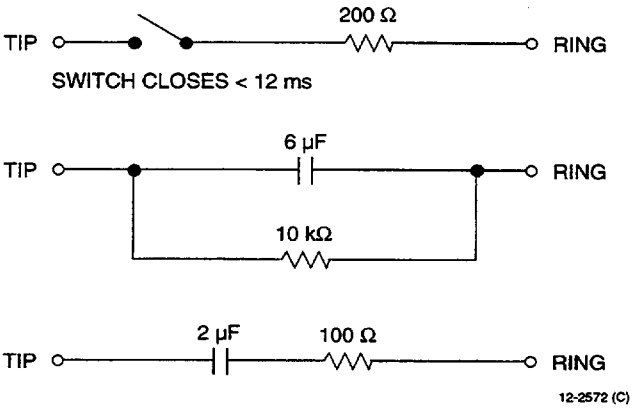
Figure 4. Ring Trip Circuits

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Test Configurations
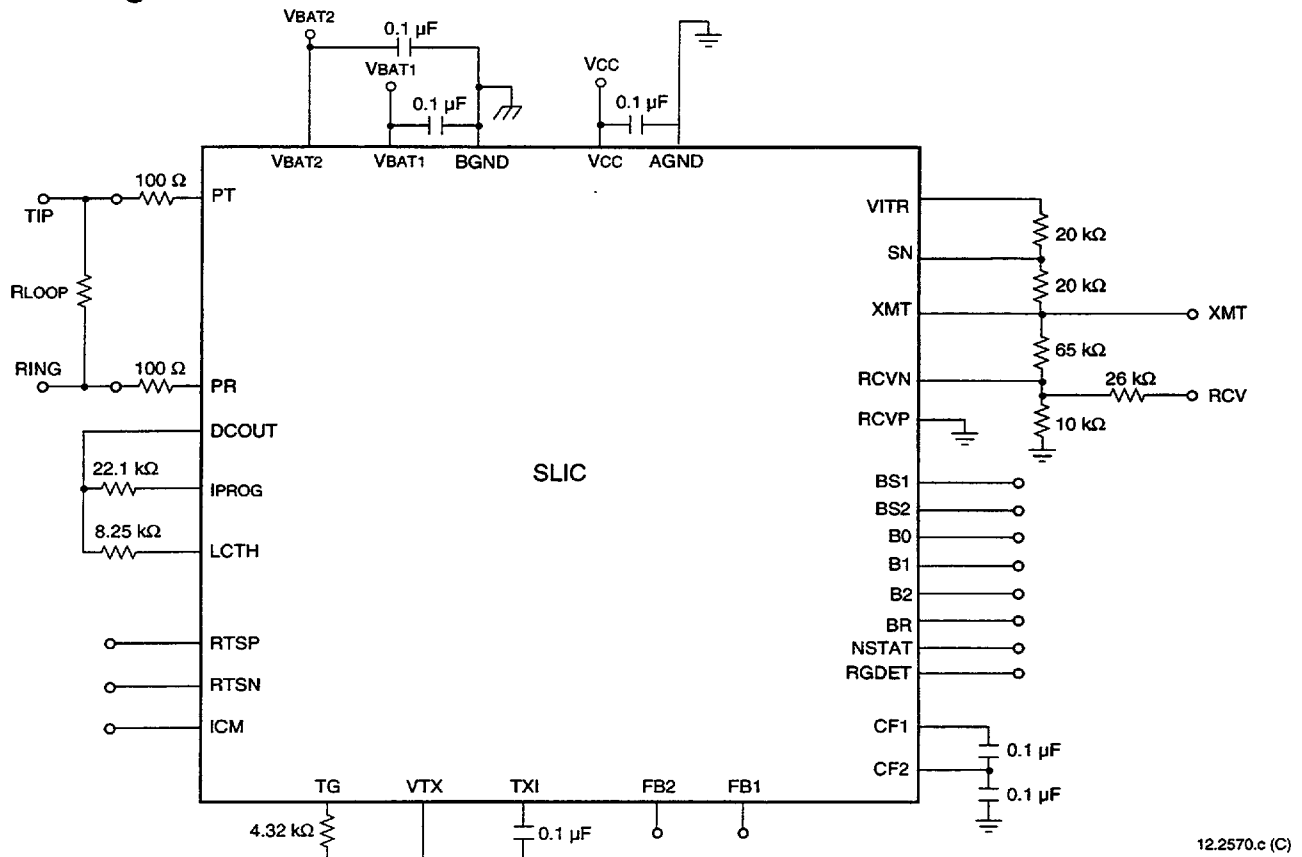
Figure 5. Basic Test Circuit (44-Pin PLCC)

$$PSRR = 20 \log \frac{V_{T/R}}{V_S}$$
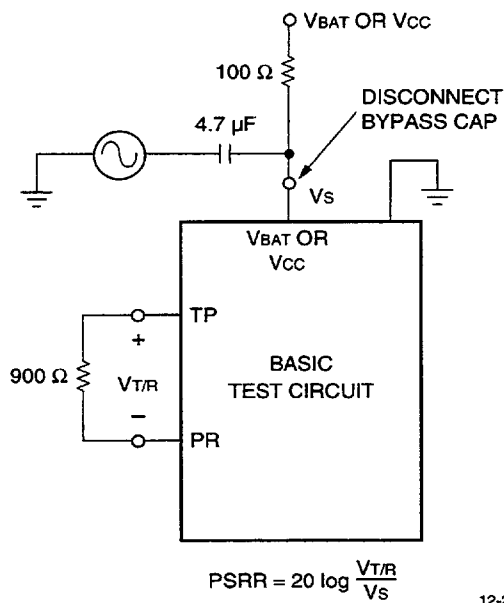
Figure 6. Metallic PSRR

$$PSRR = 20 \log \frac{V_M}{V_S}$$
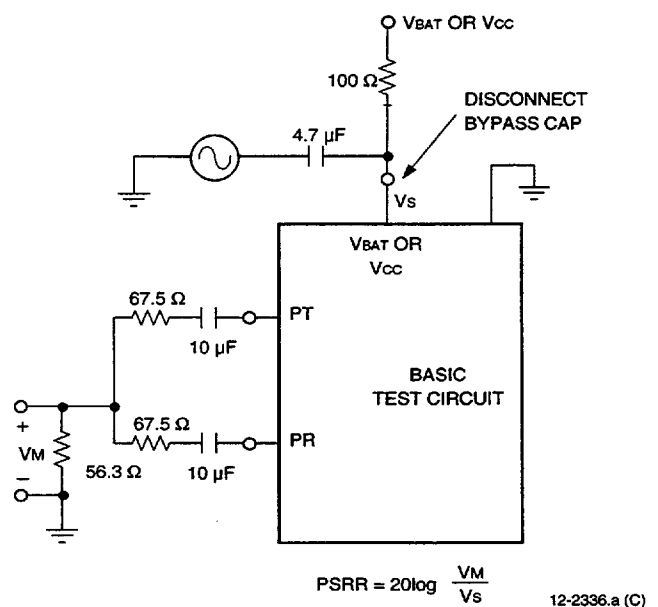
Figure 7. Longitudinal PSRR

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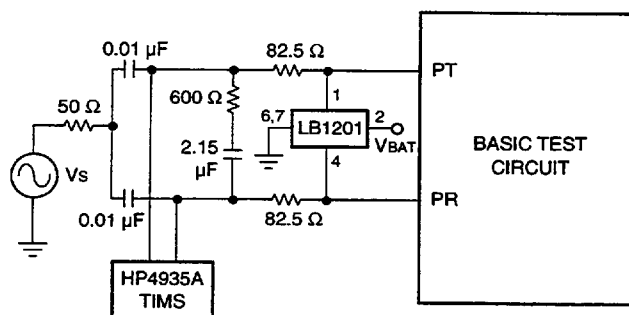## Test Configurations (continued)
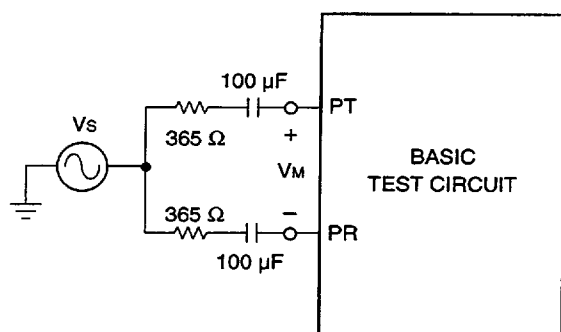
$$\text{LONGITUDINAL BALANCE} = 20 \log \frac{V_M}{V_S}$$

12-2584.a (C)

Figure 8. Longitudinal Balance

Vs = 0.5 Vrms 30% AM 1 kHz MODULATION,
f = 500 kHz – 1 MHz
DEVICE IN POWERUP MODE, 600 Ω TERMINATION

12-2586 (C)

Figure 9. RFI Rejection
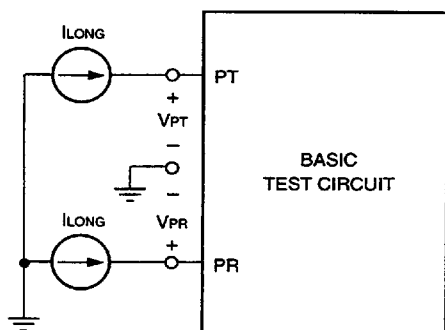
$$Z_{LONG} = \frac{\Delta V_{PT}}{\Delta I_{LONG}} \text{ OR } \frac{\Delta V_{PR}}{\Delta I_{LONG}}$$

12-2585 (C)

Figure 10. Longitudinal Impedance
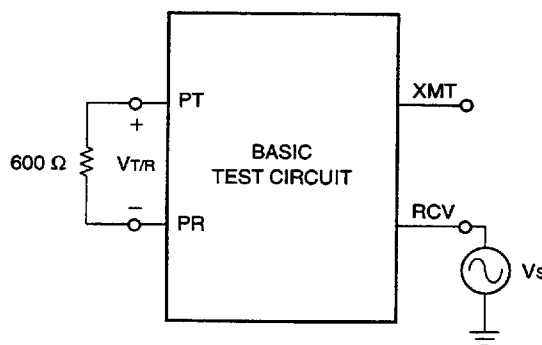
$$G_{XMT} = \frac{V_{XMT}}{V_{T/R}}$$

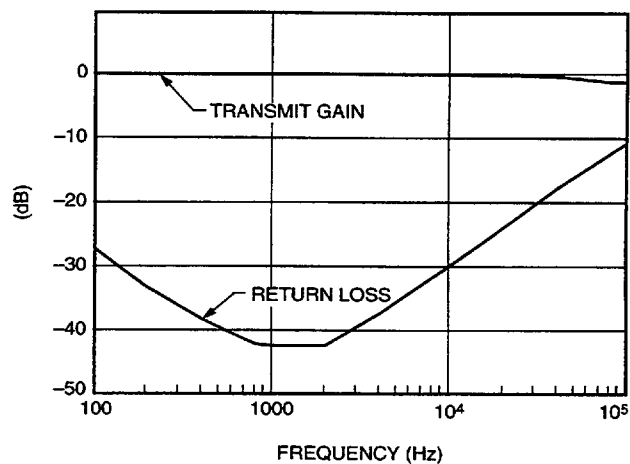$$G_{RCV} = \frac{V_{T/R}}{V_{RCV}}$$

12-2587 (C)

Figure 11. ac Gains
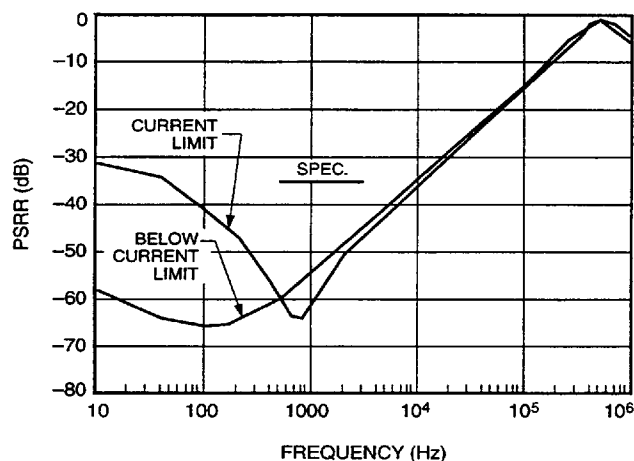
■ 0050026 0021174 519 ■

Applications

Characteristic Curves
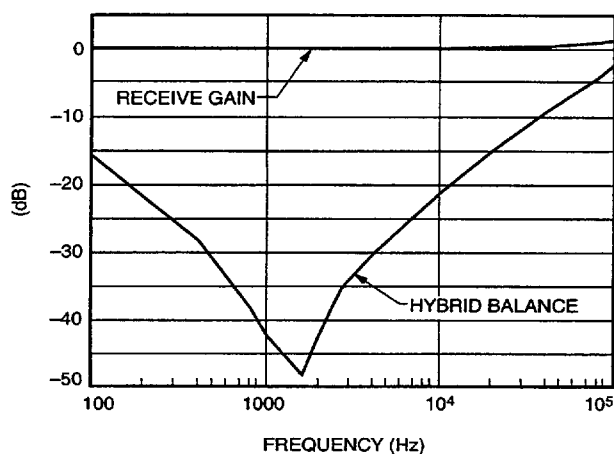
Figure 12. LUCL8560 Receive Gain and Hybrid Balance vs. Frequency

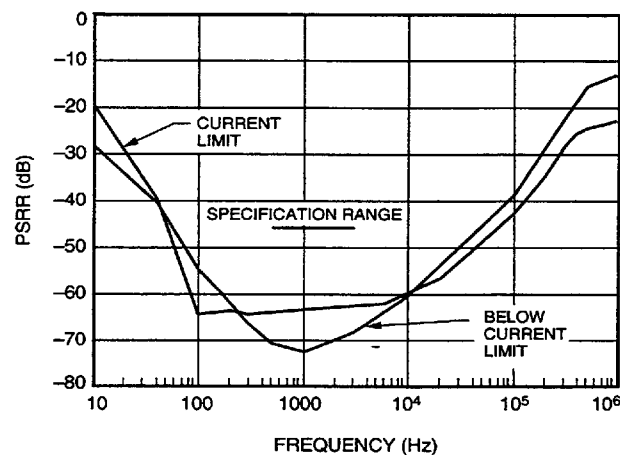**Figure 13. LUCL8560 Transmit Gain and Return Loss vs. Frequency**

Figure 14. LUCL8560 Typical Vcc Power Supply Rejection

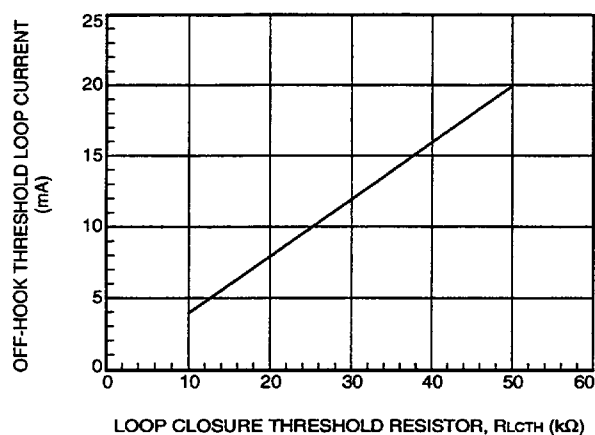**Figure 15. LUCL8560 Typical V$_{BAT}$ Power Supply Rejection**
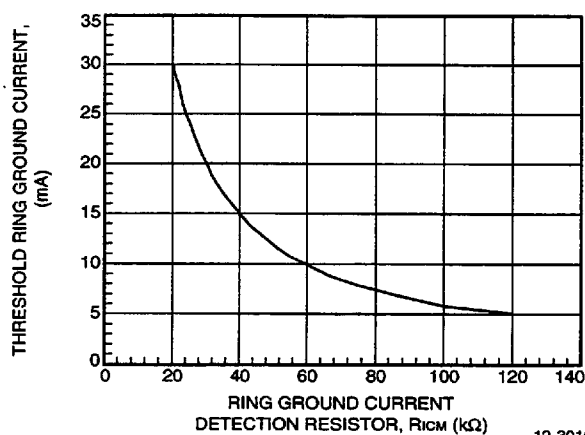
■ 0050026 0021175 455 ■

Applications (continued)

Characteristic Curves (continued)

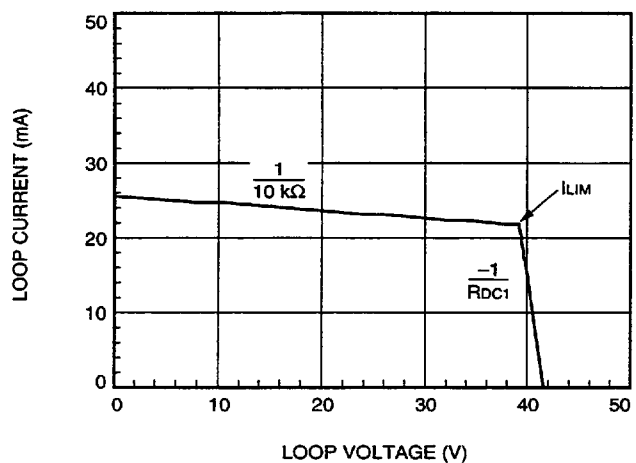Notes: $V_{BAT1} = -48$ V, $I_{TR} = 1.2 \times 10^{-3}\ R_{LCTH}$ (kΩ)

**Figure 16. Loop Closure Program Resistor
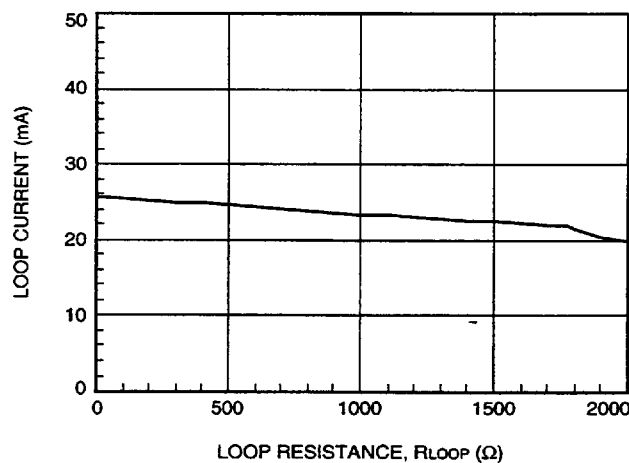Selection**

Notes: TIP lead is open; $V_{BAT1} = -48$ V.

Figure 17. Ring Ground Detection Programming

Notes: $V_{BAT1} = -48$ V; $I_{LIM} = 22$ mA; $R_{DC1} = 55$ Ω

Figure 18. Loop Current vs. Loop Voltage

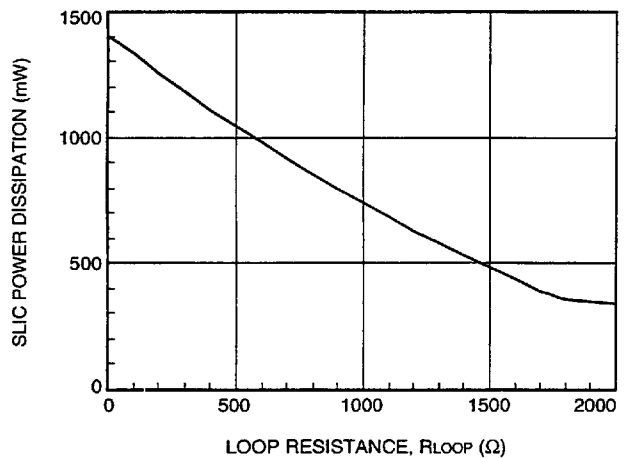
Notes: $V_{BAT1} = -48$ V; $I_{LIM} = 22$ mA; $R_{DC1} = 55$ Ω

Figure 19. Loop Current vs. Loop Resistance

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Applications (continued)

Characteristic Curves (continued)

Notes: $V_{BAT1} = -48$ V; $I_{LIM} = 22$ mA; $R_{DC1} = 55\ \Omega$

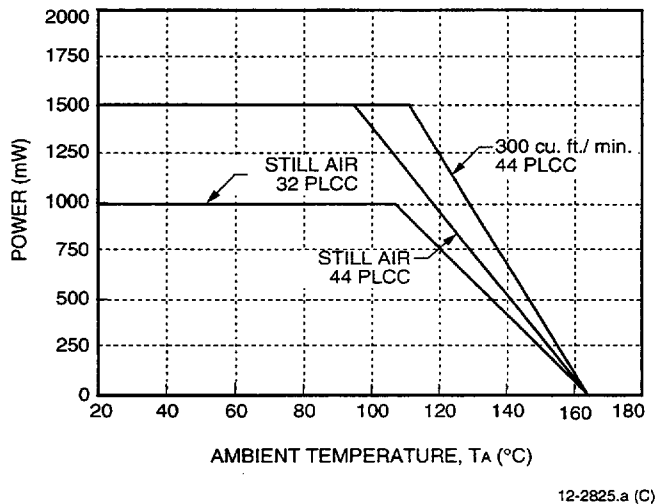**Figure 20. LUCL8560 Typical SLIC Power Dissipation vs. Loop Resistance**

Figure 21. Power Derating

dc Applications

Battery Feed

The dc feed characteristic can be described by:

$$V_{T/R} = \frac{(|V_{BAT}| - V_{OH}) \times R_L}{R_L + 2R_P + R_{dc}}$$

$$I_L = \frac{|V_{BAT}| - V_{OH}}{R_L + 2R_P + R_{dc}}$$

where:
I_L = dc loop current.
$V_{t/r}$ = dc loop voltage.
$|V_{BAT}|$ = battery voltage magnitude.

Note: The LUCL8560 has a battery switch circuit which allows use of a primary battery VBAT1 or an auxiliary battery VBAT2. IVBATI is the battery, VBAT1 or VBAT2, that is active. See the Battery Switch section for more information.

V_{OH} = overhead voltage. This is the difference between the battery voltage and the open loop TIP/RING voltage.
R_L = loop resistance, not including protection resistors.
R_P = protection resistor value.
R_{dc} = SLIC internal dc feed resistance.

The design begins by drawing the desired dc template. An example is shown in Figure 22.
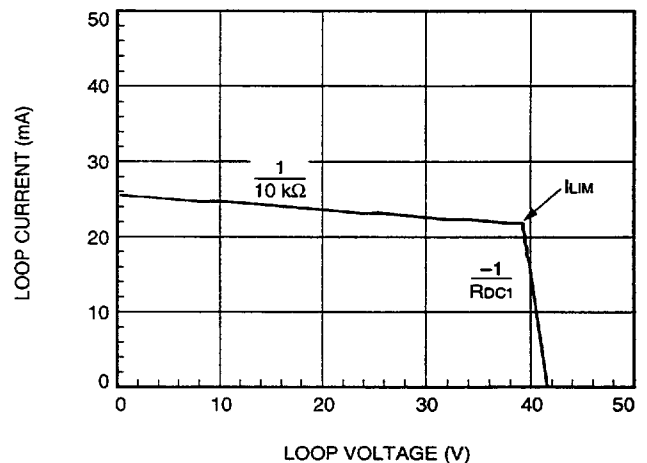
Notes: $V_{BAT1} = -48$ V; $I_{LIM} = 22$ mA; $R_{DC1} = 55\ \Omega$

Figure 22. Loop Current vs. Loop Voltage

■ 0050026 0021177 228 ■

Applications (continued)

dc Applications (continued)

Starting from the on-hook condition and going through to a short circuit, the curve passes through two regions:

Region 1: On-hook and low loop currents. In this region, the slope corresponds to the dc resistance of the SLIC, R_{DC1} (default is 55 Ω typical). The open circuit voltage is the battery voltage less the overhead voltage of the device, V_{OH} (default is 7.1 V typical). These values are suitable for most applications, but can be adjusted if needed. For more information, see the sections entitled Adjusting dc Feed Resistance or Adjusting Overhead Voltage.

Region 2: Current limit. The dc current is limited to a value determined by external resistor R_{PROG}. This region of the dc template has a high resistance (10 kΩ).

Calculate the external resistor as follows:

$$R_{PROG} \text{ (k}\Omega) = 0.555 \, I_{LIM} \text{ (mA)}^*$$

* During the balanced ringing mode, the current limit is increased from the value predicted by this equation by a factor of 2.8. See the Ringing Application section for more information.

Overhead Voltage

In order to drive an on-hook ac signal, the SLIC must set up the TIP and RING voltage to a value less than the battery voltage. The amount that the open loop voltage is decreased relative to the battery is referred to as the overhead voltage. Expressed as an equation,

$$V_{OH} = |V_{BAT}| - (V_{PT} - V_{PR})$$

Without this buffer voltage, amplifier saturation will occur and the signal will be clipped. The LUCL8560 is automatically set at the factory to allow undistorted on-hook transmission of a 3.17 dBm signal into a 900 Ω loop impedance.

The drive amplifiers are capable of 4 Vrms minimum (V_{AMP}). So, the maximum signal the device can guarantee is:

$$V_{T/R} = 4 \text{ V} \left(\frac{|Z_{T/R}|}{|Z_{T/R}| + 2R_P} \right)$$

For applications where higher signal levels are needed, e.g., periodic pulse metering, the 2-wire port of the SLIC can be programmed with pin DCR (pin DCR is not available in the 32-pin PLCC package). The first step is to determine the amount of overhead voltage needed. The peak voltage at output of TIP and

RING amplifiers is related to the peak signal voltage by:

$$\hat{V}_{amp} = \hat{V}_{t/r}\left(1 + \frac{2R_P}{|Z_{T/R}|} \right)$$

12-2563 (C)
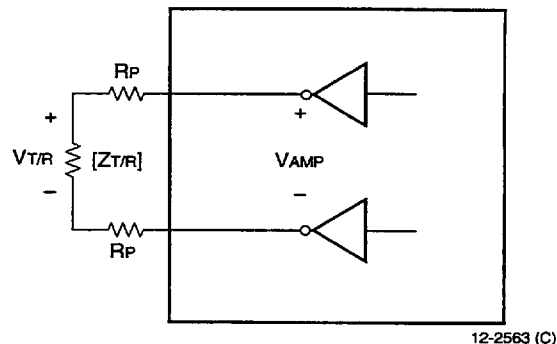
Figure 23. SLIC 2-Wire Output Stage

In addition to the required peak signal level, the SLIC needs about 2 V from each power supply to bias the amplifier circuitry. It can be thought of as an internal saturation voltage. Combining the saturation voltage and the peak signal level, the required overhead can be expressed as:

$$V_{OH} = V_{SAT} + \left(1 + \frac{2R_P}{|Z_{T/R}|} \right)\hat{V}_{t/r}$$

$$= V_{SAT} + \left(1 + \frac{2R_P}{|Z_{T/R}|} \right)\sqrt{\frac{2|Z_{T/R}|}{1000}} \times 10^{dBm/20}$$

where V_{SAT} is the combined internal saturation voltage between the TIP/RING amplifiers and V_{BAT} (4.0 V typ.). R_P (Ω) is the protection resistor value. $Z_{T/R}$ (Ω) is the ac loop impedance.

Example 1, On-Hook Transmission of a Meter Pulse:

Signal level: 2.2 Vrms into 200 Ω
35 Ω protection resistors
$I_{LOOP} = 0$ (on-hook transmission of the metering signal)

$$V_{OH} = 4.0 + \left(1 + \frac{2 \times 35}{200} \right)\sqrt{2}(2.2)$$

$$= 8.2 \text{V}$$

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Applications (continued)

dc Applications (continued)

Accounting for V_{SAT} tolerance of 0.5 V, a nominal overhead of 8.7 V would ensure transmission of an undistorted 2.2 V metering signal.

Adjusting Overhead Voltage

To adjust the open loop 2-wire voltage, pin DCR (44-pin PLCC only) is programmed at the midpoint of a resistive divider from ground to either –5 V or V_{BAT}. In the case of –5 V, the overhead voltage will be independent of the battery voltage. Figure 24 shows the equivalent input circuit to adjust the overhead.

12-2562 (C)
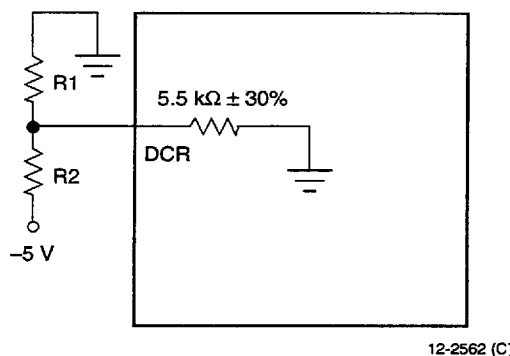
Figure 24. Equivalent Circuit for Adjusting the Overhead Voltage

The overhead voltage is programmed by using the following equation:

$$V_{OH} = 7.1 - 18.18 \; V_{DCR}$$

$$= 7.1 - 18.18 \left(-5 \times \left(\frac{R_1 \parallel 5.5k\Omega}{R_2 + R_1 \parallel 5.5k\Omega} \right) \right)$$

$$= 7.1 + 90.9 \left(\frac{R_1 \parallel 5.5k\Omega}{R_2 + R_1 \parallel 5.5k\Omega} \right)$$

Adjusting dc Feed Resistance

The dc feed resistance may be adjusted with the help of Figure 25.

12-2560 (C)
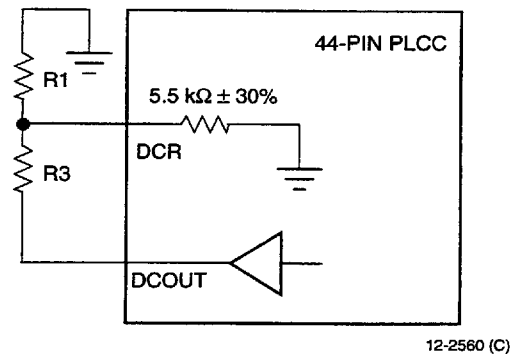
Figure 25. Equivalent Circuit for Adjusting the dc Feed Resistance

$$R_{DC} = 55\Omega + 705\Omega \frac{\Delta V_{DCR}}{\Delta V_{DCOUT}}$$

$$= 55\Omega + 705\Omega \left(\frac{R_1 \parallel 5.5k\Omega}{R_3 + R_1 \parallel 5.5k\Omega} \right)$$

Adjusting Overhead Voltage and dc Feed Resistance Simultaneously

The above paragraphs describe the independent setting of the overhead voltage and the dc feed resistance. If both need to be set to customized values, combine the two circuits as shown in Figure 26.

12-2561 (C)
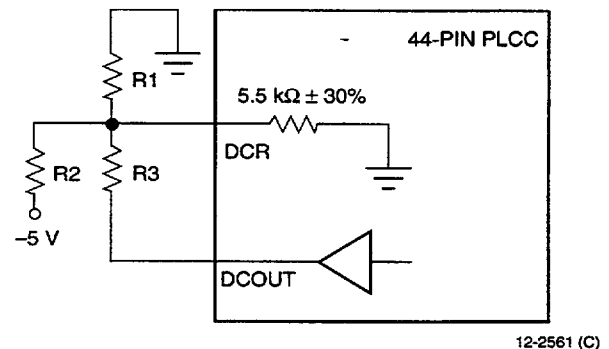
Figure 26. Adjusting Both Overhead Voltage and dc Feed Resistance

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Applications (continued)

dc Applications (continued)

This is a equivalent circuit for adjusting both the dc feed resistance and overhead voltage together.

The adjustments can be made by simple superposition of the overhead and dc feed equations:

$$V_{OH} = 7.1 + 40\left(\frac{R_1 \parallel 5.5 \text{ k}\Omega \parallel R_3}{R_2 + R_1 \parallel 5.5 \text{ k}\Omega \parallel R_3}\right)$$

$$R_{DC} = 55\Omega + 705\Omega\left(\frac{R_1 \parallel 5.5\text{k}\Omega}{R_3 + R_1 \parallel 5.5 \text{ k}\Omega}\right)$$

When selecting external components, select R1 on the order of 5 kΩ to minimize the programming inaccuracy caused by the internal 25 kΩ resistor. Lower values can be used; the only disadvantage is the power consumption of the external resistors.

Loop Range

The equation below can be rearranged to provide the loop range for a required loop current:

$$R_L = \frac{|V_{BAT}| - V_{OH}}{I_L} - 2R_P - R_{DC}$$

Off-Hook Detection

The loop closure comparator has built-in longitudinal rejection, eliminating the need for an external 60 Hz filter. This applies in both powerup and low-power scan states. The loop closure detection threshold is set by resistor R_{LCTH}. Referring to Figure 27, NLC is high in an on-hook condition ($I_{TR} = 0$, $V_{DCOUT} = 0$), and $V_{LCTH} = 0.05$ mA x R_{LCTH}. The off-hook comparator

goes low when V_{LCTH} crosses zero and then goes negative:

$$V_{LCTH} = 0.05 \text{ mA} \times R_{LCTH} + V_{DCOUT}$$

$$= 0.05 \times R_{LCTH} - 0.04167 \text{ V/mA} \times I_{TR}$$

$$R_{LTCH}(\text{k}\Omega) = 8.33 \times I_{TR}(\text{mA})$$
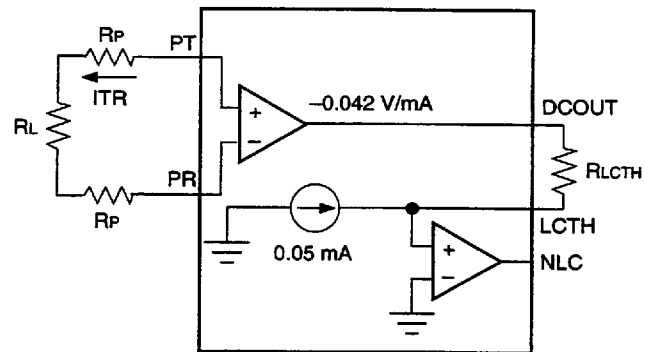
12-2553.a (C)

Figure 27. Off-Hook Detection Circuit

Ring Ground Detection

Pin ICM sinks a current proportional to the longitudinal loop current. It is also connected to an internal comparator whose output is pin RGDET. In a ground start application where TIP is open, the ring ground current is half differential and half common mode. In this case, to set the ring ground current threshold, connect a resistor R_{ICM} from pin ICM to Vcc. Select the resistor according to the following relation:

$$R_{ICM}(\text{k}\Omega) = \frac{V_{CC} \times 120}{I_{RG}(\text{mA})}$$

The above equation is shown graphically in Figure 17. It applies for the case of TIP open. The more general equation can be used in ground key application to detect a common-mode current I_{CM}:

$$R_{ICM}(\text{k}\Omega) = \frac{V_{CC} \times 60}{I_{CM}(\text{mA})}$$

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Applications (continued)

Power Derating

Thermal considerations can affect the choice of 32-pin PLCC or 44-pin PLCC package. Operating temperature range, maximum current limit, maximum battery voltage, minimum dc loop, and protection resistor values will influence the overall thermal performance. This section shows the relevant design equations and considerations in evaluating the SLIC thermal performance.

First, consider the LUCL8560 SLIC in a 44-pin PLCC package. The still air thermal resistance is 47 °C/W, however, this number implies zero air flow as if the LUCL8560 were totally enclosed in a box. A more realistic number would be 43 °C/W. This is an experimental number that represents a thermal impedance with no forced air flow (i. e. from a muffin fan), but from the natural air flow as seen in a typical switch cabinet.

The SLIC will enter the thermal shutdown state at typically 165 °C. The thermal shutdown design should ensure that the SLIC temperature does not reach 165 °C under normal operating conditions.

Assume a maximum ambient operating temperature of 85 °C, a maximum current limit of 45 mA, and a maximum battery of –52 V. Further, assume a (worst case) minimum dc loop of 100 Ω and that 100 Ω protection resistors are used at both Tip and Ring.

1. $T_{TSD} - T_{AMBIENT(max)}$ = allowed thermal rise.

    165 °C – 85 °C = 80 °C

2. Allowed thermal rise = package thermal impedance $\bullet$ SLIC power dissipation.

    80 °C = 43 °C/W $\bullet$ SLIC power dissipation

    SLIC power dissipation (P_{DISS}) = 1.9 W

Thus, if the total power dissipated in the SLIC is less than 1.9 W, it will not enter the thermal shutdown state. Total SLIC power is calculated as:

Total P_{DISS} = Maximum battery $\bullet$ Maximum current limit + SLIC quiescent power.

For the LUCL8560, SLIC quiescent power (P_Q) is approximated at 0.167 W. Thus,

Total P_{DISS} = (–52 V $\bullet$ 45 mA) + 0.167 W

Total P_{DISS} = 2.34 W + 0.167 W

Total P_{DISS} = 2.507 W

The power dissipated in the SLIC is the total power dissipation less the power that is dissipated in the loop.

SLIC P_{DISS} = Total power – Loop power

Loop power = $(I_{LIM})^2 \bullet (R_{dcLOOP} \text{ min} + 2R_P)$

Loop power = $(45 \text{ mA})^2 \bullet (100\ \Omega + 200\ \Omega)$

Loop power = 0.61 W

SLIC power = 2.507 W – 0.61 W

SLIC power = 1.897 W < 1.9 W

Thus, in this example, the thermal design ensures that the SLIC will not enter the thermal shutdown state.

The next example uses the 32-pin PLCC package and demonstrates the technique used to determine the maximum allowed current.

In this example, assume a 0 °C to 70 °C operating range. Thus,

$T_{TSD} - T_{AMBIENT (max)}$ = Allowed thermal rise

165 °C –70°C = 95 °C

To estimate the open-air thermal impedance, use the 43 °C/W parameter from the 44-pin PLCC and ratio the lead count.

Thermal Impedance (32-pin PLCC) = 48 °C/W $\bullet \left[\dfrac{44}{32}\right]$ = 59 °C/W

Again:

Allowed thermal rise = Thermal impedance $\bullet$ SLIC power dissipation

95 °C = 59 °C/W $\bullet$ SLIC power dissipation

SLIC P_{DISS} = 1.6 W

In this example again assume the dc loop + 2 $\bullet$ protection resistors = 300 Ω, then:

$(I_{LIM})(V_{BAT} \text{ max}) + P_Q - (I_{LIM})^2 (R_{dc} + 2\ R_P)$ = 1.6 W

I $\bullet$ 52 + 0.167 – I^2 300 = 1.6 W

300 I^2 – 52 I + 1.433 = 0

This is a quadratic equation whose solution is in the form:

$$X = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

$$I_{LIM} = \frac{52 \pm \sqrt{52^2 - (4)(300)(1.433)}}{2(300)}$$

$$I_{LIM} = \frac{52 \pm 31.4}{600}$$

Ignore the "+" term:

$$I_{LIM} = \frac{52 - 31.4}{600} = 34 \text{ mA}$$

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Applications (continued)

Power Derating (continued)

Thus, 34 mA is the maximum allowable current limit in the 32-pin PLCC package under the conditions given in this example.

This type of analysis should be performed under the conditions of the user's particular application to ensure adequate thermal design.

Battery Switch

The LUCL8560 SLIC provides an input for an auxiliary battery. Called VBAT2, this power supply should be lower in magnitude than the primary battery VBAT1. Under an acceptable loop condition, VBAT2 can be switched to provide the loop power through the amplifiers of the SLIC. The dc template, described in previous sections, is determined by the battery that is active—either VBAT1 or VBAT2.

There are several important applications where use of a lower voltage battery in the off-hook state is desired to provide dc current to the loop, yet a higher voltage battery is desired in on-hook or ringing modes. These applications are typically short loop applications, such as an ISDN terminal adaptor, Fiber-in-the-Loop applications, or a cable telephony interface.

In these applications, typically the maximum dc loop resistance (which includes the off-hook telephone handset plus twisted cable pair) is relatively low. For example, Bellcore TA909, *Generic Requirements and Objectives for Fiber in the Loop Systems*, specifies that in the off-hook state, 20 mA must be provided into a 430 Ω dc loop. To meet these requirements, a lower battery in the off-hook condition is important to minimize off-hook power consumption. Power conservation is important from a cost of energy point of view, and is vital in remotely powered POTs interface applications.

While use of a low-voltage battery in off-hook short dc loops is important, certain on-hook applications, such as providing a balanced power ring signal or to maintain compatibility with certain CPE such as answering machines may require a higher magnitude battery.

With the logic controlled battery switch, the LUCL8560 is able to provide a higher voltage battery to meet on-hook battery voltage requirements. At the same time, the LUCL8560 can accept a lower voltage auxiliary battery during short loop off-hook applications. If a dc-dc convertor with two fixed voltage outputs is used, tie the battery voltage that is higher in magnitude to VBAT1 and the voltage that is lower in magnitude to VBAT2. If it

is desired to use a single battery supply or a dc/dc convertor with a single programmable voltage output, tie VBAT1 to VBAT2 and connect the battery to this node. Note that VBAT1 is forced during the balanced ringing state.

Power Ringing

The LUCL8560 Ringing SLIC is designed to generate a balanced trapezoidal power ring signal to Tip and Ring. Because the SLIC itself generates the power ringing signal, no ring relay is needed in this mode of operation. Alternatively, the LUCL8560 SLIC can also be used in the more standard battery-backed, unbalanced ringing application. In this case, the ring signal is generated by a central ring generator and is bussed to individual Tip-Ring pairs. A "ringing" relay is used during ringing to disconnect the SLIC from, and apply the ring generator to, the Tip and Ring pair.

This section discusses in detail the use of the LUCL8560 ringing SLIC in either mode of application.

Ringing SLIC Balanced Ring Signal Generation

POTS for ISDN Terminal Adapters

The LUCL8560 Ringing SLIC is designed to provide a balanced trapezoidal power ring signal to Tip and Ring. This mode of operation is suited for short loop, plain old telephone service (POTS) applications, such as ISDN terminal adapters (TA).

When ISDN was first visualized, it was thought we would all exchange our existing telephones for new, high-featured ISDN phones. Digital technology would drive these sets to very low costs. While this may happen in the future, the current demand is for the ISDN TA to service a standard analog telephone. The challenges of this application are discussed here along with a suggested solution.

Until recently, POTS has been the exclusive domain of the service provider. Over its 100-year history, any architectural change was always required to be compatible with the existing installed local loop plant and all telephone sets.

If this is the expectation of the TA, it would be capable of being connected into the residence phone wiring to drive every phone in the house. It would also be designed with enough backup battery to provide uninterrupted service during electrical power interruptions. In this case, adherence to a standard, such as Bellcore's TR-909, is recommended.

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Applications (continued)

Power Ringing (continued)

For the case where a TA is only going to provide limited service, the design can be made less costly by limiting the scope of the device. An example of this limited scope would be the provision of s analog jacks for a fax/modem and a phone set near the TA in a home office environment. A block diagram of a POTS design is outlined in Figure 28.
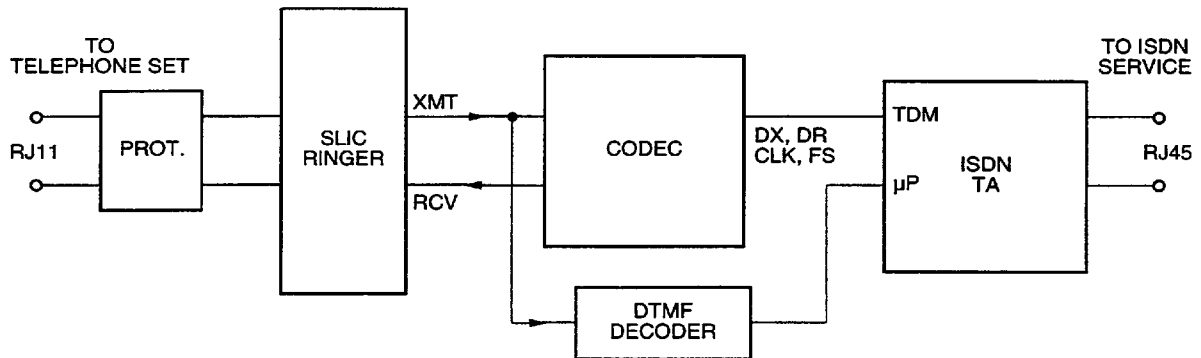
12-3286

Figure 28. POTS Controlled from an ISDN Terminal Adaptor

The table below outlines the comparison of the main specifications associated with this mode of operation.

Parameter	Bellcore TA-909	Typical New Phone
Protection	Must pass lightning and power cross require-ments.	Won't see lightning if not wired throughout the house. Could see customer misuse.
Ringing	Must be single-ended (unbalanced). Must deliver 40 Vrms into 5 REN load, not including loop. Non-square wave (e.g., trapezoid) is permissible. Magnitude of negative dc level must be less than 75 V. Pretrip immunity to 6 μF II 10 k Ω.	Newer phones (1986 to present) are typically under 1 REN. Balanced or single-ended source will work. –
SLIC	On-hook, must provide 40 V. Off-hook, must provide 20 mA into 530 Ω.	10 V on-hook enough for phone. Allow at least 25 V on-hook for some fax and answering machines.
Codec	Must meet ITU-T (formerly CCITT).	Should meet ITU-T (formerly CCITT).

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Applications (continued)

Power Ringing (continued)

Crest Factor

The balanced ring signal is generated by simply toggling the SLIC between the powerup state forward and powerup reverse battery states. The state change is done by applying a square wave (whose frequency is the desired ring frequency) to logic input B1. Capacitors FB1 and FB2 are used to control or ramp the speed of the transition of the battery reverse, thus "shaping" the balanced ring signal. Setting capacitor FB1 = FB2 = 0.0047 μF will give a crest factor that meets the Bellcore TA-909 requirement of ringing waveform crest factor between 1.2 and 1.6. Ringing waveforms of crest factors 1.6 and 1.2 are shown in Figure 29 and Figure 30.
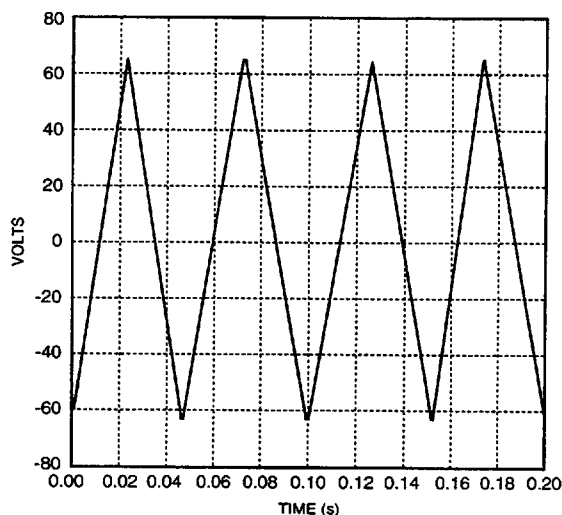
Slew Rate = 5.65 V/ms
trise = tfall = 23 ms
pwidth = 2 ms
period = 50 ms

12-3346 (C)

Figure 29. Ringing Waveform Crest Factor = 1.6
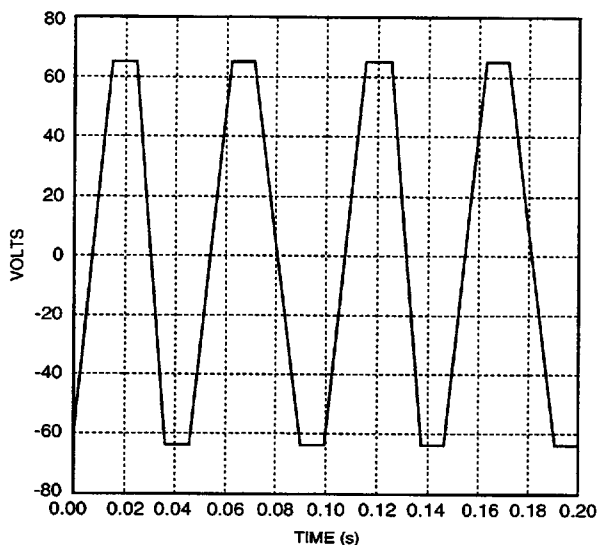
Slew Rate = 10.83 V/ms
trise = tfall = 12 ms
pwidth = 13 ms
period = 50 ms

12-3347 (C)

Figure 30. Ringing Waveform Crest Factor = 1.2

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Applications (continued)

Power Ringing (continued)

Power Ringing Load

Bellcore TA-909 specifies that a minimum 40 Vrms must be delivered to a 5 REN ringing load of 1380 Ω + 40 μF. During the ringing state, VBAT1 is automatically applied to the Tip/Ring power amplifiers. For 5 REN load it is recommended that VBAT1 be set to –65 Vdc. Also during the power ring state, the dc current limit is automatically boosted by a factor of 2.8 over the current limit set by resistor RPROG. Both of these factors are necessary to ensure delivery of 40 Vrms to the North American 5 REN ringing load of 1380 Ω + 40 μF.

Current-Limit Switch

The dc current is limited to a value determined by eternal resistor RPROG, an internal current source and the gain from Tip/Ring to pin DCOUT. Current limit is set by the equation:

$$I_{PROG} * R_{PROG} = I_{LIM} * B_{DCOUT}$$

Where:

I_{PROG} = the current from an internal current source
R_{PROG} = the external resistor used to set the current limit
Bdcout = the tranconductance from Tip/Ring to DCOUT which is nominally 41.67 V/A

During non-ringing modes, the internal current source is set at 75 μA, thus:

$$I_{PROG} * R_{PROG} = I_{LIM} * B_{DCOUT}$$

$$R_{PROG} = I_{LIM} * B_{DCOUT}/I_{PROG}$$

$$R_{PROG}(K) = I_{LIM} (mA) * 0.04167 (V/mA) / 75E\text{-}3 (mA)$$

$$R_{PROG}(K) = 0.556 * I_{LIM} (mA) - \text{Non-ringing Modes}$$

During the ring mode, the current limit is automatically increased by a factor of 2.8. This is done to provide sufficient ring to a true North American 5 REN load. This is done internally by increasing the value of I_{PROG} from 75 μA to 210 μA, thus:

$$I_{PROG} * R_{PROG} = I_{LIM} * B_{DCOUT}$$

$$R_{PROG} = I_{LIM} * B_{DCOUT}/I_{PROG}$$

$$R_{PROG}(K) = I_{LIM} (mA) * 0.04167 (V/mA) / 210E\text{-}3 (mA)$$

$$R_{PROG}(K) = 0.198 * I_{LIM} (mA) - \text{Ringing Mode}$$

Note that in either mode, the current limit region of the dc template has a high resistance (10K).

Applications (continued)

Power Ringing (continued)

Ring Trip

Ring trip is accomplished by filtering the voltage seen at node DCOUT and applying it to the integrated ring trip comparator. DCOUT is a voltage proportional to the Tip/Ring current, and under short dc loop conditions, on-hook ringing current and off-hook current provide sufficient voltage differential at DCOUT to distinguish a ring trip condition has occurred. The ring trip comparator threshold is set via a resistor between the ring trip comparator and ground.

Output NSTAT is automatically set to detect ring trip during the balanced ring mode. During quiet intervals of ringing, output NSTAT is automatically determined by the loop closure detector.

The equivalent ring trip circuit for the balanced Ringing SLIC application is shown in Figure 31.
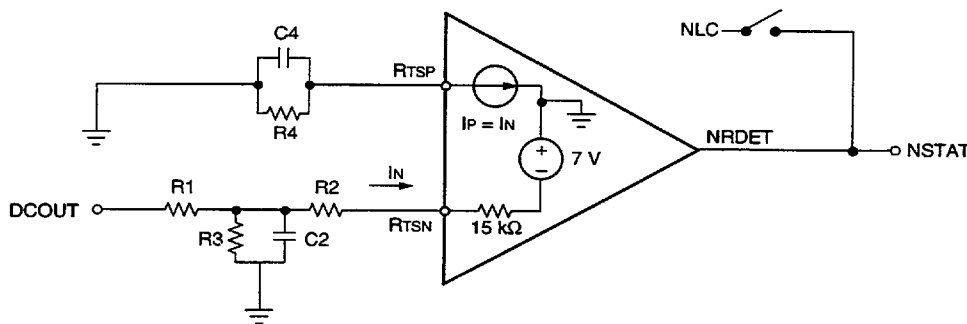
12-3349 (C)

Figure 31. Equivalent Ring Trip Circuit for Balanced Ringing SLIC

The equations governing Ring Trip are derived below.

Capacitors C2 and C4 in conjunction with resistors R2 and R4 for a double pole low pass filter that smooth the voltage seen at DCOUT. The poles of the filters are determined by C2 and C4. Where these poles are set will influence both the ripple seen at DCOUT and the speed of the transistor of the voltage at DCOUT from the pre-trip to the tripped level. For the derivation of the ring trip threshold equations, capacitors C2 and C4 can be ignored.

Redrawing the circuit, ignoring the capacitors, and taking the Thevevin equivalent circuit of the network at RTSN gives:
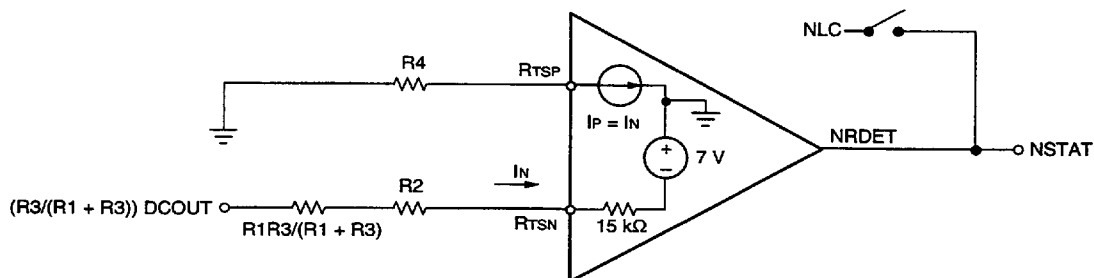
12-3348 (C)

Figure 32. Thevevin Equivalent Ring Trip Circuit for Balanced Ringing SLIC

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Applications (continued)

Power Ringing (continued)

$$I_{RSTN} = \frac{\left(\dfrac{R_S}{R_3 + R_1} V_{DCOUT}\right) - (-7V)}{\dfrac{R_1 R_3}{R_1 + R_3} + R_2 + 15K}$$

At the trip point, the internal current repeater will force I_{RTSP} to be equal to I_{RTSN} and V_{RTSP} will be equal to V_{RTSN}, which is –7 V. Thus at the trip point:

$$I_{RTSN} = I_{RTSP} = \frac{0 - (-7)}{R_4}$$

Thus:

$$\frac{\left(\dfrac{R_3}{R_3 + R_1}\right) V_{DCOUT} + 7V}{\dfrac{R_1 R_3}{R_1 + R_3} + R_2 + 15k} = \frac{7V}{R_4}$$

Solving for V_{DCOUT}, the voltage at DCOUT at the ring trip point is given by:

$$V_{DCOUT} \atop (TRIP)} = 7(R_3 + R_1)\left[\frac{R_1}{R_1 R_4 + R_3 R_4} + \frac{R_2}{R_3 R_4} + \frac{15(k)}{R_3 R_4} - \frac{1}{R_3}\right]$$

The loop current at ring trip is given by:

$$I_{LOOP(TRIP)} = (V_{DCOUT})/(\beta_{DCOUT})$$

For the LUCL8560, the gain (β) at pin DCOUT is 41.67 V/A.

Capacitors C_2 and C_4 along with resistors R_2 and R_4, respectively, form low-pass filters to filter the ac voltage seen at DCOUT before it is applied to the ring trip comparator input. The lower the pole of the filter, the less the ripple, but also the slower the state transistor at NSTAT. Poles in the neighborhood of 2.5 Hz—3 Hz are suggested; as given by:

$$f_{LP} = (1/2)\pi R_2 C_2$$

$$f_{LP} = (1/2)\pi R_4 C_4$$

In the reference designs discussed in the next section, the ring trip threshold is set for 50 mA with:

$R_1 = 267\ k$
$R_2 = 576\ k$
$C_2 = 0.1\ \mu F$
$R_3 = 267\ k$
$R_4 = 630\ k$
$C_4 = 0.1\ \mu F$

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Applications (continued)

Power Ringing (continued)

Reference Designs for ISDN TA Applications

Two POTS circuits for reference design are shown in Figure 33 and Figure 34. In Figure 33, the LUCL8560 SLIC and T7503 Codec are used. The ac circuit is designed per Bellcore TA-909 with a 600 Ω resistive termination and hybrid circuit, with the transmit gain set for –2 dB and the receive gain set for –4 dB. The T7503 Codec is compatible with the T7237 U-interface transceiver and the T7256 SCNT1 interface.

The second POTS reference design in Figure 34 uses LUCL8560 SLIC and T7501 Codec. The ac circuit is also designed per Bellcore TA-909 with a 600 Ω resistive termination and hybrid circuit, with the transmit gain set for –2 dB and the receive gain set for –4 dB. The T7501 Codec is compatible with the T7250C S-interface IC.
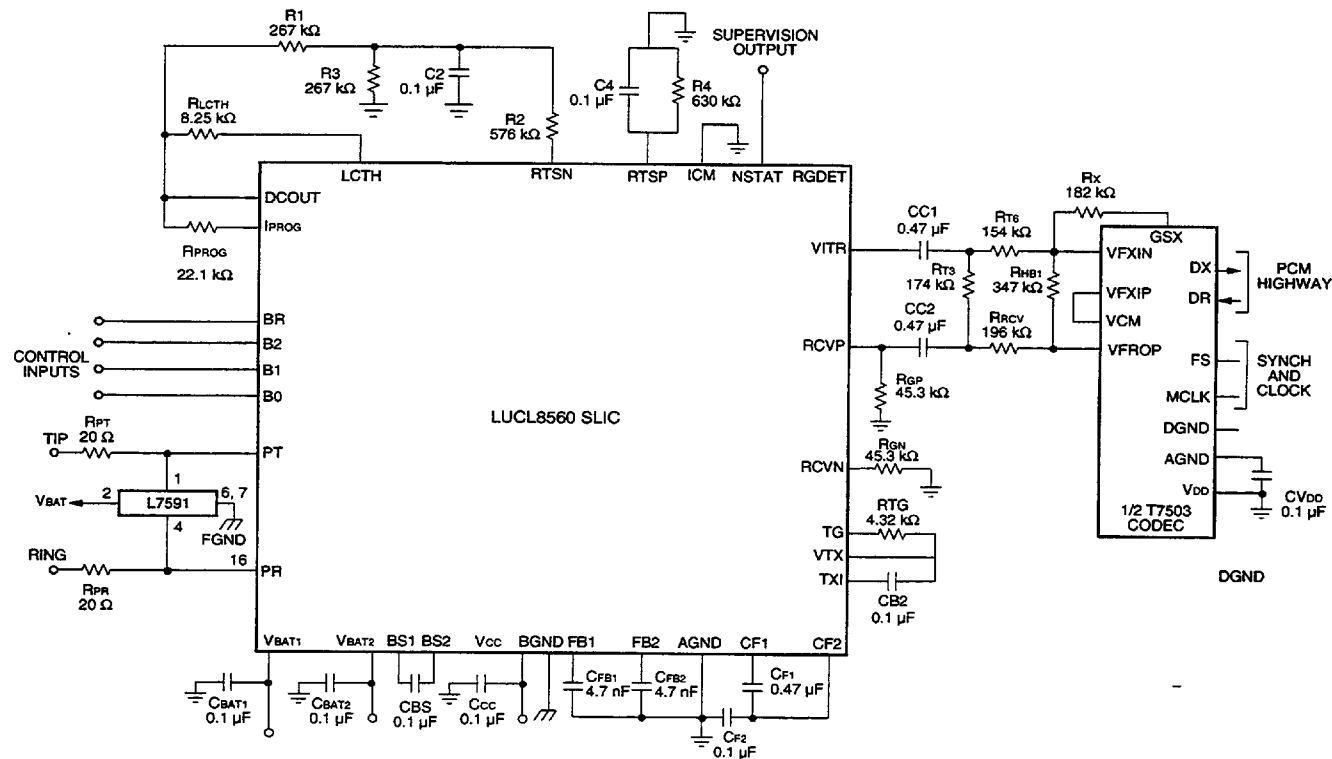
TX = –2 dB
RX = –4 dB
Termination = 600 Ω
Hybrid Balance = 600 Ω

12-3345 (C)

Figure 33. POTS Interface with Balanced Ringing using LUCL8560 SLIC and T7503 Codec

Table 10. Parts List for Balanced Ringing Using T7503 Codec

Name	Value	Function
Integrated Circuits		
SLIC	LUCL8560	Subscriber Loop Interface Circuit (SLIC).
Protector	L7591	Secondary Protection.
Codec	T7503	First Generation Codec.

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Applications (continued)

Power Ringing (continued)

Table 10. Parts List for Balanced Ringing using T7503 Codec (continued)

Name	Value	Function
Fault Protection		
R_{PT}	20 Ω PTC	Overcurrent protection.
R_{PR}	20 Ω PTC	Overcurrent protection.
Power Supply		
C_{BAT1}	0.1 μF, 20%, 100 V	V_{BAT} filter capacitor.
C_{BAT2}	0.1 μF, 20%, 100 V	V_{BAT} filter capacitor.
C_{CC}	0.1 μF, 20%, 10 V	V_{CC} filter capacitor.
C_{F1}	0.47 μF, 20%, 100 V	With C_{F2}, improves idle channel noise.
C_{F2}	0.1 μF, 20%, 100 V	With C_{F1}, improves idle channel noise.
C_{BS}	0.1 μF, 20%, 100 V	Slows battery switch transition.
dc Profile/Ringing		
C_{FB1}	4.7 nF, 20%, 100 V	With C_{FB2} slows rate of forward/reverse battery transition. Sets crest factor of balanced power ring signal.
C_{FB2}	4.7 nF, 20%, 100 V	With C_{FB1} slows rate of forward/reverse battery transition. Sets crest factor of balanced power ring signal.
R_{PROG}	22.1 kΩ, 1%, 1/4 W	Sets dc loop current.
ac Characteristics		
R_{TG}	4.32 kΩ, 1%, 1/4 W	Sets internal transmit path gain to 19.2.
C_{B2}	0.1 μF, 20%, 100 V	ac/dc separation capacitor.
C_{C1}	0.47 μF, 20%, 10 V	dc blocking capacitor.
C_{C2}	0.47 μF, 20%, 10 V	dc blocking capacitor.
R_{T3}	174 kΩ, 1%, 1/4 W	With R_{GP} and R_{RCV}, sets ac termination impedance.
R_{RCV}	196 kΩ, 1%, 1/4 W	With R_{GP} and R_{T3}, sets receive gain.
R_{GP}	45.3 kΩ, 1%, 1/4 W	With R_{T3} and R_{RCV}, sets ac termination impedance and receive gain.
R_{GN}	45.3 kΩ, 1%, 1/4 W	Compensates for input bias offset at RCVN/RCVP
R_{T6}	154 kΩ, 1%, 1/4 W	With R_X, sets transmit gain in codec.
R_X	182 kΩ, 1%, 1/4 W	With R_{T6}, sets transmit gain in codec.
R_{HB1}	374 kΩ, 1%, 1/4 W	Sets hybrid balance.
Supervision		
R_{LCTH}	8.25 kΩ, 1%, 1/4 W	Sets loop closure (off-hook) threshold.
R_1	267 kΩ, 1%, 1/4 W	With R_2, R_3, and R_4 sets ring trip threshold.
R_2	576 kΩ, 1%, 1/4 W	With R_1, R_3, and R_4 sets ring trip threshold.
C_2	0.1 μF, 20%, 50 V	With R_2 sets pole of low pass ring trip sense filter.
R_3	267 kΩ, 1%, 1/4 W	With R_1, R_2, and R_4 sets ring trip threshold.
R_4	630 kΩ, 1%, 1/4 W	With R_1, R_2, and R_3 sets ring trip threshold.
C_4	0.1 μF, 20%, 10 V	With R_4 sets pole of low pass ring trip sense filter.

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Applications (continued)

Design Considerations

Table 11 shows the design parameters of the application circuit shown in Figure 33. Components that are adjusted to program these values are also shown.

Table 11. 600 Ω Design Parameters

Design Parameter	Parameter Value	Components Adjusted
Loop Closure Threshold	10 mA	R_{LCTH}
dc Loop Current Limit	40 mA	R_{PROG}
dc Feed Resistance	55 Ω	—
2-wire Signal Overload Level	3.14 dBm	—
ac Termination Impedance	600 Ω	R_{T1}, R_{GP}, R_{RCV}
Hybrid Balance Line Impedance	600 Ω	R_{HB1}
Transmit Gain	–2 dB	R_{T6}, R_X
Receive Gain	–4 dB	R_{RCV}, R_{GP}, R_{T3}

TX = –2 dB
RX = –4 dB
Termination = 600 Ω
Hybrid Balance = 600 Ω

12-3344 (C)

Figure 34. POTS Interface with Balanced Ringing Using LUCL8560 SLIC and T7501 Codec

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Applications (continued)

Design Considerations (continued)

Table 12. Parts List for Balanced Ringing using T7501 Codec

Name	Value	Function
Integrated Circuits		
SLIC	LUCL8560	Subscriber Loop Interface Circuit (SLIC).
Protector	L7591	Secondary protection.
Codec	T7501	First generation codec.
Fault Protection		
RPT	20 Ω PTC	Overcurrent protection.
RPR	20 Ω PTC	Overcurrent protection.
Power Supply		
CBAT1	0.1 µF, 20%, 100 V	VBAT filter capacitor.
CBAT2	0.1 µF, 20%, 100 V	VBAT filter capacitor.
CCC	0.1 µF, 20%, 10 V	VCC filter capacitor.
CF1	0.47 µF, 20%, 100 V	With CF2, improves idle channel noise.
CF2	0.1 µF, 20%, 100 V	With CF1, improves idle channel noise.
CBS	0.1 µF, 20%, 100 V	Slows battery switch transition.
dc Profile/Ringing		
CFB1	4.7 nF, 20%, 100 V	With CFB2, slows rate of forward/reverse battery transition. Sets crest factor of balanced power ring signal.
CFB2	4.7 nF, 20%, 100 V	With CFB1, slows rate of forward/reverse battery transition. Sets crest factor of balanced power ring signal.
RPROG	22.1 kΩ, 1%, 1/4 W	Sets dc loop current.
ac Characteristics		
RTG	4.32 kΩ, 1%, 1/4 W	Sets internal transmit path gain to 19.2.
CB2	0.1 µF, 20%, 100 V	ac/dc separation capacitor.
RT2	90.9 kΩ, 1%, 1/4 W	With Rx, sets transmit gain.
Rx	110 kΩ, 1%, 1/4 W	With RT2, sets transmit gain.
RT1	86.6 kΩ, 1%, 1/4 W	With RGN and RRCV, sets ac termination impedance.
RRCV	80.6 kΩ, 1%, 1/4 W	With RGN and RT1, sets receive gain.
RGN	18.2 kΩ, 1%, 1/4 W	With RT1 and RRCV, sets ac termination impedance and receive gain.
RGP	13.7 kΩ, 1%, 1/4 W	Compensates for input bias offset at RCVN/RCVP.
RT3	90.9 kΩ, 1%, 1/4 W	Input to codec.
RHB1	182 kΩ, 1%, 1/4 W	Sets hybrid balance.
Supervision		
RLCTH	8.25 kΩ, 1%, 1/4 W	Sets loop closure (off-hook) threshold.
R1	267 kΩ, 1%, 1/4 W	With R2, R3, and R4 sets ring trip threshold.
R2	576 kΩ, 1%, 1/4 W	With R1, R3, and R4 sets ring trip threshold.
C2	0.1 µF, 20%, 50 V	With R2 sets pole of low pass ring trip sense filter.
R3	267 kΩ, 1%, 1/4 W	With R1, R2, and R4 sets ring trip threshold.
R4	630 kΩ, 1%, 1/4 W	With R1, R2, and R3 sets ring trip threshold.
C4	0.1 µF, 20%, 10 V	With R4, sets pole of low pass ring trip sense filter.

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Applications (continued)

Design Considerations (continued)

Table 13 shows the design parameters of the application circuit shown in Figure 34. Components that are adjusted to program these values are also shown.

Table 13. 600 Ω Design Parameters

Design Parameter	Parameter Value	Components Adjusted
Loop Closure Threshold	10 mA	R_{LCTH}
dc Loop Current Limit	40 mA	R_{PROG}
dc Feed Resistance	55 Ω	—
2-wire Signal Overload Level	3.14 dBm	—
ac Termination Impedance	600 Ω	R_{T1}, R_{GP}, R_{RCV}
Hybrid Balance Line Impedance	600 Ω	R_{HB1}
Transmit Gain	–2 dB	R_{T6}, R_X
Receive Gain	–4 dB	R_{RCV}, R_{GP}, R_{T3}

Unbalanced "Bussed" Ring Signal Application

The LUCL8560 SLIC can also be used in the standard battery-backed, unbalanced ringing application. In this case, the ring signal is generated by a central ring generator and is bussed to individual Tip/Ring pairs. A "ringing" relay is used during ringing to disconnect the SLIC from, and apply the ring generator to, the Tip and Ring pair.

Ring Trip Detection

The ring trip circuit is a comparator that has a special input section optimized for this application. The equivalent circuit is shown in Figure 35, along with its use in an application using unbalanced, battery-backed ringing.
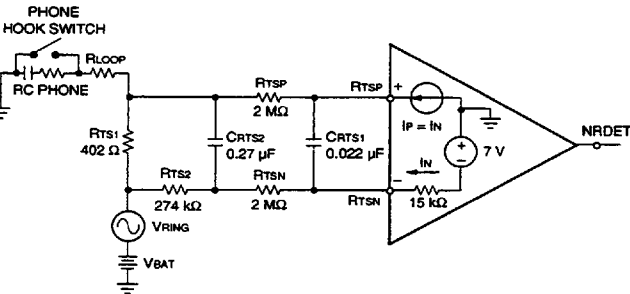
12-3014 (C)

Figure 35. Ring Trip Equivalent Circuit and Equivalent Application

The comparator input voltage compliance is Vcc to V_{BAT}, and the maximum current is 240 µA in either direction. Its application is straightforward. A resistance (R_{TSN} + R_{TS2}) in series with the R_{TSN} input establishes a current that is repeated in the R_{TSP} input. A slightly lower resistance (R_{TSP}) is placed in series with the R_{TSP} input. When ringing is being injected, no dc current flows through R_{TS1}, and so the R_{TSP} input is at a lower potential than R_{TSN}. When enough dc loop current flows, the R_{TSP} input voltage increases to trip the comparator. In Figure 35, a low-pass filter with a double pole at 2 Hz was implemented to prevent false ring trip.

The following example illustrates how the detection circuit of Figure 35 will trip at a 12.5 mA dc loop current using a –48 V battery.

$$I_N = \frac{-7 - (-48)}{2.289 \ M\Omega}$$

$$= 17.9 \ \mu A$$

The current I_N is repeated as I_P in the positive comparator input. The voltage at comparator input R_{TSP} is:

$$V_{RTSP} = V_{BAT} + I_{LOOP(dc)} \times R_{TS1} + I_P \times R_{TSP}$$

Using this equation and the values in the example, the voltage at input R_{TSP} is –12 V during ringing injection ($I_{LOOP(dc)} = 0$). Input R_{TSP} is therefore at a level of 5 V below R_{TSN}. When enough dc loop current flows through R_{TS1} to raise its dc drop to 5 V, the comparator will trip.

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Applications (continued)

Design Considerations (continued)

In this example:

$$I_{LOOP(dc)} = \frac{5\ V}{402\ \Omega}$$

$$= 12.5\ mA$$

Note that during ringing in this mode of operation, both the NLC and NRDET circuits are active. During the actual ringing, NRDET is connected and NLC is iso-lated from Tip and Ring by the ring relay, thus NSTAT reflects the status at NRDET. During quiet intervals of ringing, NLC is connected and NRDET is isolated from Tip and Ring by the ring relay, thus NSTAT reflects the status at NLC. Thus, during ring cadence, the logic input that drives the ring relay can be used as an indi-cation as to whether NRDET or NLC appears at output NSTAT.

A Basic Loop Start reference circuit, using "bussed" ringing with the LUCL8560 SLIC and T7504 first gener-ation codec is shown in Figure 36. This circuit is designed for a 600 Ω resistive termination impedance and hybrid balance. Transmit and receive gains are both set at 0 dB.

Figure 36 shows the ground start application.

TX = 0 dB
RX = 0 dB
Termination = 600 Ω
Hybrid = 600 Ω

12.2573.f (C)

Figure 36. Basic Loop Start Application Circuit Using T7504 Type Codec and "Bussed" Ringing

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Applications (continued)

Design Considerations (continued)

Figure 37. Ground Start Application Circuit

Table 14. Parts List for Loop Start with Bussed Ringing and Ground Start Applications

Name	Value	Function
Integrated Circuits		
SLIC	—	Subscriber Loop Interface Circuit (SLIC).
Protector	250 V Thyristor type (e.g., Tecor P2103/SGS TPA180B)	Secondary protection.
Ringing Relay	L7581	Switches ringing signals.
Codec	T7504	First generation codec.
Fault Protection		
R_{PT}	20 Ω PTC	Protection resistor.
R_{PR}	20 Ω PTC	Protection resistor.
Power Supply		
C_{BAT1}	0.1 µF, 20%, 100 V	V_{BAT} filter capacitor.
C_{BAT2}	0.1 µF, 20%, 100 V	V_{BAT} filter capacitor.
C_{CC}	0.1 µF, 20%, 10 V	V_{CC} filter.
C_{F1}	0.47 µF, 20%, 100 V	With C_{F2}, improves idle channel noise.
C_{F2}	0.1 µF, 20%, 100 V	With C_{F1}, improves idle channel noise.
C_{BS}	0.1 µF, 20%, 100 V	Slows battery switch transition.
dc Profile		
R_{PROG}	22.1 kΩ, 1%, 1/4 W	Sets dc loop current.

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Applications (continued)

Design Considerations (continued)

Table 14. Parts List for Loop Start with Bussed Ringing and Ground Start Applications (continued)

Name	Value	Function
ac Characteristics		
RGX	4.32 kΩ, 1%, 1/4 W	Sets internal transmit path gain of 9.6.
CB2	0.1 μF, 20%, 100 V	ac/dc separation capacitor.
RT3	174 kΩ, 1%, 1/4 W	With RGP and RRCV, sets ac termination impedance.
RRCV	113 kΩ, 1%, 1/4 W	With RGP and RT3, sets receive gain.
RGP	48.7 kΩ, 1%, 1/4 W	With RT3 and RRCV, sets ac termination impedance and receive gain.
RGN	48.7 kΩ, 1%, 1/4 W	Compensates for input bias offset at RCVN/RCVP.
CC1	0.47 μF, 20%, 10 V	dc blocking capacitor.
CC2	0.47 μF, 20%, 10 V	dc blocking capacitor.
RT6	121 kΩ, 1%, 1/4 W	With Rx, sets transmit gain in codec.
Rx	182 kΩ, 1%, 1/4 W	With RT6, sets transmit gain in codec.
RHB1	182 kΩ, 1%, 1/4 W	Sets hybrid balance.
Supervision		
RLCTH	8.25 kΩ, 1%, 1/4 W	Sets loop closure (off-hook) threshold.
RTS1	402 Ω, 5%, 2 W	Ringing source series resistor.
RTS2	274 kΩ, 5%, 1/4 W	With CRTS2, forms 1st pole of a double pole, 2 Hz ring trip sense filter.
CRTS1	0.022 μF, 20%, 5 V	With RTSN and RTSP, forms 2nd 2 Hz filter pole.
CRTS2	0.27 μF, 20%, 100 V	With RTS2, forms 1st 2 Hz filter pole.
RTSN	2 MΩ, 5%, 1/4 W	With CRTS1 and RTSP, forms 2nd 2 Hz filter pole.
RTSP	2 MΩ, 5%, 1/4 W	With CRTS1 and RTSN, forms 2nd 2 Hz filter pole.
RLK	2.58 MΩ, 5%, 1/4 W	Sets loop leakage detection threshold.
Ground Start		
CICM	0.47 μF, 20%, 10 V	Provides 60 Hz filtering for ring ground detection.
RGDET	100 kΩ, 20%, 1/4 W	Digital output pull-up resistor.
RICM2	82.5 kΩ, 1%, 1/4 W	Sets ring ground detection threshold.

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Applications (continued)

Design Considerations (continued)

Table 15 shows the design parameters of the application circuit shown in Figure 36. Components that are adjusted to program these values are also shown.

Table 15. 600 Ω Design Parameters

Design Parameter	Parameter Value	Components Adjusted
Loop Closure Threshold	10 mA	R_{LCTH}
dc Loop Current Limit	40 mA	R_{PROG}
dc Feed Resistance	55 Ω	—
2-wire Signal Overload Level	3.14 dBm	—
ac Termination Impedance	600 Ω	R_{T3}, R_{GP}, R_{RCV}
Hybrid Balance Line Impedance	600 Ω	R_{HB1}
Transmit Gain	0 dB	R_{T6}, R_X
Receive Gain	0 dB	R_{RCV}, R_{GP}, R_{T3}

ac Design

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is done from the PCM highway to the transmit port. Finally, the **hybrid balance** network cancels the unwanted amount of the receive signal that appears at the transmit port.

At this point in the design, the codec needs to be selected. The discrete network between the SLIC and the codec can then be designed. Below is a brief codec feature and selection summary.

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and μ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, and μ-law/A-law selectability. This generation of codec has the lowest cost. It is most suitable for applications with fixed gains, termination impedance, and hybrid balance.

Second-Generation Codecs

This class of devices includes a microprocessor interface for software control of the gains and hybrid balance. The hybrid balance is included in the device. ac programmability adds application flexibility and saves several passive components. It also adds several I/O latches that are needed in the application. It does not have the transmit op amp, since the transmit gain and hybrid balance are set internally.
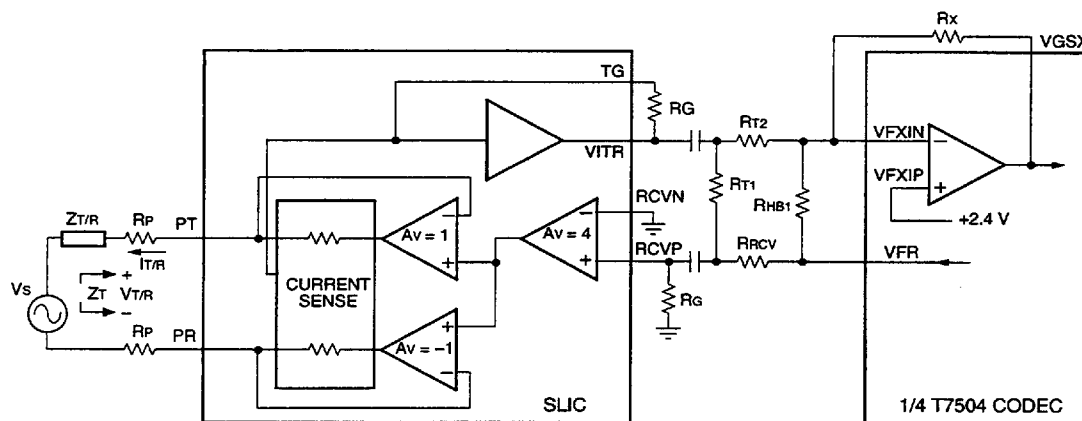
Third-Generation Codecs

This class of devices includes the gains, termination impedance, and hybrid balance—all under microprocessor control. Depending on the device, it may or may not include latches.

In the codec selection, increasing software control and flexibility are traded for device cost. To help decide, it may be useful to consider the following: Will the application require only one value for each gain and impedance? Will the board be used in different countries with different requirements? Will several versions of the board be built? If so, will one version of the board be most of the production volume? Does the application need only real termination impedance? Does the hybrid balance need to be adjusted the in the field?
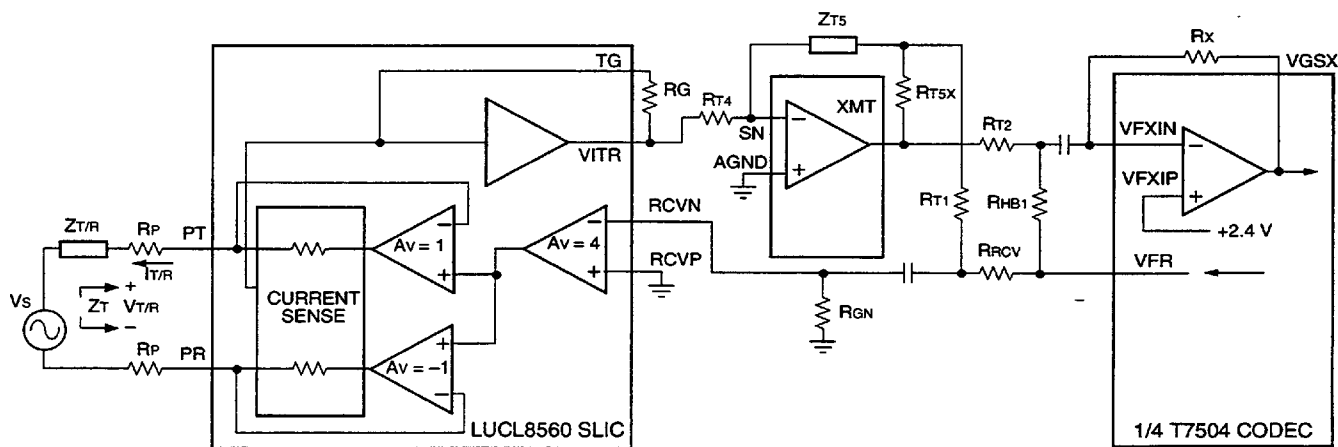
 ■ 0050026 0021196 18T ■

Applications (continued)

ac Design (continued)

ac equivalent circuits using a T7504 Codec (Vcc only) are shown in Figures 38 and 39.

Figure 38. ac Equivalent Circuit Not Including Spare Op Amp

Figure 39. ac Equivalent Circuit Including Spare Op Amp

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Applications (continued)

ac Design (continued)

In the preceding examples, use of a first-generation codec is shown. The equations for second- and third-generation codecs are simply subsets of these. There are two examples below: The first shows the simplest circuit, which uses a minimum number of discrete components to synthesize a real termination impedance. The second example shows the use of the uncommitted op amp to synthesize a complex termination. The design has been automated in a DOS-based program, available on request.

Example 1, Real Termination:

The following design equations refer to the circuit in Figure 38. Use these to synthesize real termination impedance.

Termination Impedance:

$$z_T = \frac{V_{T/R}}{-i_{tr}}$$

$$z_T = 2R_P + \frac{3200}{1 + \frac{R_{T1}}{R_{GP}} + \frac{R_{T1}}{R_{RCV}}}$$

Receive Gain:

$$g_{rcv} = \frac{V_{t/r}}{V_{FR}}$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T1}} + \frac{R_{RCV}}{R_{GP}}\right)\left(1 + \frac{z_T}{Z_{T/R}}\right)}$$

Transmit Gain:

$$g_{tx} = \frac{V_{GSX}}{V_{T/R}}$$

$$g_{tx} = \frac{-R_x}{R_{T2}} \times \frac{400}{Z_{T/R}}$$

Hybrid Balance:

$$h_{bal} = 20\log\left(\frac{R_x}{R_{HB}} - g_{tx} \times g_{rcv}\right)$$

$$h_{bal} = 20\log\left(\frac{V_{GSX}}{V_{FR}}\right)$$

To optimize the hybrid balance, the sum of the currents at the VFX input of the codec op amp should be set to 0. The expression for ZHB becomes:

$$R_{HB}(k\Omega) = \frac{R_x}{g_{tx} \times g_{rcv}}$$

Example 2, Complex Termination.

For complex termination, the spare op amp is used (see Figure 39).

$$z_T = 2R_P + \frac{3200}{1 + \frac{R_{T3}}{R_{GN}} + \frac{R_{T3}}{R_{RCV}}}\left(\frac{Z_{T5}}{R_{T4}}\right)$$

$$= 2R_P + k(Z_{T5})$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GN}}\right)\left(1 + \frac{z_T}{Z_{T/R}}\right)}$$
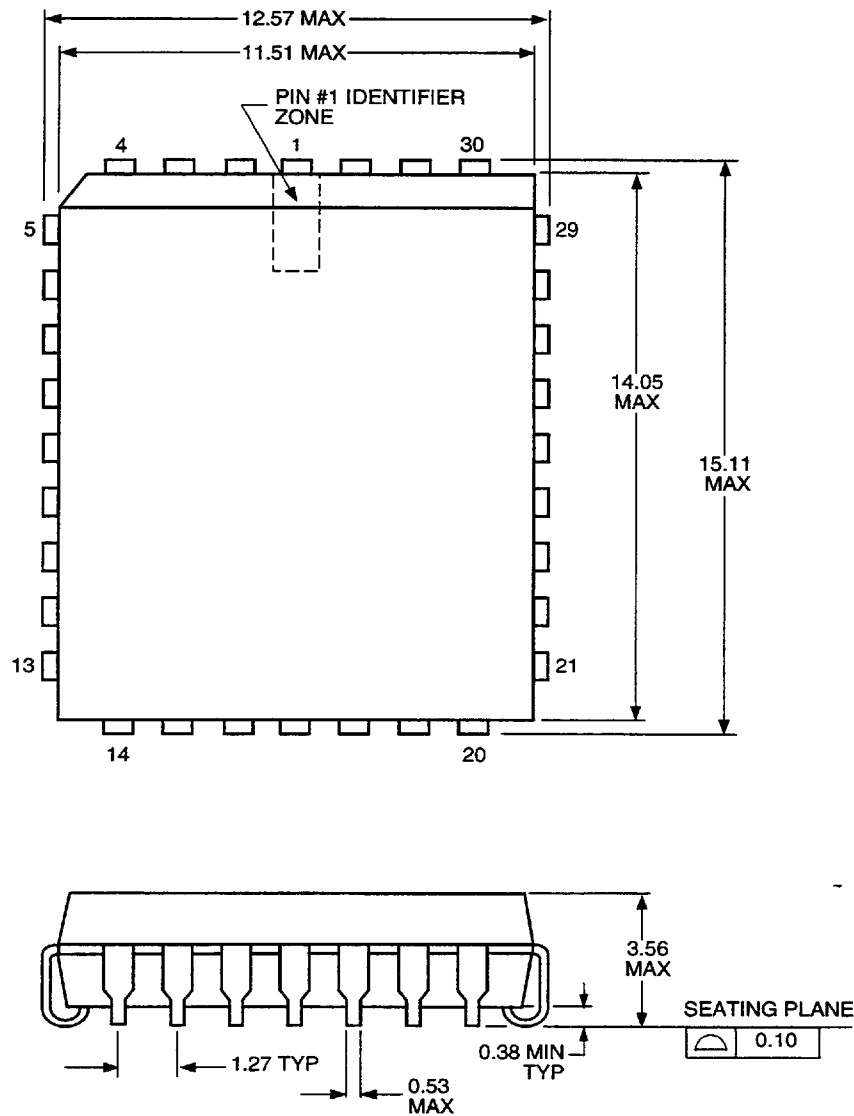
$$g_{tx} = \frac{R_x}{R_{T6}} \times \frac{400}{Z_{T/R}} \times \frac{Z_{T5}}{R_{T4}}\left(1 + \frac{R_{T5X}}{Z_{T5}} + \frac{R_{T5X}}{R_{T3} + R_{GN}||R_{RCV}}\right)$$

The hybrid balance equation is the same as in Example 1.

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Outline Diagrams

Dimensions are in millimeters.

32-Pin PLCC

5-3813

Outline Diagrams (continued)

Dimensions are in millimeters.

44-Pin PLCC

5-2506r.7

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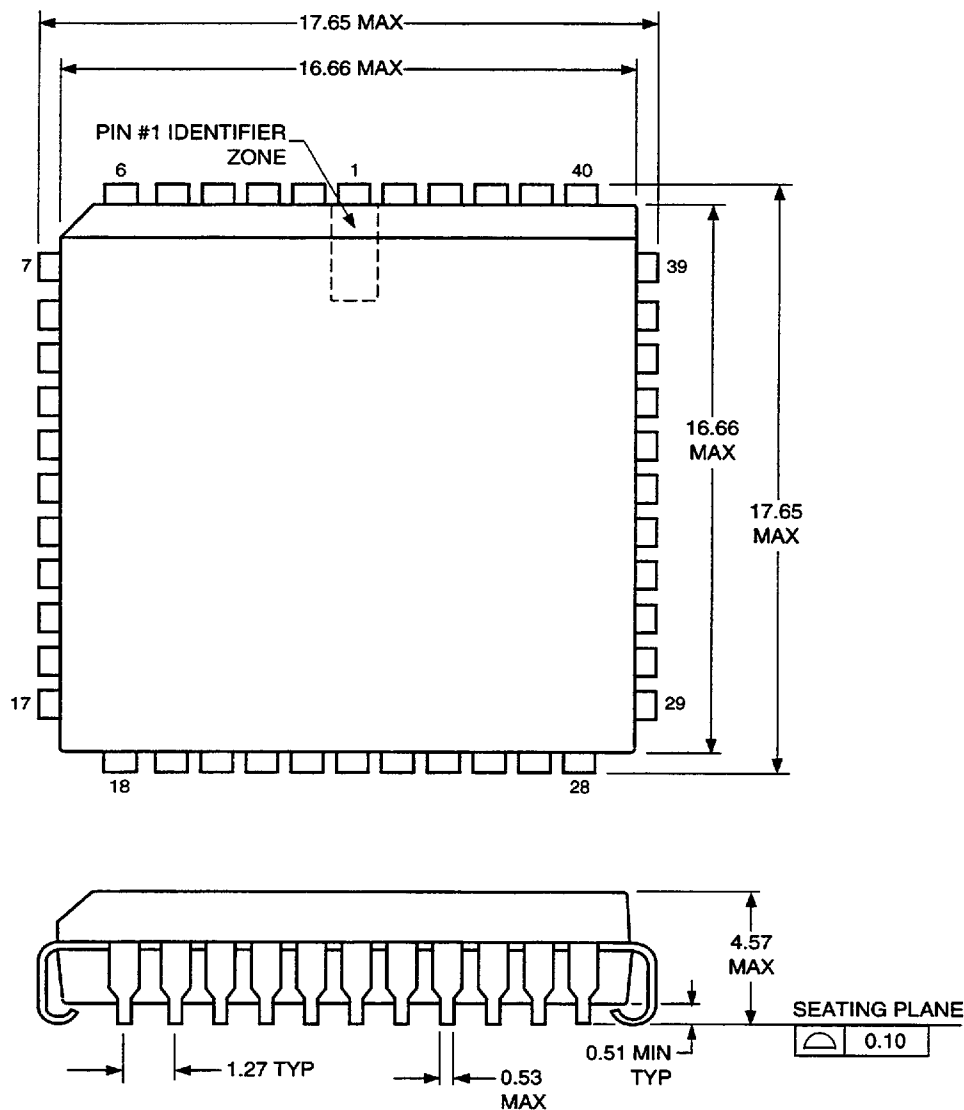
Ordering Information

Device Code	Description	Package	Comcode
ATTL8560AU	Full Feature Low-Power SLIC	32-pin PLCC	TBD
ATTL8560AP	Full Feature Low-Power SLIC	44-pin PLCC	TBD

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