TDA8596

I²C-bus controlled 4 × 45 W power amplifier with symmetrical inputs

Rev. 02 — 8 November 2007 Product data sheet

1. General description

The TDA8596 is a quad Bridge Tied Load (BTL) audio power amplifier with symmetrical inputs, made in BCDMOS technology. It contains four independent amplifier channels in BTL configuration with complementary (PMOST/NMOST) output stages. Temperature warning and output signal clipping diagnosis is possible via the I²C-bus and via the diagnostic pins (DIAG and STB pin). The temperature pre-warning level and clip detection levels can be programmed via the I²C-bus. The status of each amplifier channel (i.e. output offset, load connected or not, short circuit condition at the output pins) can be read out separately.

2. Features

2.1 General

- Operates in legacy mode (non I²C-bus) and I²C-bus mode (3.3 V and 5 V compliant)
- Three hardware-programmable I²C-bus addresses
- Drives 4 Ω or 2 Ω loads
- Balanced/symmetrical inputs
- Speaker fault detection
- Programmable gain (26 dB and 16 dB) also available in legacy mode
- Independent short circuit protection per channel
- Loss of ground and loss of V_P safe (with 300 mΩ series impedance and a maximum supply decoupling capacitor of 2200 μF)
- All outputs are short-circuit proof to ground, supply voltage and across the load
- All pins are short circuit proof to ground
- Temperature-controlled gain reduction to prevent audio holes at high junction temperatures
- Low battery voltage detection
- Qualified in accordance with AEC-Q100

2.2 I²C-bus mode

- DC load detection: open (no load), normal load, line-driver load
- AC load (tweeter) detection
- Detect which load is connected during start-up to allow the system to be configured to select the gain accordingly (e.g. line-driver mode or normal mode).
- Independently selectable soft mute of front (channel 1 and channel 3) and rear channels (channel 2 and channel 4)

- Independently programmable gain (26 dB and 16 dB) of front (channel 1 and channel 3) and rear (channel 2 and channel 4) channels
- Flexible programmable diagnostic levels:
  - Programmable clip detect: 2 %, 5 % or 10 %
  - Programmable thermal pre-warning
- Selectable information on the DIAG or STB pin:
  - The STB pin can be programmed/multiplexed with second clip detection
  - Clip information of each channel separately can be directed to the DIAG pin or the STB pin
  - Independent enabling of thermal-, clip- or load fault (short across the load, to V_P or to ground) available on the DIAG pin
- Offset detection

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_P	supply voltage	R_L = 4 Ω	8	14.4	18	V
I_q	quiescent current	no load	-	270	400	mA
P_o	output power	R_L = 4 Ω; V_P = 14.4 V; maximum power; V_i = 2 V (RMS) square wave	37	40	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 0.5 %	18	20	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 10 %	23	25	-	W
		R_L = 2 Ω; V_P = 14.4 V; maximum power; V_i = 2 V (RMS) square wave	58	64	-	W
THD	total harmonic distortion	R_L = 4 Ω; f = 1 kHz; P_o = 1 W to 12 W	-	0.01	0.1	%
$V_{n(o)}$	noise output voltage	filter 20 Hz to 22 kHz; R_S = 1 kΩ				
		normal mode; T_{amb} = 25 °C to 105 °C	-	45	65	μV
		normal mode; T_{amb} = −20 °C to 25 °C	-	45	110	μV
		line driver mode	-	22	29	μV

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8596TH	HSOP36	plastic, heatsink small outline package; 36 leads; low stand-off height	SOT851-2

5. Block diagram

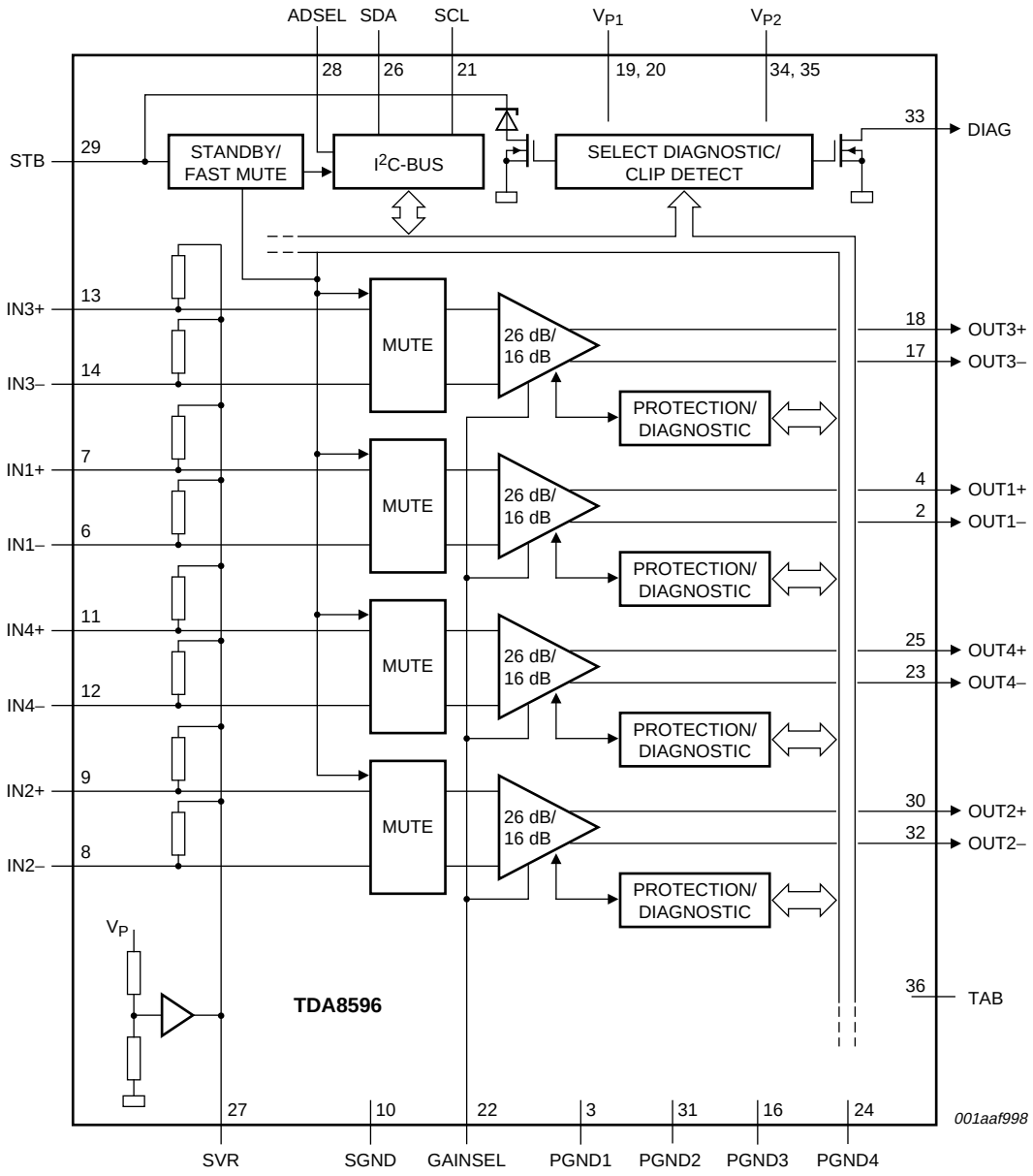


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

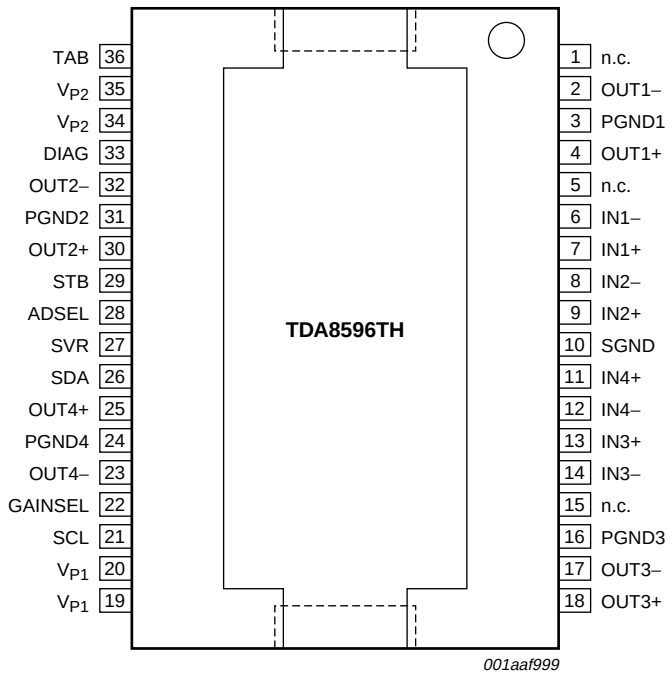


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
OUT1–	2	channel 1 negative output
PGND1	3	power ground channel 1
OUT1+	4	channel 1 positive output
n.c.	5	not connected
IN1–	6	channel 1 negative input
IN1+	7	channel 1 positive input
IN2–	8	channel 2 negative input
IN2+	9	channel 2 positive input
SGND	10	signal ground
IN4+	11	channel 4 positive input
IN4–	12	channel 4 negative input
IN3+	13	channel 3 positive input
IN3–	14	channel 3 negative input
n.c.	15	not connected

Table 3. Pin description *…continued*

Symbol	Pin	Description
PGND3	16	power ground channel 3
OUT3–	17	channel 3 negative output
OUT3+	18	channel 3 positive output
V_{P1}	19 and 20	supply voltage 1
SCL	21	I²C-bus clock input
GAINSEL	22	gain select input (legacy mode only)
OUT4–	23	channel 4 negative output
PGND4	24	power ground channel 4
OUT4+	25	channel 4 positive output
SDA	26	I²C-bus data input/output
SVR	27	half supply filter capacitor
ADSEL	28	I²C-bus address select
STB	29	standby (I²C-bus mode) or mode pin (legacy mode); programmable second clip indicator
OUT2+	30	channel 2 positive output
PGND2	31	power ground channel 2
OUT2–	32	channel 2 negative output
DIAG	33	diagnostic/clip detection output
V_{P2}	34 and 35	supply voltage 2
TAB	36	heatsink connection; must be connected to ground

7. Functional description

The TDA8596 is a quad BTL audio power amplifier with symmetrical inputs, made in BCDMOS technology. It contains four independent amplifier channels in BTL configuration with complementary (PMOST/NMOST) output stages (see Figure 1). The status of each amplifier channel (output offset, connected load, short circuit condition at output pins) can be read out separately via the I²C-bus. The TDA8596 is protected against overvoltage on the supply pins, short circuits at the output pins, overheating and loss-of-ground or loss-of-V_P conditions.

The temperature pre-warning level and the clip detection levels can be programmed via the I²C-bus. Further, the information that will be available on the diagnostic pins (i.e. DIAG or STB) can be programmed. Three different I²C-bus addresses can be selected by connecting a resistor to the ADSEL pin. In case the ADSEL pin is shorted to ground, the TDA8596 operates in legacy mode. In this mode no I²C-bus is needed and the STB pin will change from a two level pin (Standby mode and Operating mode) to a three level pin (Standby, Mute operating and Normal operating mode).

7.1 Output stage

The output stage of each amplifier channel consists of two PMOS power transistors and two NMOS transistors in BTL configuration. The TDA8596 is manufactured in a BCDMOS process on an isolated substrate Silicon On Insulator (SOI). Due to the absence of a doped (bulk) substrate, this process is insensitive to latch-up induced by substrate coupled parasitic paths.

7.2 Gain selection

The gain of the TDA8596 can be programmed at 16 dB (line driver mode) or 26 dB (Normal operating mode). This can be done either in I²C-bus mode by means of a bus command or in legacy mode by using the GAINSEL pin. To allow this, the device must first be put in legacy mode by connecting the ADSEL pin to ground. In case the GAINSEL pin is connected to ground the 26 dB mode is selected. By leaving the GAINSEL pin open the 16 dB mode is selected. The GAINSEL pin will be ignored in I²C-bus mode.

7.3 Distortion (clip-) detection

If the output of an amplifier channel starts clipping to either the supply voltage or to ground the output signal will become distorted. When the Total Harmonic Distortion (THD) per channel exceeds a preselected threshold (2 %, 5 % or 10 %), one of the two diagnostic pins (DIAG or STB) will be pulled LOW. The clip information of each channel can be directed separately to one specific diagnostic pin. This way, it is possible to distinguish between clipping on the front or rear channels. Redirection of temperature and load information to the diagnostic pins can be disabled to allow only the clip information to be present on these pins. In this mode, the temperature and load information is still available but can only be read out through the I²C-bus.

Note: during mute-to-on or on-to-mute transitions, the clip detection may be activated even when no output clipping occurs.

7.4 Output protection and short circuit operation

When a short circuit to ground, to V_P or across the load occurs, the concerning amplifier channel will switch off. After 16 ms of non-operation it will switch on again. If the short circuit condition is still present the amplifier channel will again return to 16 ms of non-operation. The 16 ms cycle will reduce the dissipation.

The other amplifier channels (without short circuit condition) will retain functionality. To prevent audible distortion, the amplifier channel with the short circuit condition can be disabled via the I²C-bus.

In case the diagnostic pin is selected for load fault information (IB2[D4] = 0), it will be pulled LOW. Via the I²C-bus it can be read out which channel is shorted by what type of short circuit (to ground, to V_P or across the load).

In order to detect a shorted load, a signal should be applied to the inputs of the amplifier. A shorted load is only detected when the output current level on the related output crosses the defined Safe Operating ARea (SOAR) protection threshold.

7.4.1 SOAR protection

The output transistors are protected by a Safe Operating ARea (SOAR) protection. The TDA8596 has a two-stage SOAR protection:

- If the differential output voltage across the load (V_o) is less than 1 V, and the current through the load (I_L) exceeds 4 A, the amplifier channel will be switched off during 16 ms. To prevent spurious switch-off events (which may occur for instance in case of inductive loads or very high input signals), the fault condition (V_o < 1 V and I_L > 4 A) must exist for more than 300 µs.
- If the differential output voltage across the load (V_o) is more than 1 V, and the current through the load (I_L) exceeds 8 A, the amplifier channel will be switched off during 16 ms.

7.4.2 Speaker protection

To prevent damage of the speaker when one side of the speaker is connected to ground, a missing-current protection is implemented. When the current in the high side power transistor of one amplifier channel is not equal to the current through the corresponding low side power transistor, a fault condition is assumed and the concerning channel will be switched off. The boundary conditions for the activation of this speaker protection are:

- V_o < 1.55 V and $I_{missing}$ > 1 A for 80 µs
- V_o > 1.55 V and $I_{missing}$ > 3 A for 80 µs

7.5 Standby and mute operation

The functionality of the STB pin depends on the mode of operation of the device (i.e. legacy- or I²C-bus mode).

7.5.1 I²C-bus mode

When the STB pin is LOW (< 1 V), the device is in standby condition. The I²C-bus lines will not be loaded and the quiescent current will be low. When the STB pin is switched HIGH (> 2.5 V) the TDA8596 switches to operating condition and performs a Power-On Reset (POR). This will cause the DIAG pin to be pulled LOW. The TDA8596 will start-up when bit D0 of instruction byte IB1 is set. Bit D0 will also reset the ‘power-on reset occurred’ bit (DB2[D7]) and releases the DIAG pin.

The soft- and fast-mute functions can be activated by means of I²C-bus instructions. The soft mute can be activated independently for the front (1 and 3) and rear (2 and 4) channels, and mutes the audio in 20 ms. The fast mute is activated for all channels simultaneously and mutes the audio in 0.1 ms. Releasing the mute will always occur via a soft mute and will take 20 ms.

When the STB pin is switched LOW and the amplifier is in Operating mode, the fast mute will be activated prior to shut-down. This enables the option to fast mute the amplifier by means of the STB pin in case of, for instance an engine start, thus preventing audible pop noise.

7.5.2 Legacy mode (pin ADSEL connected to ground)

In legacy mode, the function of the STB pin changes into a three level (standby, mute and operating) enable pin and the amplifier will directly start-up when the STB pin is put into Mute or Normal operating mode. Mute operation is controlled through an internal timer

(20 ms) to minimize mute-to-operating pops. When the STB pins directly switched from Normal operating to Standby mode, the fast mute (mutes in 0.1 ms) will be activated prior to shut-down.

7.6 Start-up and shut-down sequence

To prevent the amplifier from producing switch-on and switch-off pop noise, the capacitor on the SVR pin is used for smooth start-up and shut-down sequences. Larger capacitors will lead to longer (smoother) start-up and shut-down sequences. Initially the amplifier outputs are charged to Half Supply Voltage (HVP) minus 1.4 V in mute condition. This is independent of the I²C-bus mute settings in I²C-bus mode or the pin STB voltage in legacy mode. The remaining 1.4 V before the outputs reach HVP, is used for mute release in case the I²C-bus bits (IB2[D2:D0] = 000) have been programmed to mute-off (or V_{STB} > 6.5 V in legacy mode). In case the I²C-bus bits have been programmed to maintain mute condition (IB2[D2:D0] = 111) (or 2.5 V < V_{STB} < 6.5 V in legacy mode) the amplifier will stay in mute.

When the STB pin is switched LOW (< 1 V), a fast mute is performed prior to discharging the capacitor on pin SVR. With a capacitor of 22 µF the device goes into Standby mode (low quiescent current) within 1 s after switching STB to LOW (see also Figure 3 and Figure 6).

Start-up and shut-down pop noise can be further reduced by activating the low pop mode. When this mode is selected (IB2[D3] = 0), the output voltage rising slope will decrease (resulting in a longer start-up time).

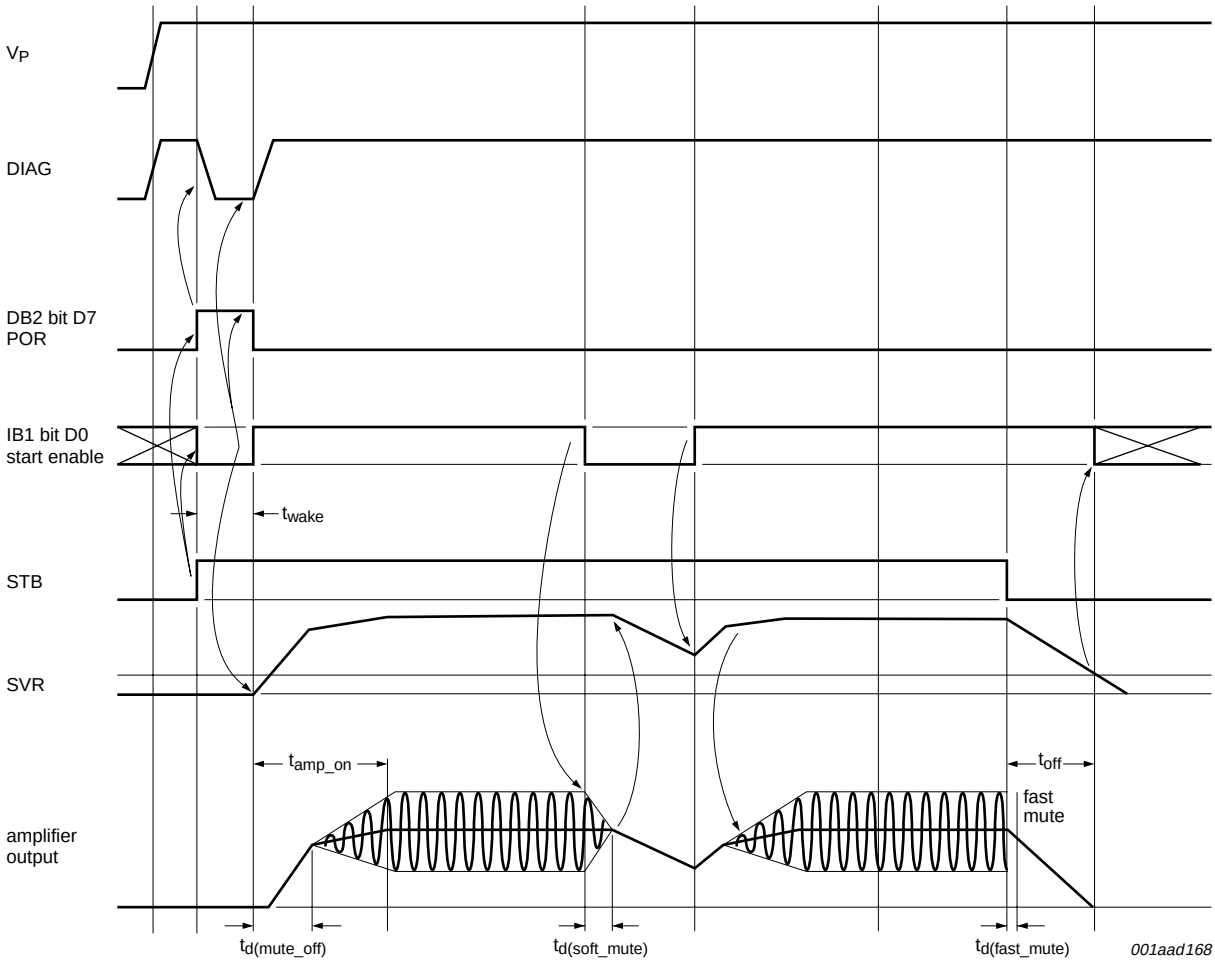


Fig 3. Start-up and shut-down timing in I²C-bus mode

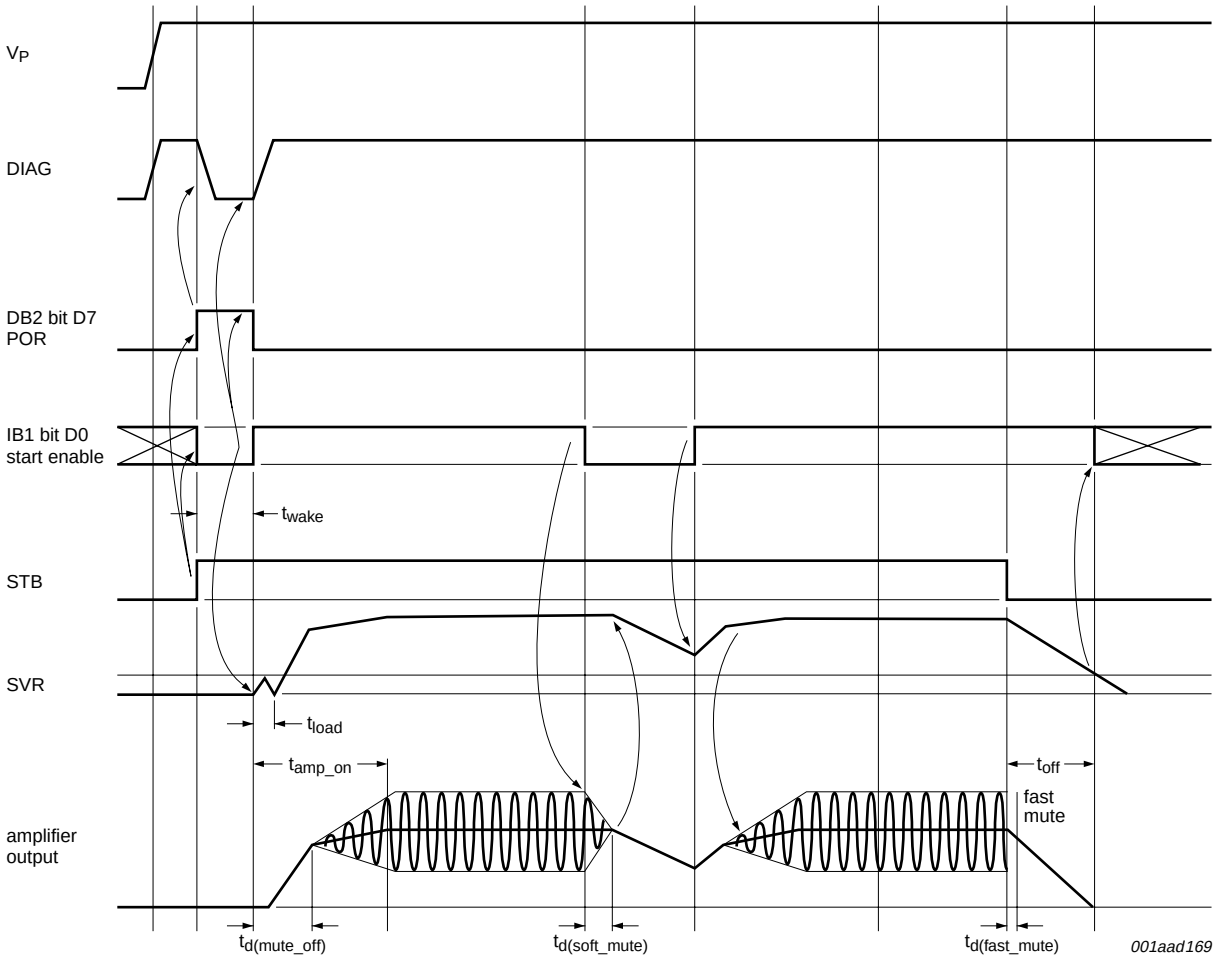


Fig 4. Start-up and shut-down timing with DC load active in I²C-bus mode

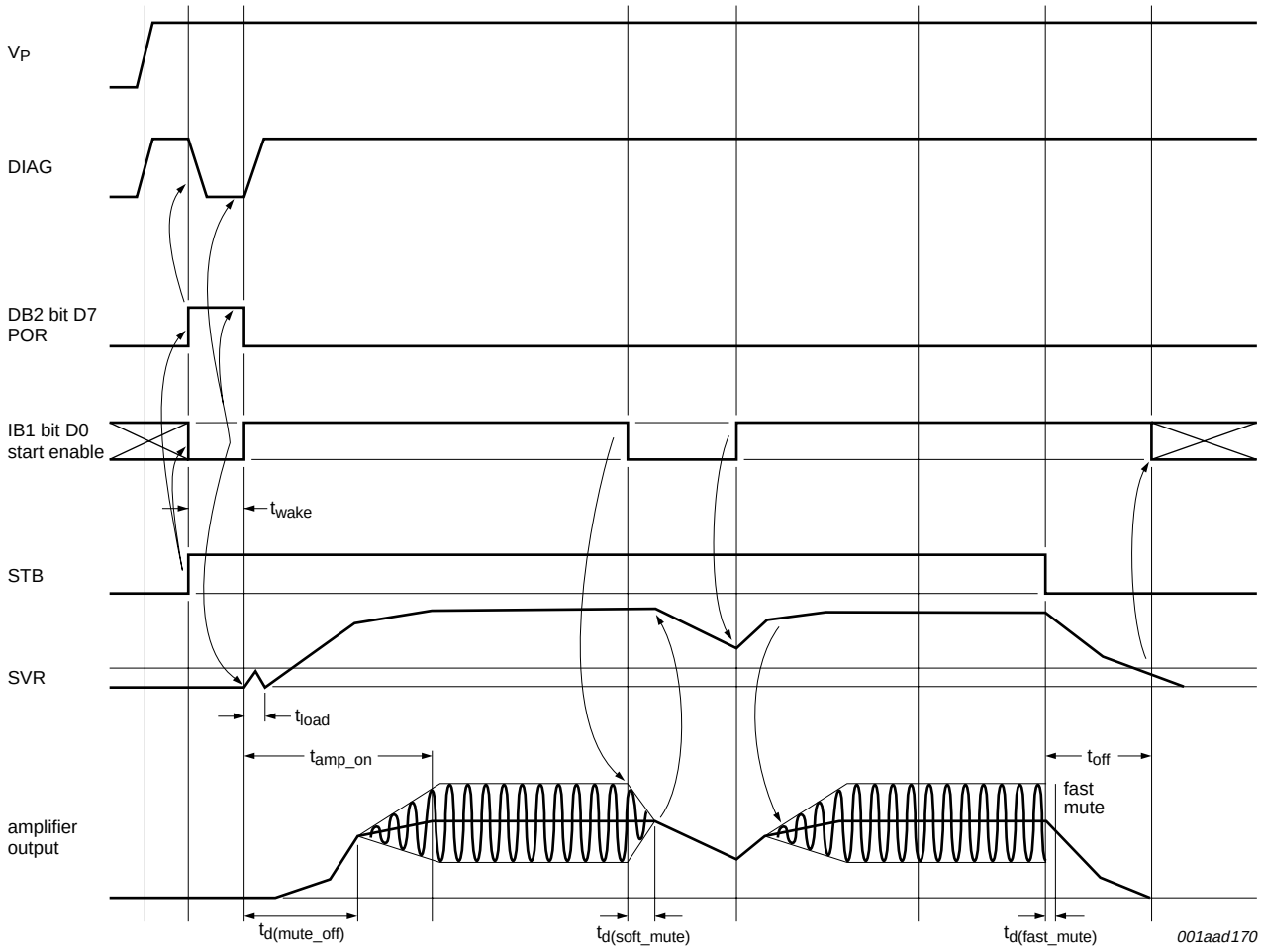


Fig 5. Start-up and shut-down timing with low pop and DC load activated

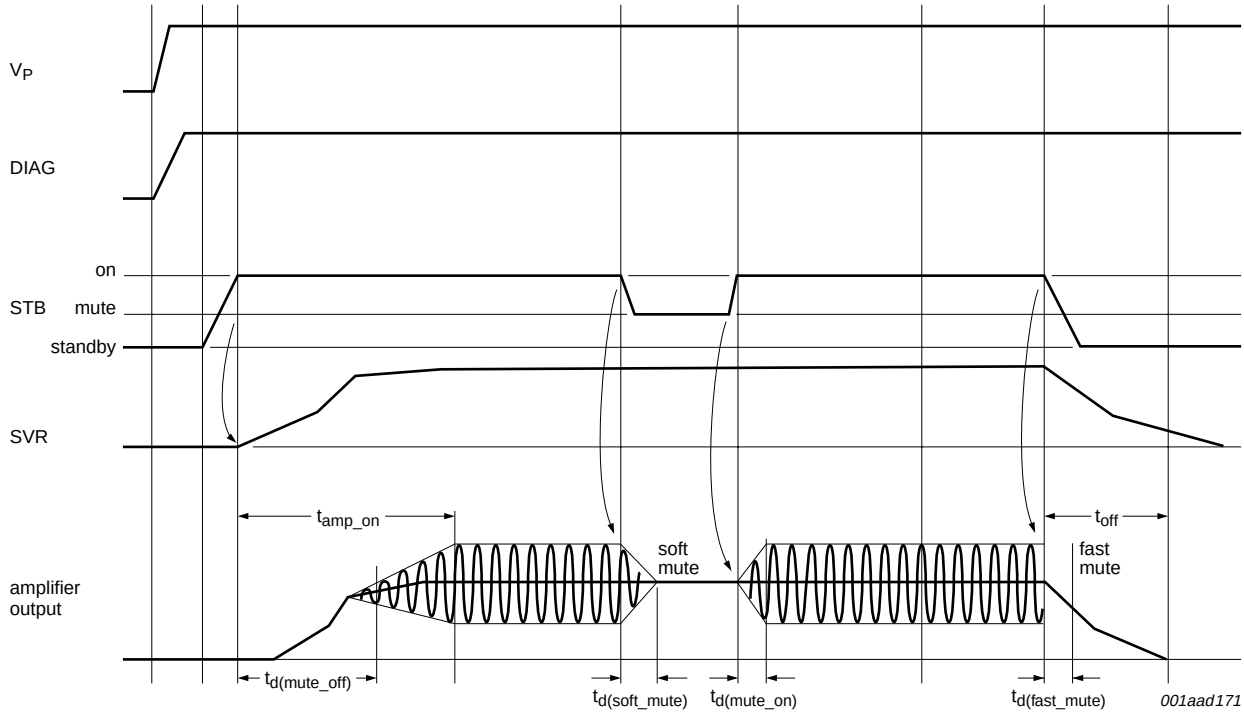


Fig 6. Start-up and shut-down timing in legacy mode

7.7 Power-on reset and supply voltage spikes

If the supply voltage drops below 5 V in I²C-bus mode (see Figure 8 and 9), the content of the I²C-bus latches cannot be guaranteed and a power-on reset will be performed. This will cause all latches to be reset, the amplifier to be switched off and the DIAG pin to be pulled LOW, indicating that a power-on reset has occurred (see DB2[D7]). When bit IB1[D0] is set, the power-on flag is reset, the DIAG pin is released and the amplifier will start-up.

In legacy mode a supply voltage drop below 5 V will switch off the amplifier without pulling the DIAG pin LOW.

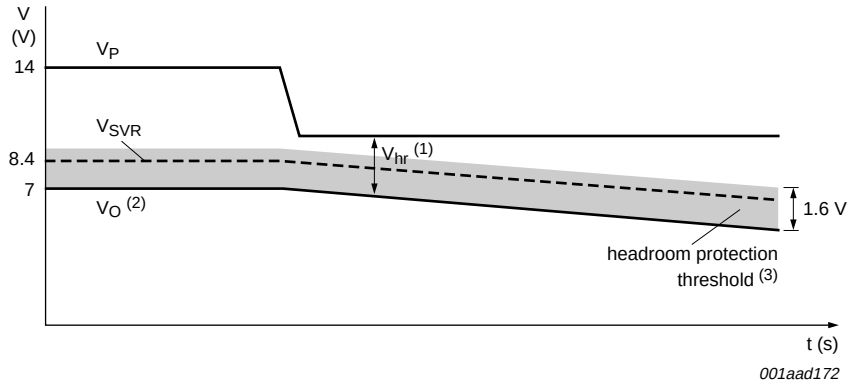
7.8 Engine start and low voltage operation

In steady state, the DC output voltage of an amplifier channel V_O equals half the supply voltage (HVP). This voltage is related to the voltage on the SVR pin (refer to Figure 7: $V_O = V_{SVR} - 1.4$ V). An external capacitor has been connected to the SVR pin to suppress coupling of power supply ripple to the amplifier outputs.

The headroom voltage V_{hr} is defined as the difference between the supply voltage V_P and the DC output voltage V_O, i.e. $V_{hr} = V_P - V_O$ (refer to Figure 7). If the supply voltage drops, e.g. during an engine start, the outputs will follow slowly due to the capacitor on pin SVR. However, if the headroom voltage V_{hr} drops below the headroom protection threshold of 1.6 V, the headroom protection will be activated to prevent pop noise at the output. This protection will first activate the fast mute and will subsequently discharge the capacitor on pin SVR to generate more headroom for the amplifier (refer to Figure 8 and 9).

When the SVR capacitor has discharged, the amplifier will only start-up again when the supply voltage V_P increases above the low V_P mute threshold, typically 7.5 V. Below this threshold, the outputs of the amplifier remain low. In I²C-bus mode, a supply voltage drop below $V_{P(reset)}$, typically 5 V will result in setting bit DB2[D7]. In this condition the amplifier will wait for an I²C-bus command in order to start-up.

The TDA8596 prevents internally induced output pops during engine start. In order to prevent pops on the output caused by the application (e.g. due to the tuner supply going out of regulation), the STB pin can be pulled LOW when an engine start is detected. The STB pin will activate the fast mute within 0.1 ms and consequently all disturbances at the amplifier inputs will be suppressed.

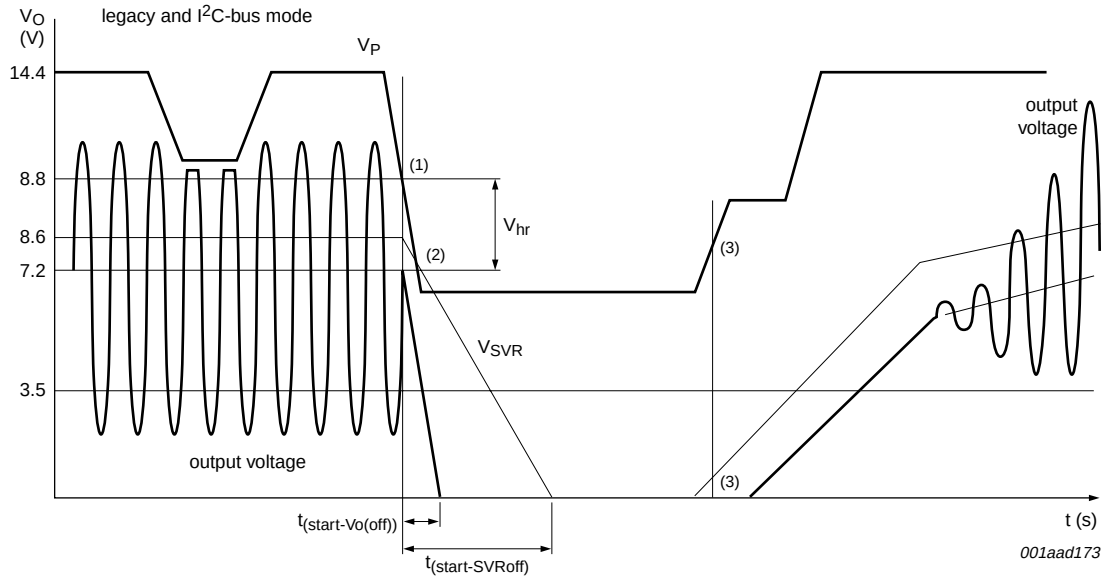


(1) Headroom voltage $V_{hr} = V_P - V_O$.

(2) Steady state output voltage $V_O = V_{SVR} - 1.4$ V.

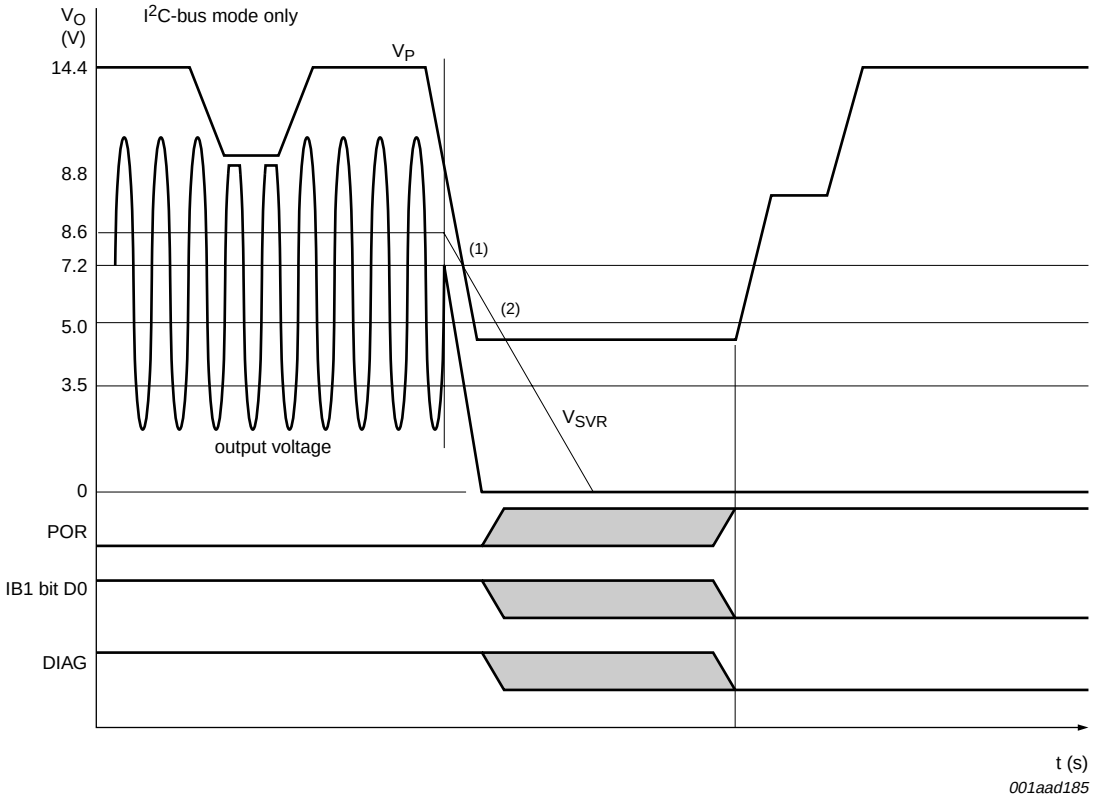
(3) Headroom protection threshold = $V_O + 1.6$ V.

Fig 7. Low-headroom protection



(1) Headroom protection activated:
a) Fast mute.
b) Discharge of SVR.
(2) Low V_P mute activated.
(3) Low V_P mute released.

Fig 8. Low V_P behavior; legacy and I²C-bus modes



(1) Low V_P mute activated.

(2) V_{POR}: V_P level at which POR is activated.

Fig 9. Low V_P behavior; I²C-bus mode only

7.9 Overvoltage and load dump protection

When the supply voltage V_P exceeds 22 V, all amplifier output stages will be switched to high-impedance. The TDA8596 is protected against load dump transients up to 50 V.

7.10 Thermal pre-warning and thermal protection

If the average junction temperature reaches the (I²C-bus programmable) pre-warning level, a thermal pre-warning will be generated, which can be read out on the I²C-bus. If the TDA8596 is programmed to send thermal warning information to the DIAG pin, the DIAG pin will be pulled LOW. The default thermal pre-warning detection level (IB3[D4] = 0) is 145 °C typical. In case IB3[D4] = 1, the detection level is modified to 122 °C typical.

In legacy mode the thermal pre-warning level is fixed at 145 °C typical.

If the junction temperature increases further, the temperature controlled gain reduction will be activated for all four channels to reduce the output power (see Figure 10). If this still does not reduce the average junction temperature, all channels will be switched off at the absolute maximum temperature T_{off}, typical 175 °C.

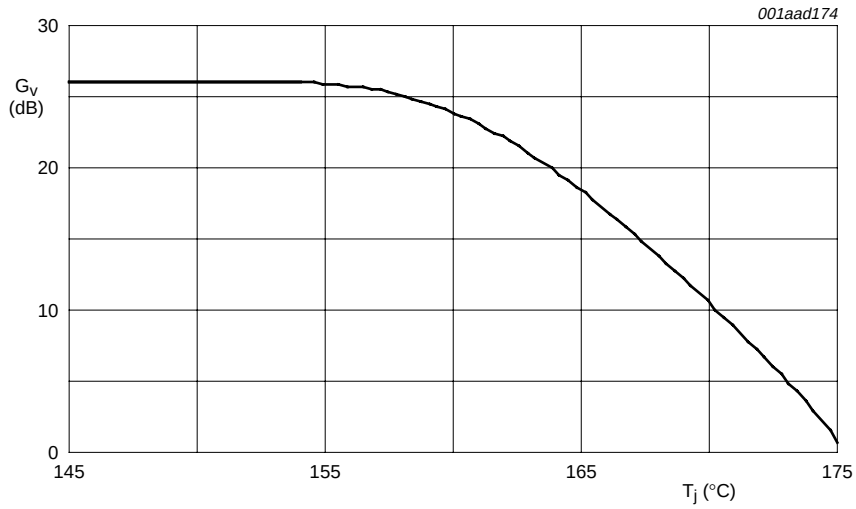


Fig 10. Temperature controlled amplifier gain

7.11 Diagnostics

Diagnostic information can be read via the I²C-bus and it can also be made available on the DIAG pin or STB pin. The information on the DIAG pin is partly fixed, i.e. power-on reset occurred and low or high battery events. Through I²C-bus commands selectable information (i.e. load faults, temperature alarms and clip detection) can be made available. This information will be directed to the DIAG pin through a logical OR function. In case of any of the above mentioned failures, the DIAG pin will remain LOW so the microcontroller is triggered to read out the failure information via the I²C-bus (the DIAG pin can be used as microcontroller interrupt to minimize I²C-bus traffic). As soon as the failure is removed, the DIAG pin will be released.

The STB pin can be configured as a second clip detection pin. The clip detection level is equal for all channels. It is possible to redirect the clip information of all separate channels to each of the two diagnostic pins DIAG or STB. This option can be used to distinguish between for instance clipping on the front and rear side channels (i.e. by redirecting the front channels to one diagnostic output and the rear channels to the second diagnostic output).

Table 4 shows the diagnostic options for the DIAG pin and STB pin for both I²C-bus and legacy mode:

Table 4. Diagnostic information per pin for various modes

Diagnostic information	I²C-bus mode		Legacy mode
	Pin DIAG	Pin STB	Pin DIAG
Power-on reset	after power-on reset; pin DIAG will remain LOW until amplifier has been started	no	no
Low battery	yes	no	yes
Clip detection	can be enabled per channel	can be enabled per channel	yes; fixed level for all channels on 2 %

Table 4. Diagnostic information per pin for various modes *…continued*

Diagnostic information	I²C-bus mode		Legacy mode
	Pin DIAG	Pin STB	Pin DIAG
Temperature pre-warning	can be enabled	no	yes; pre-warning level is 145 °C
Short	can be enabled	no	yes
Speaker protection (missing current)	can be enabled	no	yes
Offset detection	no	no	no
Load detection	no	no	no
Overvoltage	yes	no	yes

7.12 Offset detection

Offset detection can be performed either with or without input signal (for instance when the DSP is in mute after a start-up). Assume the amplifier is in I²C-bus mode. When an I²C-bus read of the output offset is performed the DBx[D2] latch will be set. When the amplifier BTL output voltage crosses the 1.55 V window threshold within 1 s after a read is performed, the DBx[D2] latch is reset and setting is disabled. After a certain delay, the next read can be performed.

Example: in case the offset bits are still set when a successive read is performed more than 1 s after the previous read, the output signal has not been within the offset window thresholds for at least 1 s. This could either indicate an output signal with a frequency below 1 Hz or the presence of an output offset above 1.55 V (see Figure 11).

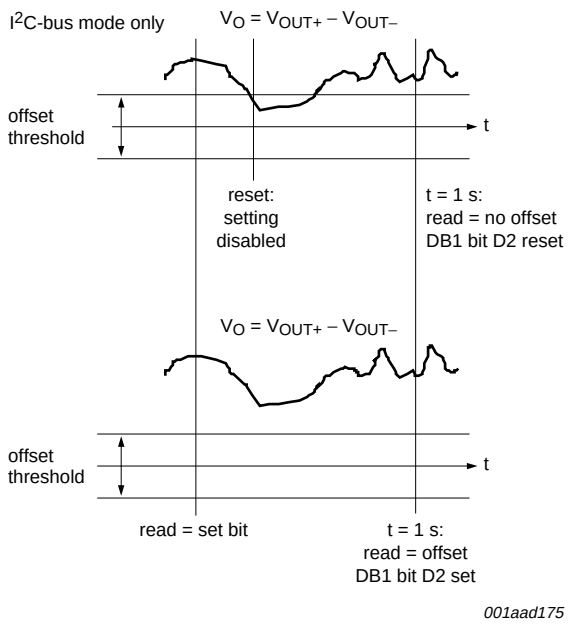


Fig 11. Offset detection

7.13 DC load detection

When the DC load detection is enabled (IB1[D1] = 1), a DC offset is slowly applied at the outputs of the amplifiers during the start-up sequence (see Figure 4 and Figure 5) and the load currents as a result of the applied offset are measured. Based on this measurement the load impedance can be determined to differentiate between normal, line driver and no load (see Figure 12).

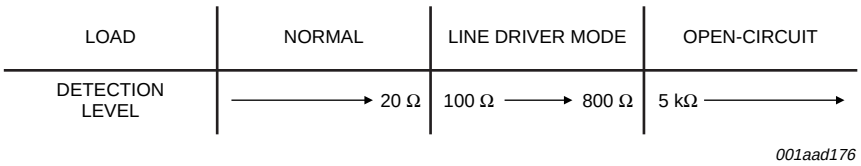


Fig 12. DC load detection levels

When the amplifier is used in line driver mode and the external booster has an input impedance between 100 Ω and 800 Ω (DC-coupled), the DC load bits will be set at DBx[D5:D4] = 10 independent of the selected gain setting (see Table 5).

Table 5. DC load detection translation table

DC load bits		Load indication[1]
DBx[D5]	DBx[D4]	
0	0	normal load
1	0	line driver load
1	1	open load
0	1	not valid

[1] Only when IB1[D2] = 0.

By reading the I²C-bus bits the microprocessor can determine after the start-up of the amplifier whether a speaker or an external booster is connected and initiate the proper selection of the amplifier gain, i.e. 26 dB for normal mode or 16 dB for line driver mode. Gain selection will occur without audible pop noise when the amplifier is in mute.

The DC load bit DBx[D4] is shared with the AC load detection. This implies that Table 5 is only valid when AC load detection is disabled (IB1[D2] = 0). When the AC load detection is enabled (IB1[D2] = 1) the bits DBx[D4] will show the result of the AC load detection. After disabling the AC load detection data bit DBx[D4] will show the result of the DC load measurement, which was stored during the AC load measurement.

7.14 AC load detection

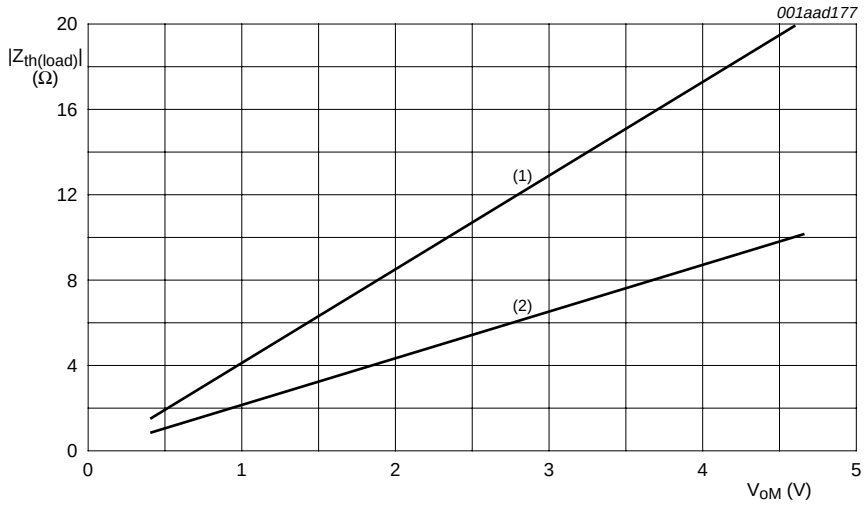
When AC load detection is enabled (IB1[D2] = 1), AC coupled speakers (e.g. tweeters) can be detected during the assembly process. The detection is performed by means of applying an audible input sine wave (e.g. 19 kHz) to the inputs of the amplifier. The AC current into the load is measured with a 460 mA peak current detector to detect the presence of an AC load. In order to prevent spurious AC load detection (e.g. due to amplifier on/off switching), the AC load detection bit will only be set when the peak current threshold is triggered at least three times. Besides the 460 mA peak current threshold, a secondary threshold level at 230 mA is present. In case this level is not triggered, a high ohmic DC load (e.g. line driver) is assumed (also refer to Figure 13).

Example: at an AC output voltage of 2 V peak the total impedance must be less than 4 Ω to detect an AC coupled load or above 9 Ω to guarantee the detection of a DC load. Refer to Table 6 for the interpretation AC load detection bits.

Table 6. AC load detection translation table

Normal DC load bit DBx[D5]	Line driver DC load bit DBx[D4]	Load indication
Don't care	0	no AC load detected
Don't care	1	AC load detected

The AC load detection can only be performed when the amplifier has completed its start-up sequence. Consequently it will not conflict with the DC load detection.



(1) I_{oM} < 230 mA (no load detection level).

(2) I_{oM} > 460 mA (load detection level).

Fig 13. AC load impedance versus output signal

7.15 I²C-bus diagnostic bits read out

The diagnostic information of the amplifier can be read out via the I²C-bus. The I²C-bus data bits are set in case a failure event occurs and are not reset until an I²C-bus read command is given. This implies that even when the failure mode is removed before reading out the I²C-bus, the microcontroller will still be able to read out what kind of failure has occurred. A consequence of this procedure is that during the I²C-bus read cycle old information is read. When actual information is required, it is recommended to perform two successive read actions.

The DIAG pin will give actual diagnostic information (when selected), however it does not distinguish between the various failure modes. The DIAG pin can be used to trigger an I²C-bus read out of the data bits to retrieve actual diagnostic information. When a failure is no longer present, the DIAG pin will be released instantly, independently of the I²C-bus latches.

8. I²C-bus specification

Table 7. TDA8596 ADDRESS with hardware address select

Pin ADSEL	A6	A5	A4	A3	A2	A1	A0	R/W
Open	1	1	0	1	1	0	0	0 = write to TDA8596
								1 = read from TDA8596
51 kΩ to ground	1	1	0	1	1	0	1	0 = write to TDA8596
								1 = read from TDA8596
10 kΩ to ground	1	1	0	1	1	1	1	0 = write to TDA8596
								1 = read from TDA8596
Ground	no I²C-bus; legacy mode							

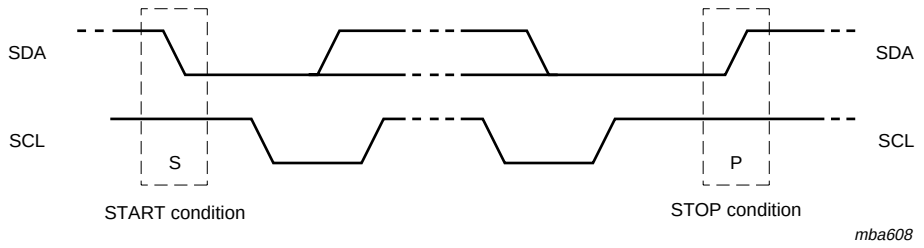


Fig 14. START and STOP conditions

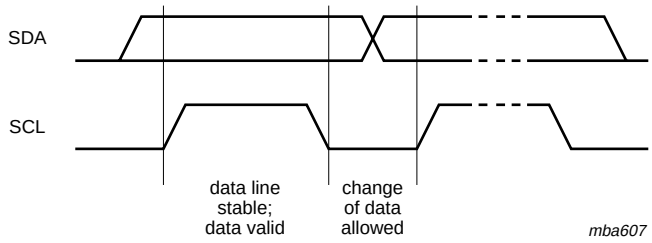


Fig 15. Bit transfer

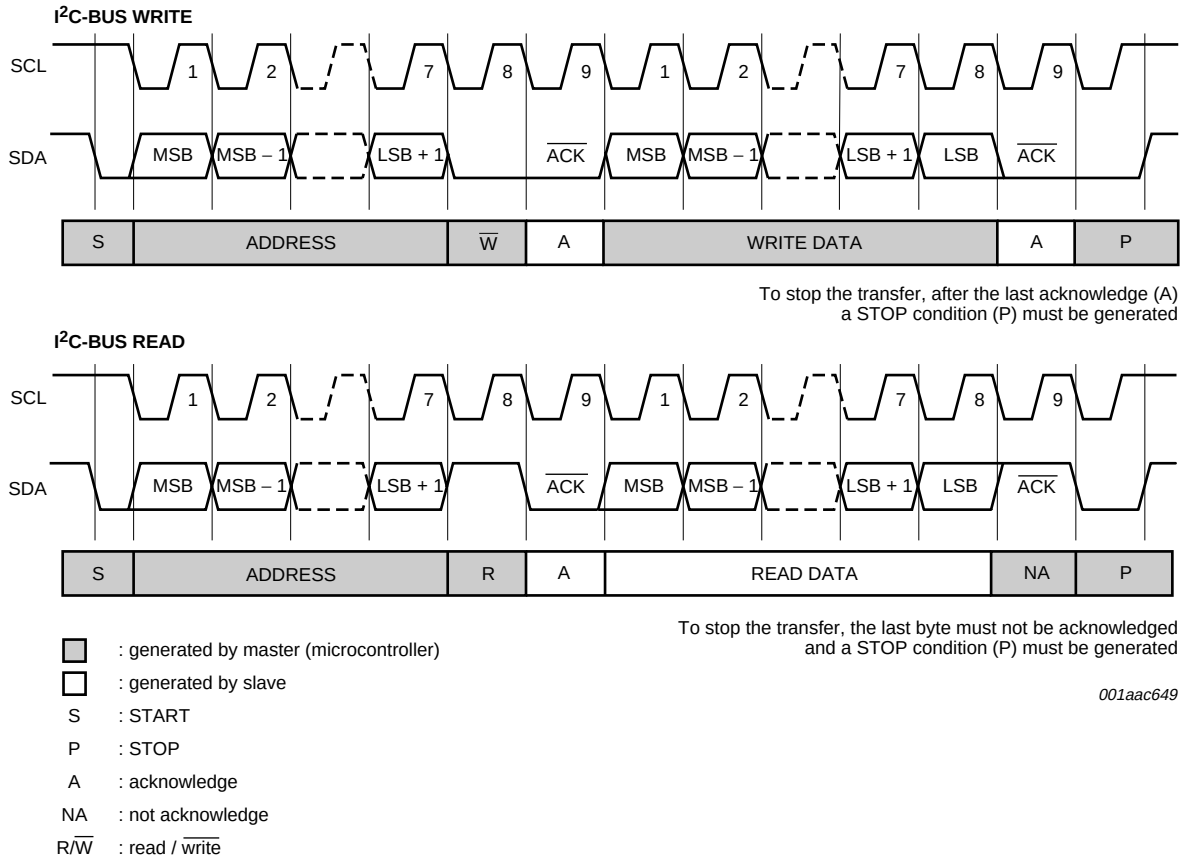


Fig 16. I²C-bus read and write modes

8.1 Instruction bytes

I²C-bus mode:

- If R/$\overline{W}$ bit = 0, the TDA8596 expects 3 instruction bytes: IB1, IB2 and IB3
- After a power-on reset, all instruction bits are set to logic 0

Legacy mode:

- The settings are equal to the condition with all instruction bits set to logic 0 (see Table 8), with the exception of IB1[D0] bit that is ignored in legacy mode.

Table 8. Instruction byte IB1

Bit	Description
D7	don't care
D6	channel 3 clip information on DIAG or STB pin
	0 = clip information on DIAG pin
	1 = clip information on STB pin
D5	channel 1 clip information on DIAG or STB pin
	0 = clip information on DIAG pin
	1 = clip information on STB pin

Table 8. Instruction byte IB1 *…continued*

Bit	Description
D4	channel 4 clip information on DIAG or STB pin
	0 = clip information on DIAG pin
	1 = clip information on STB pin
D3	channel 2 clip information on DIAG or STB pin
	0 = clip information on DIAG pin
	1 = clip information on STB pin
D2	AC load detection enable
	0 = AC load detection disabled
	1 = AC load detection enabled; DBx[D4] bits not available for DC load detection
D1	DC load detection enable
	0 = DC load detection disabled
	1 = DC load will be detected
D0	amplifier start enable; (clear power-on reset flag, DB2[D7])
	0 = amplifier not enabled, DIAG pin will remain LOW
	1 = amplifier will start-up, power-on occurred (DB2[D7]) will be reset and DIAG pin will be released

Table 9. Instruction byte IB2

Bit	Description
D7 and D6	clip detection level
	00 = clip detection level 2 %
	01 = clip detection level 5 %
	10 = clip detection level 10 %
	11 = clip detection level disabled
D5	temperature information on DIAG pin
	0 = temperature information on DIAG pin
	1 = no temperature information on DIAG pin
D4	load fault information (shorts, missing current) on DIAG pin
	0 = fault information on DIAG pin
	1 = no fault information on DIAG pin
D3	low pop (slow start) enable
	0 = low pop enabled
	1 = low pop disabled
D2	soft mute channel 1 and channel 3 (mute delay 20 ms)
	0 = no mute
	1 = mute
D1	soft mute channel 2 and channel 4 (mute delay 20 ms)
	0 = no mute
	1 = mute

Table 9. Instruction byte IB2 *…continued*

Bit	Description
D0	fast mute all amplifier channels (mute delay 100 μs)
	0 = no mute
	1 = mute

Table 10. Instruction byte IB3

Bit	Description
D7	don't care
D6	amplifier channel 1 and channel 3 gain select
	0 = 26 dB
	1 = 16 dB
D5	amplifier channel 2 and channel 4 gain select
	0 = 26 dB
	1 = 16 dB
D4	temperature pre-warning level
	0 = warning level on 145 °C
	1 = warning level on 122 °C
D3	disable channel 3
	0 = channel 3 enabled
	1 = channel 3 disabled
D2	disable channel 1
	0 = channel 1 enabled
	1 = channel 1 disabled
D1	disable channel 4
	0 = channel 4 enabled
	1 = channel 4 disabled
D0	disable channel 2
	0 = channel 2 enabled
	1 = channel 2 disabled

8.2 Data bytes

I²C-bus mode:

- If R/$\overline{W}$ = 1, the TDA8596 will send four data bytes to the microprocessor: DB1, DB2, DB3, and DB4
- All bits are latched
- All bits are reset after a read operation except D4 and D5. D2 is set after a read operation, refer to the offset detection described in Section 7.12
- For explanation of AC and DC load detection bits, refer to Section 7.13 and Section 7.14

Table 11. Data byte DB1

Bit	Description
D7	temperature pre-warning
	0 = no warning
	1 = junction temperature too high
D6	speaker fault channel 2 (missing current)
	0 = no missing current
	1 = missing current
D5 and D4	channel 2 DC load or AC load detection
	if bit IB1[D2] = 1, AC load detection is enabled, bit D5 and bit D4 are available for AC load detection
	00 = no AC load
	01 = AC load detected
	10 = no AC load
	11 = AC load detected
	if bit IB1[D2] = 0, DC load detection is enabled, bits D5 and bit D4 are available for DC load detection
	00 = normal load
	01 = not valid
	10 = line driver load
	11 = open load
D3	channel 2 shorted load
	0 = not shorted load
	1 = shorted load
D2	channel 2 output offset
	0 = no output offset
	1 = output offset
D1	channel 2 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 2 short to ground
	0 = no short to ground
	1 = short to ground

Table 12. Data byte DB2

Bit	Description
D7	power-on reset occurred/amplifier status
	0 = amplifier on
	1 = power-on reset has occurred; amplifier off
D6	speaker fault channel 4 (missing current)
	0 = no missing current
	1 = missing current

Table 12. Data byte DB2 *…continued*

Bit	Description
D5 and D4	channel 4 DC load or AC load detection
	if bit IB1[D2] = 1, AC load detection is enabled, bit D5 and bit D4 are available for AC load detection
	00 = no AC load
	01 = AC load detected
	10 = no AC load
	11 = AC load detected
	if bit IB1[D2] = 0, DC load detection is enabled, bits D5 and bit D4 are available for DC load detection
	00 = normal load
	01 = not valid
	10 = line driver load
	11 = open load
D3	channel 4 shorted load
	0 = not shorted load
	1 = shorted load
D2	channel 4 output offset
	0 = no output offset
	1 = output offset
D1	channel 4 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 4 short to ground
	0 = no short to ground
	1 = short to ground

Table 13. Data byte DB3

Bit	Description
D7	maximum temperature protection
	0 = no protection
	1 = maximum temperature protection
D6	speaker fault channel 1 (missing current)
	0 = no missing current
	1 = missing current

Table 13. Data byte DB3 *…continued*

Bit	Description
D5 and D4	channel 1 DC load or AC load detection
	if bit IB1[D2] = 1, AC load detection is enabled, bit D5 and bit D4 are available for AC load detection
	00 = no AC load
	01 = AC load detected
	10 = no AC load
	11 = AC load detected
	if bit IB1[D2] = 0, DC load detection is enabled, bits D5 and bit D4 are available for DC load detection
	00 = normal load
	01 = not valid
	10 = line driver load
	11 = open load
D3	channel 1 shorted load
	0 = not shorted load
	1 = shorted load
D2	channel 1 output offset
	0 = no output offset
	1 = output offset
D1	channel 1 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 1 short to ground
	0 = no short to ground
	1 = short to ground

Table 14. Data byte DB4

Bit	Description
D7	reserved
D6	speaker fault channel 3 (missing current)
	0 = no missing current
	1 = missing current

Table 14. Data byte DB4 *…continued*

Bit	Description
D5 and D4	channel 3 DC load or AC load detection
	if bit IB1[D2] = 1, AC load detection is enabled, bit D5 and bit D4 are available for AC load detection
	00 = no AC load
	01 = AC load detected
	10 = no AC load
	11 = AC load detected
	if bit IB1[D2] = 0, DC load detection is enabled, bits D5 and bit D4 are available for DC load detection
	00 = normal load
	01 = not valid
	10 = line driver load
	11 = open load
D3	channel 3 shorted load
	0 = not shorted load
	1 = shorted load
D2	channel 3 output offset
	0 = no output offset
	1 = output offset
D1	channel 3 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 3 short to ground
	0 = no short to ground
	1 = short to ground

9. Limiting values

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage	operating	-	18	V
		non operating	–1	+50	V
		load dump protection; duration 50 ms; rise time > 2.5 ms	-	50	V
$V_{P(r)}$	reverse supply voltage	10 minutes maximum	-	–2	V
I_{OSM}	non-repetitive peak output current		-	13	A
I_{ORM}	repetitive peak output current	repetitive	-	8	A
T_j	junction temperature		-	150	°C
T_{stg}	storage temperature		–55	+150	°C

Table 15. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		–40	+105	°C
$V_{(prot)}$	protection voltage	AC and DC short circuit voltage of output pins and across the load	-	V_P	V
V_x	voltage on pin x				
	SCL and SDA		0	6.5	V
	inputs, SVR and DIAG		0	13	V
	STB	[1]	0	24	V
P_{tot}	total power dissipation	T_{case} = 70 °C	-	80	W
V_{esd}	electrostatic discharge voltage	human body model; C = 100 pF; R_S = 1.5 kΩ	-	2000	V
		machine model; C = 200 pF; R_S = 10 Ω; L = 0.75 µH	-	200	V

[1] 10 kΩ series resistance if connected to V_P.

10. Thermal characteristics

Table 16. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		35	K/W

11. Characteristics

Table 17. Characteristics

Refer to test circuit (see Figure 29) at V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; R_S = 0 Ω; normal mode; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_{amb} = –40 °C to +105 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage behavior						
V_P	supply voltage	R_L = 4 Ω	8	14.4	18	V
		R_L = 2 Ω [1]	8	14.4	16	V
I_q	quiescent current	no load	-	270	400	mA
I_{stb}	standby current	V_{STB} = 0.4 V	-	4	15	µA
V_O	output voltage		6.7	7	7.2	V
$V_{P(low)(mute)}$	low supply voltage mute	with rising supply voltage	6.9	7.5	8	V
		with falling supply voltage	6.3	6.8	7.4	V
$\Delta V_{P(low)(mute)}$	low supply voltage mute hysteresis		0.1	0.7	1	V
$V_{th(ovp)}$	overvoltage protection threshold voltage		18	20	22	V
V_{hr}	headroom voltage	when headroom protection is activated; see Figure 7	1.1	1.6	2.0	V

Table 17. Characteristics *...continued*

Refer to test circuit (see Figure 29) at V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; R_S = 0 Ω; normal mode; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_{amb} = −40 °C to +105 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{POR}	power-on reset voltage	see Figure 9		4.1	5.0	5.8	V
$V_{O(offset)}$	output offset voltage	amplifier on		−95	0	+95	mV
		amplifier mute		−25	0	+25	mV
		line driver mode		−40	0	+40	mV
Mode select pin STB/second clip detection pin							
V_{STB}	voltage on pin STB	Standby mode					
		I²C-bus mode		-	-	1	V
		legacy mode (I²C-bus off)		-	-	1	V
		Mute operating mode					
		legacy mode (I²C-bus off)		2.5	-	4.5	V
		Operating mode					
		I²C-bus mode		2.5	-	V_P	V
		legacy mode (I²C-bus off)		6.5	-	V_P	V
		LOW voltage on pin STB when pulled down during clipping	[2]				
		I_{STB} = 150 µA		5.6	-	6.1	V
		I_{STB} = 500 µA		6.1	-	7.4	V
I_{STB}	current on pin STB	0 V < V_{STB} < 8.5 V					
		clip detection not active; I²C-bus mode		-	4	30	µA
		legacy mode		-	10	70	µA
Start-up, shut-down and mute timing							
t_{wake}	wake-up time	time after wake-up via STB pin before first I²C-bus transmission is recognized; see Figure 3		-	300	500	µs
$I_{LO(SVR)}$	output leakage current on pin SVR			-	-	10	µA

Table 17. Characteristics *...continued*

Refer to test circuit (see Figure 29) at V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; R_S = 0 Ω; normal mode; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_{amb} = −40 °C to +105 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(mute\_off)}$	mute off delay time	mute to 10 % of output signal; $I_{LO(SVR)}$ = 0 µA					
		I²C-bus mode (IB1[D0]); with $I_{LO(SVR)}$ = 10 µA → +15 ms; no DC load (IB1[D1] = 0); low pop disabled (IB2[D3] = 1); see Figure 3	[3]	295	465	795	ms
		I²C-bus mode (IB1[D0]); with $I_{LO(SVR)}$ = 10 µA → +20 ms; DC load active (IB1[D1] = 1); low pop disabled (IB2[D3] = 1); see Figure 4	[3]	500	640	940	ms
		I²C-bus mode (IB1[D0]); with $I_{LO(SVR)}$ = 10 µA → +20 ms; DC load active (IB1[D1] = 0); low pop enabled (IB2[D3] = 0); see Figure 5	[3]	640	830	1190	ms
		legacy mode; with $I_{LO(SVR)}$ = 10 µA → +20 ms; V_{STB} = 7 V; R_{ADSEL} = 0 Ω; see Figure 6	[3]	430	650	1030	ms
t_{amp_on}	amplifier on time	amplifier from mute to 90 % of output signal; $I_{LO(SVR)}$ = 0 µA					
		I²C-bus mode (IB1[D0]); with $I_{LO(SVR)}$ = 10 µA → +30 ms; no DC load (IB1[D1] = 0); low pop disabled (IB2[D3] = 1); see Figure 3	[3]	360	520	870	ms
		I²C-bus mode (IB1[D0]); with $I_{LO(SVR)}$ = 10 µA → +35 ms; DC load active (IB1[D1] = 1); low pop disabled (IB2[D3] = 1); see Figure 4	[3]	565	695	1015	ms
		I²C-bus mode (IB1[D0]); with $I_{LO(SVR)}$ = 10 µA → +30 ms; DC load active (IB1[D1] = 0); low pop enabled (IB2[D3] = 0); see Figure 5	[3]	710	890	1270	ms
		legacy mode; with $I_{LO(SVR)}$ = 10 µA → +20 ms; V_{STB} = 7 V; R_{ADSEL} = 0 Ω; see Figure 6	[3]	510	720	1120	ms
t_{off}	amplifier switch-off time	time to DC output voltage < 0.1 V; I²C-bus mode (IB1[D0]); $I_{LO(SVR)}$ = 0 µA					
		with $I_{LO(SVR)}$ = 10 µA → +0 ms; low pop enabled (IB2[D3] = 0); see Figure 4	[3]	120	245	530	ms
		with $I_{LO(SVR)}$ = 10 µA → +0 ms; low pop disabled (IB2[D3] = 1); see Figure 5	[3]	140	280	620	ms
$t_{d(mute\text{-}on)}$	mute to on delay time	from 10 % to 90 % of output signal; IB2[D1] = 1 to 0; V_i = 50 mV; see Figure 6		-	20	40	ms
$t_{d(soft\_mute)}$	soft mute delay time	from 10 % to 90 % of output signal; IB2[D1] = 0 to 1; V_i = 50 mV; see Figure 6		-	20	40	ms

Table 17. Characteristics *...continued*

Refer to test circuit (see Figure 29) at V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; R_S = 0 Ω; normal mode; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_{amb} = −40 °C to +105 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(fast\_mute)}$	fast mute delay time	from 10 % to 90 % of output signal; V_{STB} from 8 V to 1.3 V; V_i = 50 mV; see Figure 6	-	0.1	1	ms
$t_{(start\text{-}Vo(off))}$	engine start to output off time	V_P from 14.4 V to 7 V; V_o < 0.5 V; see Figure 8	-	0.1	1	ms
$t_{(start\text{-}SVRoff)}$	engine start to SVR off time	V_P from 14.4 V to 7 V; V_{SVR} < 2 V; see Figure 8	-	40	75	ms
I²C-bus interface[4]						
V_{IL}	LOW-level input voltage	pins SCL and SDA	-	-	1.5	V
V_{IH}	HIGH-level input voltage	pins SCL and SDA	2.3	-	5.5	V
V_{OL}	LOW-level output voltage	pin SDA; I_L = 5 mA	-	-	0.4	V
f_{SCL}	SCL clock frequency		-	400	-	kHz
R_{ADSEL}	resistance on pin ADSEL	I²C-bus address A[6:0] = 110 1100	155	-	-	kΩ
		I²C-bus address A[6:0] = 110 1101	42	51	57	kΩ
		I²C-bus address A[6:0] = 110 1111	7	10	15	kΩ
		legacy mode	-	-	0.5	kΩ
Gain select pin						
$R_{GAINSEL}$	resistance on pin GAINSEL	legacy mode (I²C-bus off)				
		26 dB gain; normal mode	-	-	5	kΩ
		16 dB gain; line driver mode	20	-	-	kΩ
Diagnostic						
$V_{OL(DIAG)}$	LOW-level output voltage on pin DIAG	fault condition; I_{DIAG} = 1 mA	-	-	0.3	V
$V_{O(offset\_det)}$	output voltage at offset detection		±1.3	±1.55	± 2.0	V
THD_{clip}	total harmonic distortion clip detection level	V_P > 10 V				
		IB2[D7:D6] = 10; level 10 %	5	10	16	%
		IB2[D7:D6] = 01; level 5 %	3	5	7	%
		IB2[D7:D6] = 00; level 2 %	1	2	3	%
ΔTHD_{clip}	total harmonic distortion clip detection level variation	between IB2[D7:D6] = 10 and IB2[D7:D6] = 01 (level between 10 % and 5 %)	1	4	8	%
		between IB2[D7:D6] = 01 and IB2[D7:D6] = 00 (level between 5 % and 2 %)	1	3.5	6	%
$T_{j(AV)(pwarn)}$	pre-warning average junction temperature	IB3[D4] = 0	135	145	155	°C
		IB3[D4] = 1	112	122	132	°C
$T_{j(AV)(G(-0.5dB))}$	average junction temperature for 0.5 dB gain reduction	V_i = 0.05 V	150	155	160	°C

Table 17. Characteristics *...continued*

Refer to test circuit (see Figure 29) at V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; R_S = 0 Ω; normal mode; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_{amb} = −40 °C to +105 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta T_{j(pw\text{-}G(-0.5dB))}$	prewarning to 0.5 dB gain reduction junction temperature difference		7	10	13	°C
$\Delta T_{j(G(-0.5dB)\text{-}of)}$	junction temperature difference between 0.5 dB gain reduction and off		10	15	20	°C
$\Delta G_{(th\_fold)}$	gain reduction of thermal foldback		-	20	-	dB
$Z_{th(load)}$	load detection threshold impedance	I²C-bus mode				
		normal load detection	-	-	20	Ω
		line driver load detection	100	-	800	Ω
$Z_{th(open)}$	open load detection threshold impedance	I²C-bus mode	5000	-	-	Ω
$I_{th(o)det(load)AC}$	AC load detection output threshold current	I²C-bus mode				
		AC load bit is set	460	-	-	mA
		AC load bit is not set	-	-	230	mA
Amplifier						
P_o	output power	R_L = 4 Ω; V_P = 14.4 V; THD = 0.5 %	18	20	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 10 %	23	25	-	W
		R_L = 4 Ω; V_P = 14.4 V; maximum power; V_i = 2 V (RMS) square wave	37	40	-	W
		R_L = 4 Ω; V_P = 15.2 V; maximum power; V_i = 2 V (RMS) square wave	41	45	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 0.5 %	29	32	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 10 %	37	41	-	W
		R_L = 2 Ω; V_P = 14.4 V; maximum power; V_i = 2 V (RMS) square wave	58	64	-	W
THD	total harmonic distortion	P_o = 1 W to 12 W; f = 1 kHz; R_L = 4 Ω	-	0.01	0.1	%
		P_o = 1 W to 12 W; f = 10 kHz	-	0.09	0.3	%
		P_o = 1 W to 12 W; f = 20 kHz	-	0.14	0.4	%
		line driver mode; V_o = 1 V (RMS) and 5 V (RMS); f = 20 Hz to 20 kHz	-	0.02	0.05	%
α_{cs}	channel separation	f = 1 kHz; R_S = 1 kΩ	65	80	-	dB
		f = 10 kHz; R_S = 1 kΩ	60	65	-	dB
PSRR	power supply rejection ratio	f = 100 Hz to 10 kHz; R_S = 1 kΩ	55	70	-	dB
CMRR	common mode rejection ratio	normal mode; V_{cm} = 0.3 V (p-p); f = 1 kHz to 3 kHz; R_S = 1 kΩ	45	65	-	dB
$V_{cm(max)(rms)}$	maximum common mode voltage (RMS value)	f = 1 kHz	-	-	0.6	V

Table 17. Characteristics *...continued*

Refer to test circuit (see Figure 29) at V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; R_S = 0 Ω; normal mode; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_{amb} = −40 °C to +105 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{n(o)}$	noise output voltage	filter 20 Hz to 22 kHz; R_S = 1 kΩ					
		mute mode		-	19	26	μV
		line driver mode		-	22	29	μV
		normal mode; T_{amb} = 25 °C to 105 °C		-	45	65	μV
		normal mode; T_{amb} = −20 °C to 25 °C		-	45	110	μV
G_v	voltage gain	differential in; differential out					
		normal mode		25.5	26	26.5	dB
		line driver mode		15.5	16	16.5	dB
R_i	input resistance	symmetrical input; C_i = 470 nF; see Figure 29	[5]	44	60	100	kΩ
α_{mute}	mute attenuation	V_o / $V_{o(mute)}$; V_i = 50 mV		80	92	-	dB
$V_{o(mute)(RMS)}$	RMS mute output voltage	V_i = 1 V (RMS); filter 20 Hz to 22 kHz		-	25	-	μV
B_p	power bandwidth	−1 dB		-	20 to 20000	-	Hz

[1] Operation above 16 V with a 2 Ω reactive load can trigger the amplifier protection. The amplifier switches off and will restart after 16 ms resulting in an 'audio hole'.

[2] V_{STB} depends on the current into the STB pin: minimum = (1429 × I_{STB}) + 5.4 V, maximum = (3143 × I_{STB}) + 5.6 V.

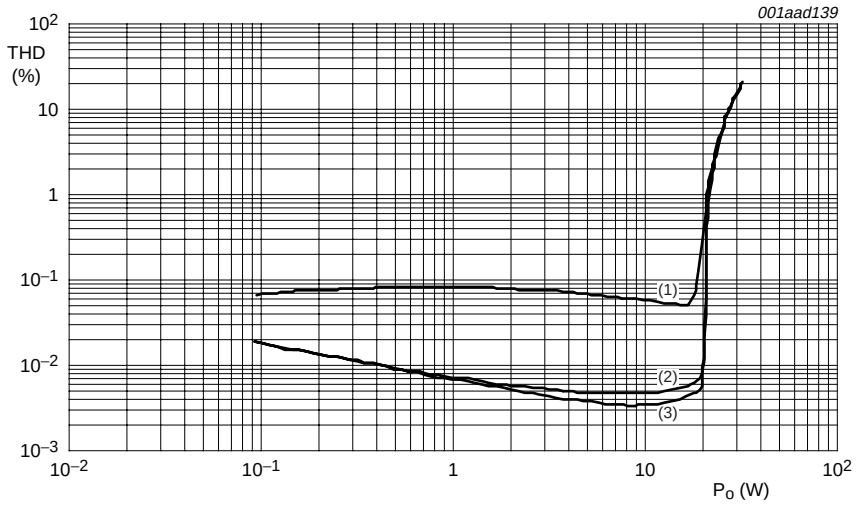
[3] The times are specified without a leakage current. For a leakage current of 10 μA on the SVR pin, the delta time is specified. If the capacitor value on the SVR pin changes with ±30 %, the specified time will also change with ±30 %. The specified time includes an ESR of the capacitor on the SVR pin of up to 15 Ω.

[4] Standard I²C-bus spec: maximum LOW level = 0.3 × V_{DD}, minimum HIGH-level = 0.7 × V_{DD}. To comply with 5 V and 3.3 V logic the maximum LOW level is defined with V_{DD} = 5 V and the minimum HIGH-level with V_{DD} = 3.3 V.

[5] R_i is the total differential input resistance. f_{-3dB} cut-off frequency is defined as

$$\frac{1}{2\pi \times R_i \times C_i/2} = \frac{1}{2\pi \times 44\ k\Omega \times 235\ nF \times 0.8} = 19\ Hz$$ assuming worst-case low input resistance and 20 % spread in C_i.

12. Performance diagrams



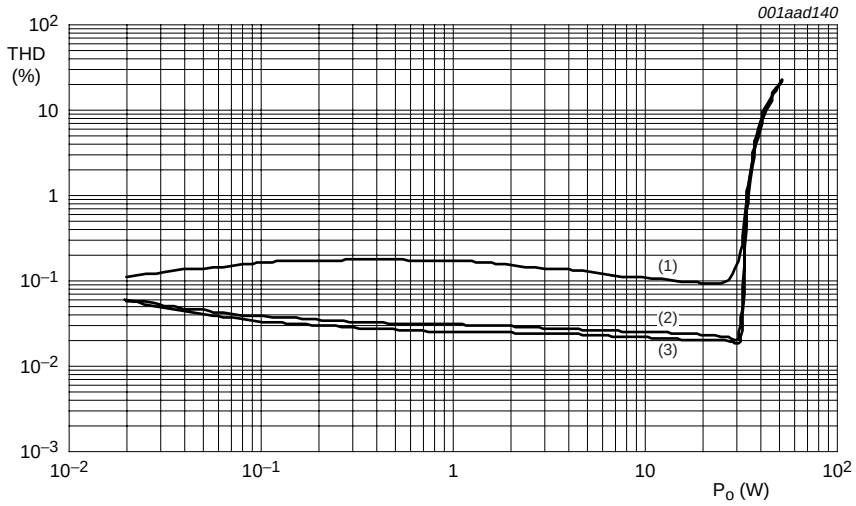
V_P = 14.4 V.

(1) f = 10 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

Fig 17. Total harmonic distortion as a function of output power; 4 Ω load



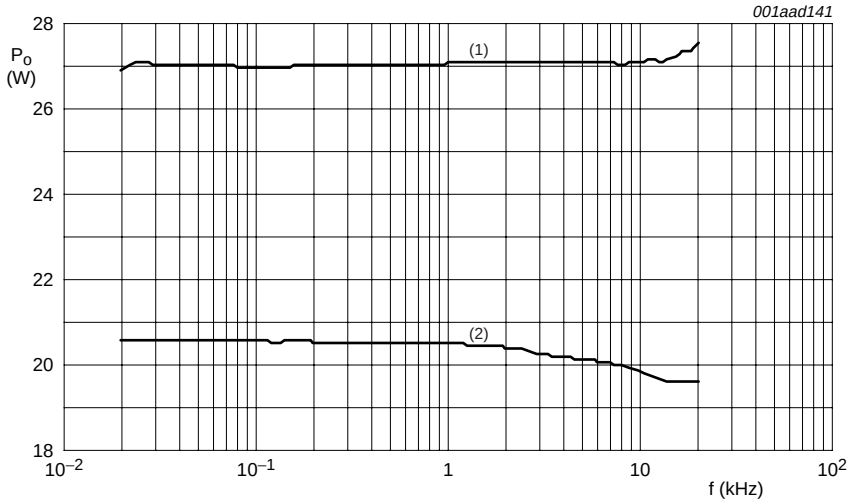
V_P = 14.4 V.

(1) f = 10 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

Fig 18. Total harmonic distortion as a function of output power; 2 Ω load

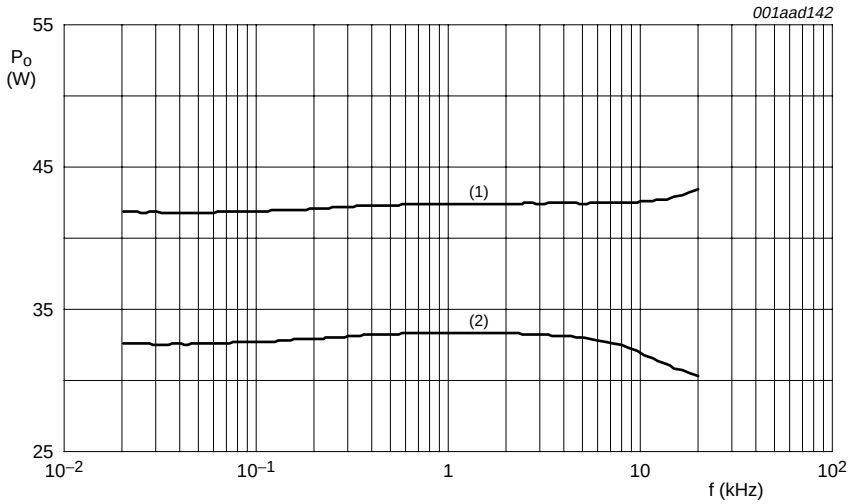


V_P = 14.4 V.

(1) THD = 10 %.

(2) THD = 0.5 %.

Fig 19. Output power as a function of frequency; 4 Ω load

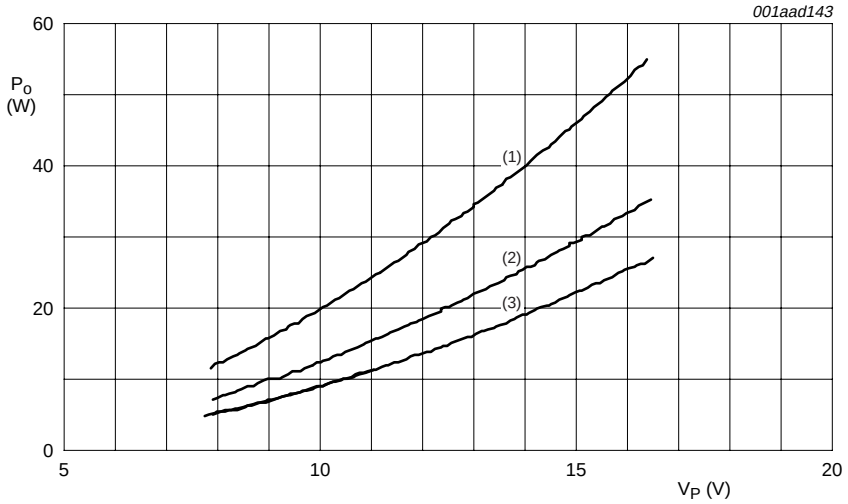


V_P = 14.4 V.

(1) THD = 10 %.

(2) THD = 0.5 %.

Fig 20. Output power as a function of frequency; 2 Ω load



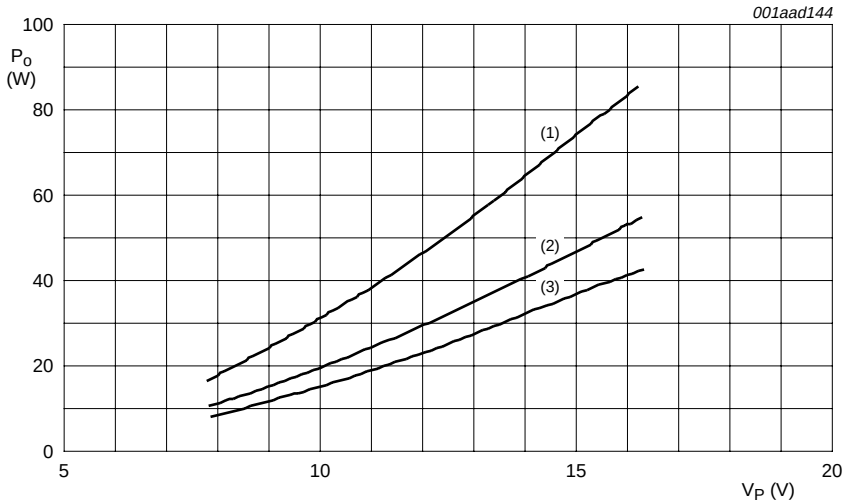
f = 1 kHz.

(1) $P_{o(max)}$.

(2) THD = 10 %.

(3) THD = 0.5 %.

Fig 21. Output power as a function of supply voltage; 4 Ω load



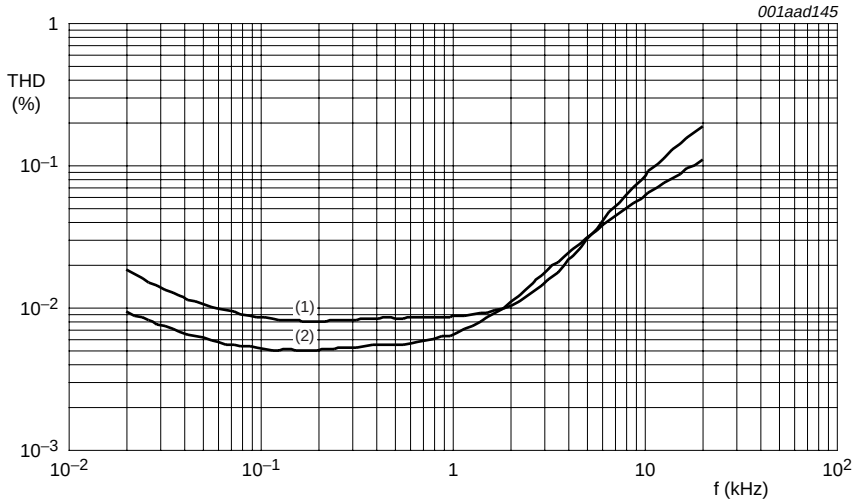
f = 1 kHz.

(1) $P_{o(max)}$.

(2) THD = 10 %.

(3) THD = 0.5 %.

Fig 22. Output power as a function of supply voltage; 2 Ω load

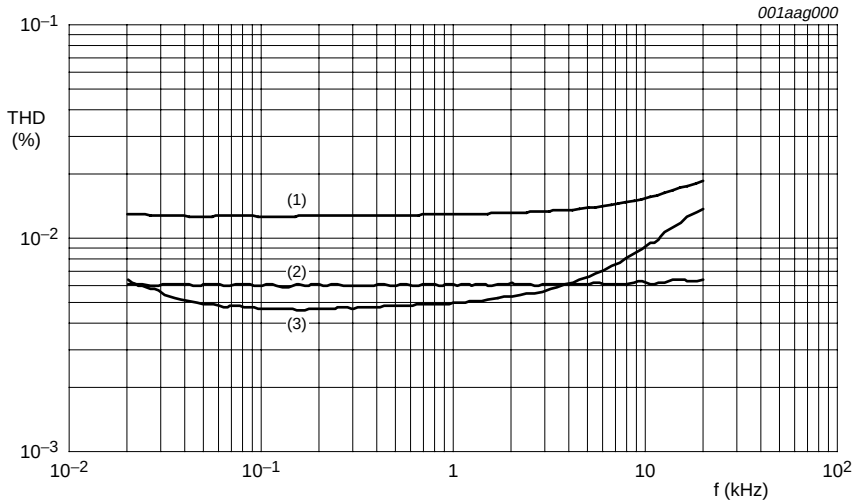


V_P = 14.4 V; R_L = 4 Ω.

(1) P_o = 1 W.

(2) P_o = 10 W.

Fig 23. Total harmonic distortion as a function of frequency; normal mode



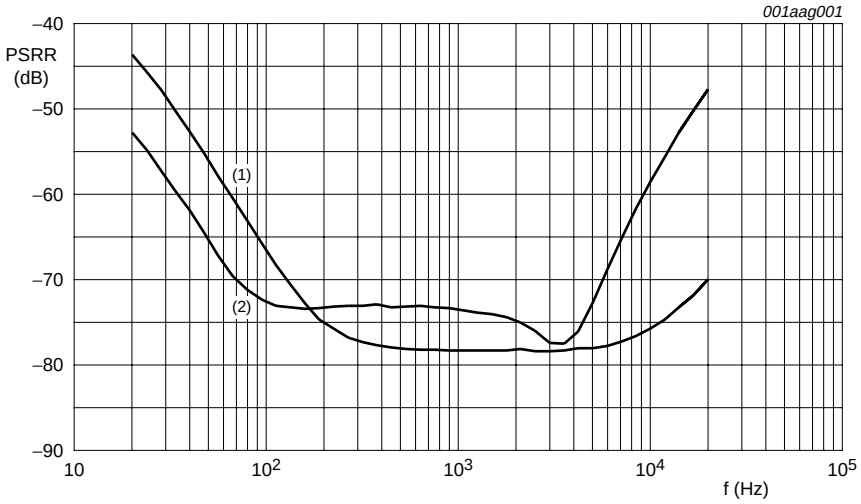
V_P = 14.4 V; R_L = 600 Ω.

(1) V_o = 5 V; front channel.

(2) V_o = 1 V.

(3) V_o = 5 V; rear channel.

Fig 24. Total harmonic distortion as a function of frequency; line driver mode

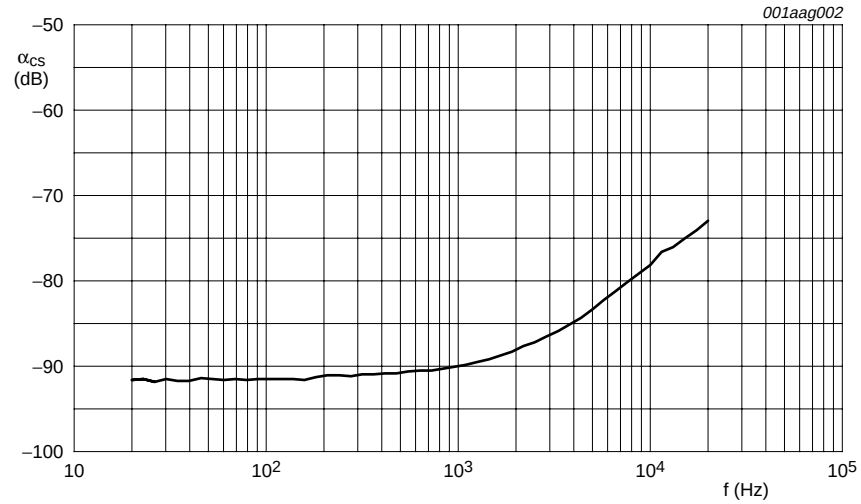


V_P = 14.4 V; R_L = 4 Ω; V_{ripple} = 2 V (p-p).

(1) front channel.

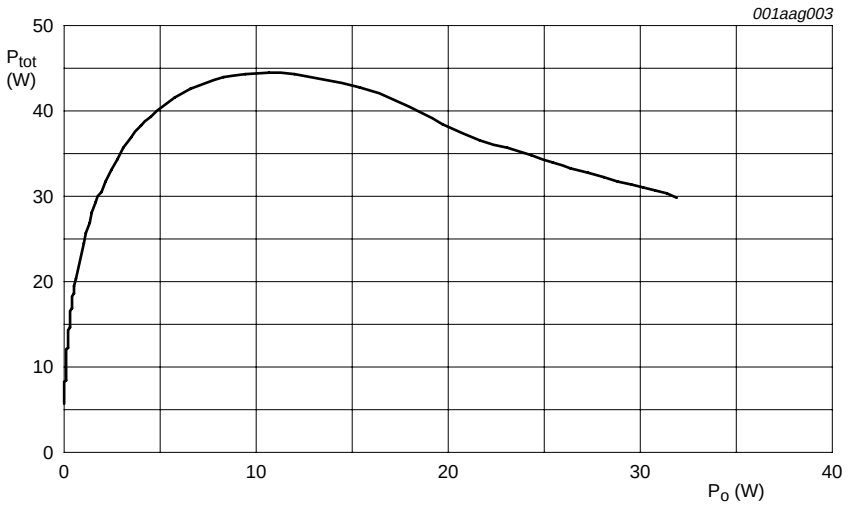
(2) rear channel.

Fig 25. Powers supply ripple rejection ratio as a function of frequency



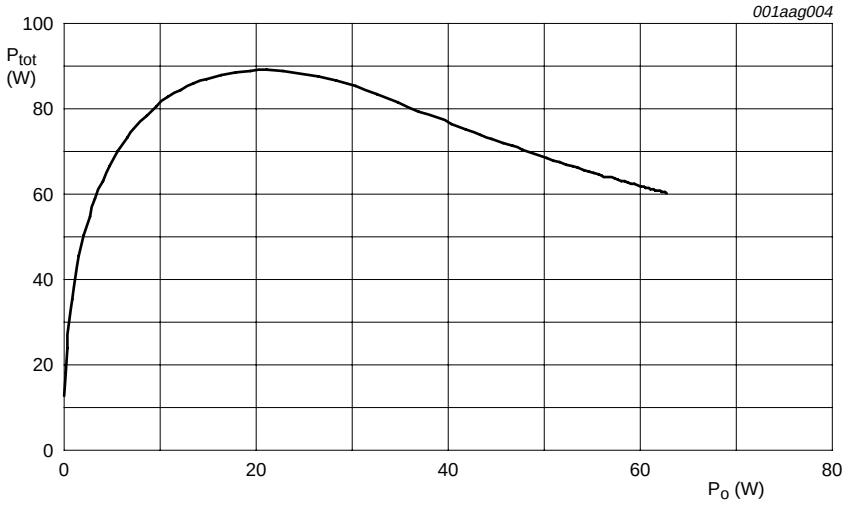
V_P = 14.4 V; R_L = 4 Ω; P_o = 4 W.

Fig 26. Channel separation as a function of frequency



V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz.

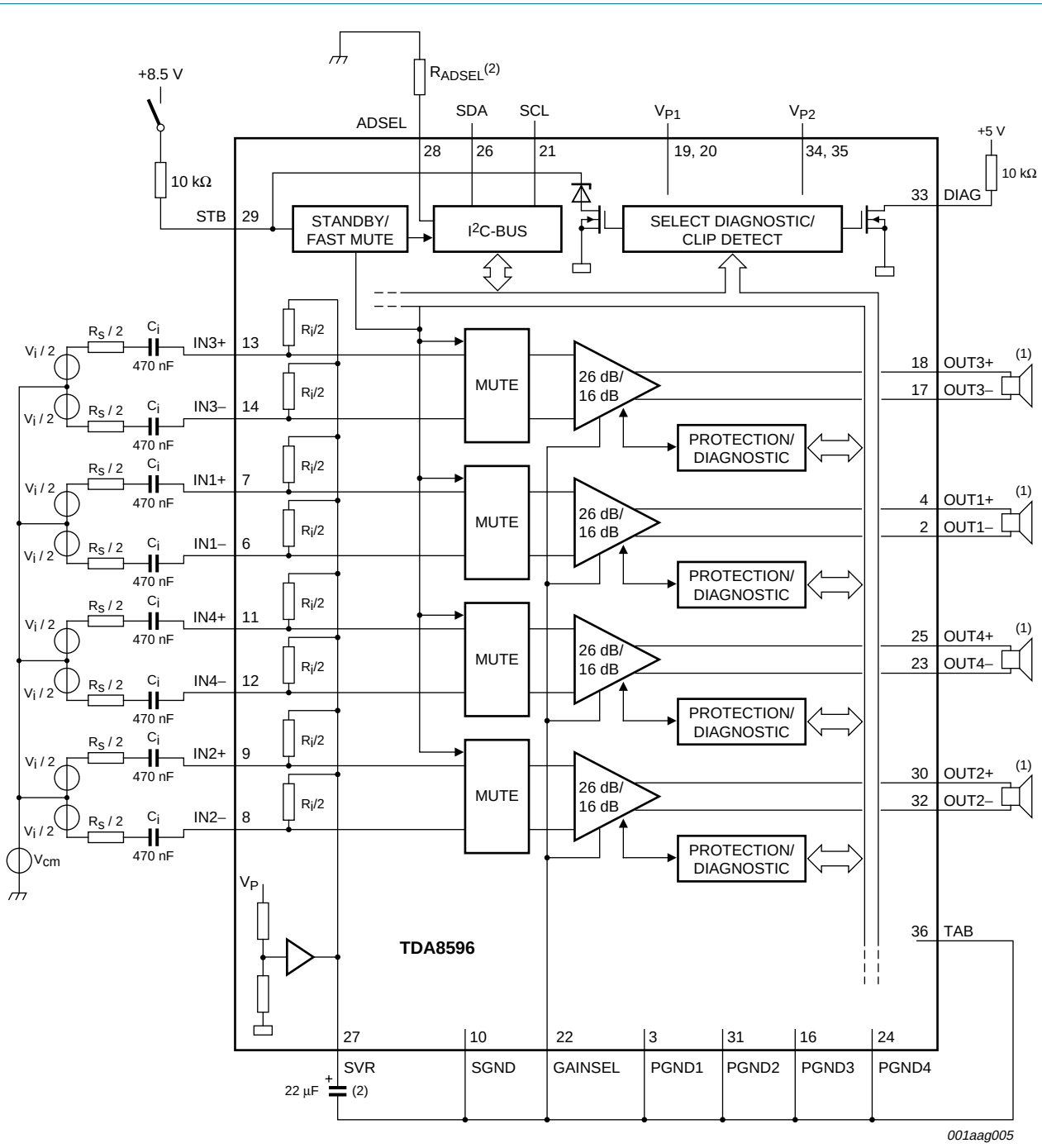
Fig 27. Power dissipation as a function of output power; 4 Ω load



V_P = 14.4 V; R_L = 2 Ω; f = 1 kHz.

Fig 28. Power dissipation as a function of output power; 2 Ω load

13. Application information



(1) A capacitor of 10 nF may be added between every amplifier output and ground for EMC reasons.

(2) The SVR capacitor and R_{ADSEL} resistor should first be connected to SGND before connecting to PGND.

Fig 29. Test and application information

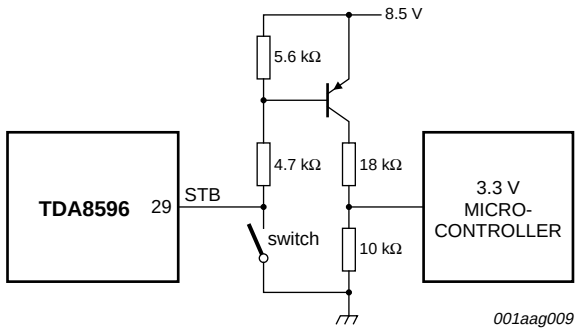


Fig 30. Circuit for combined STB and clip detection function on pin STB

13.1 PCB schematic and layout

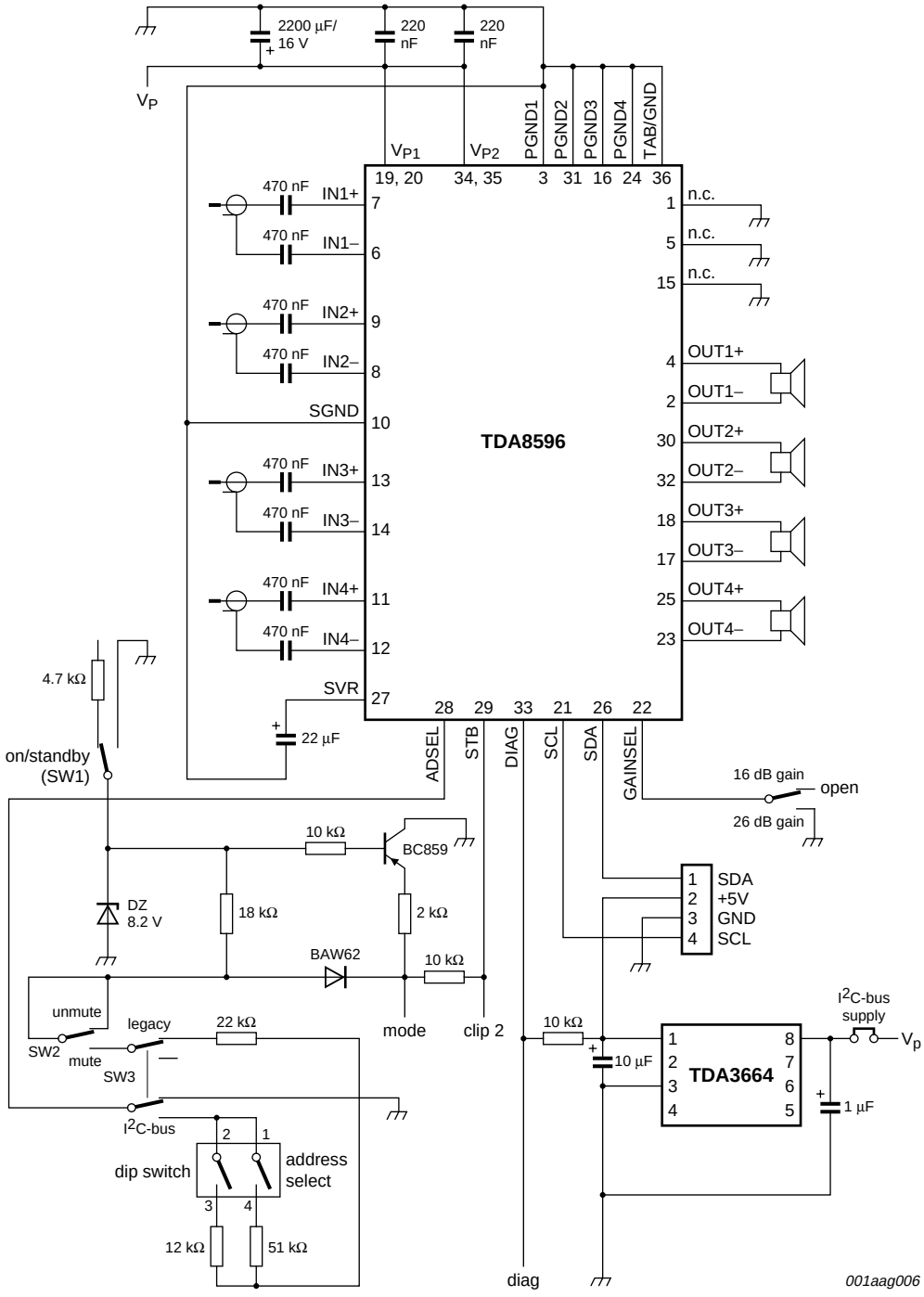
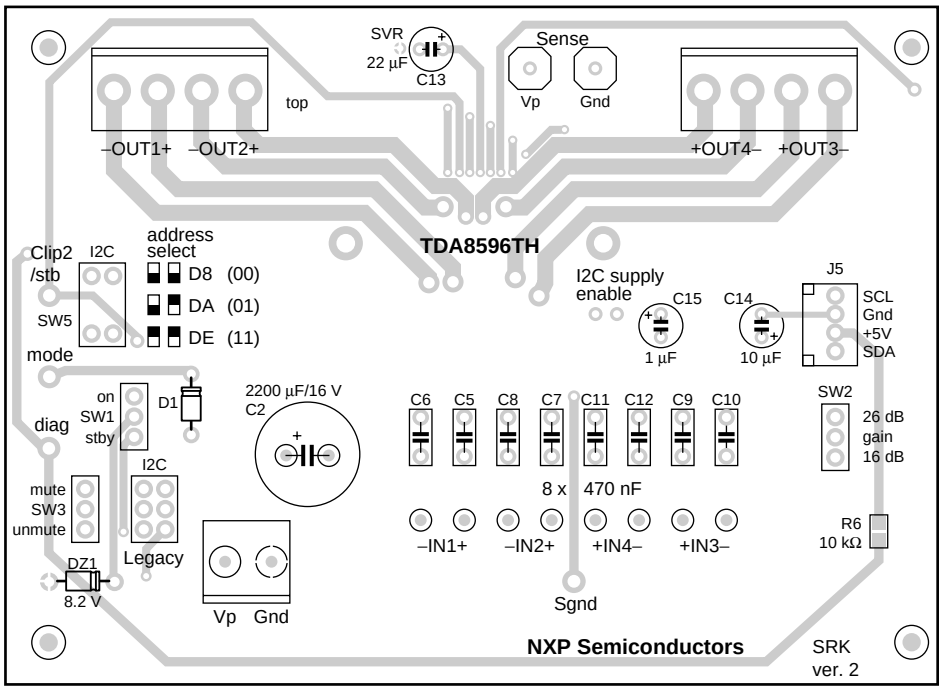
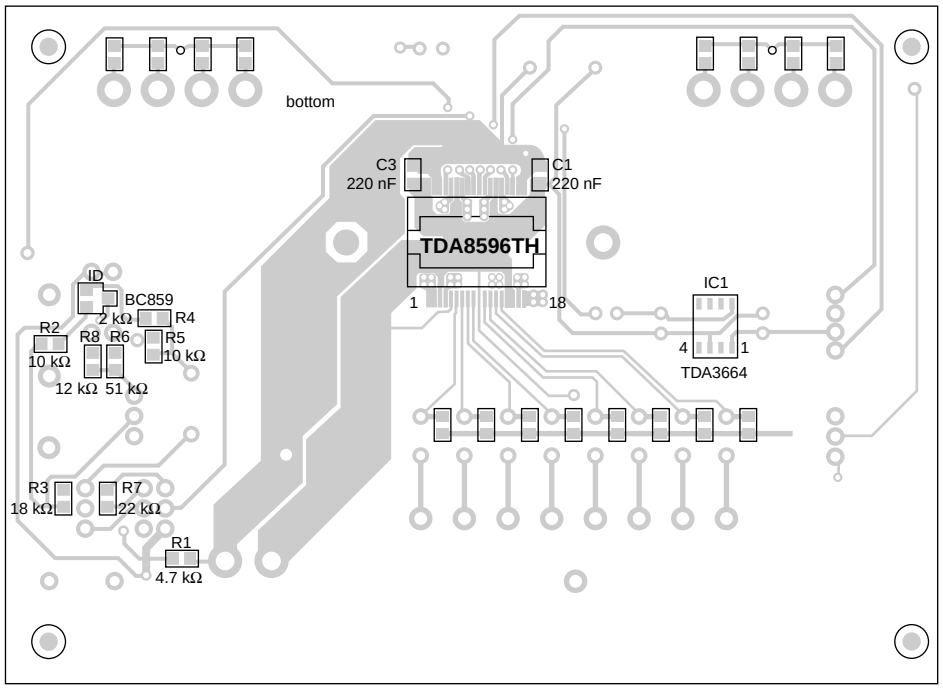


Fig 31. Evaluation board; schematic



001aag007

Fig 32. Evaluation board layout; top view



001aag008

Fig 33. Evaluation board layout; bottom view

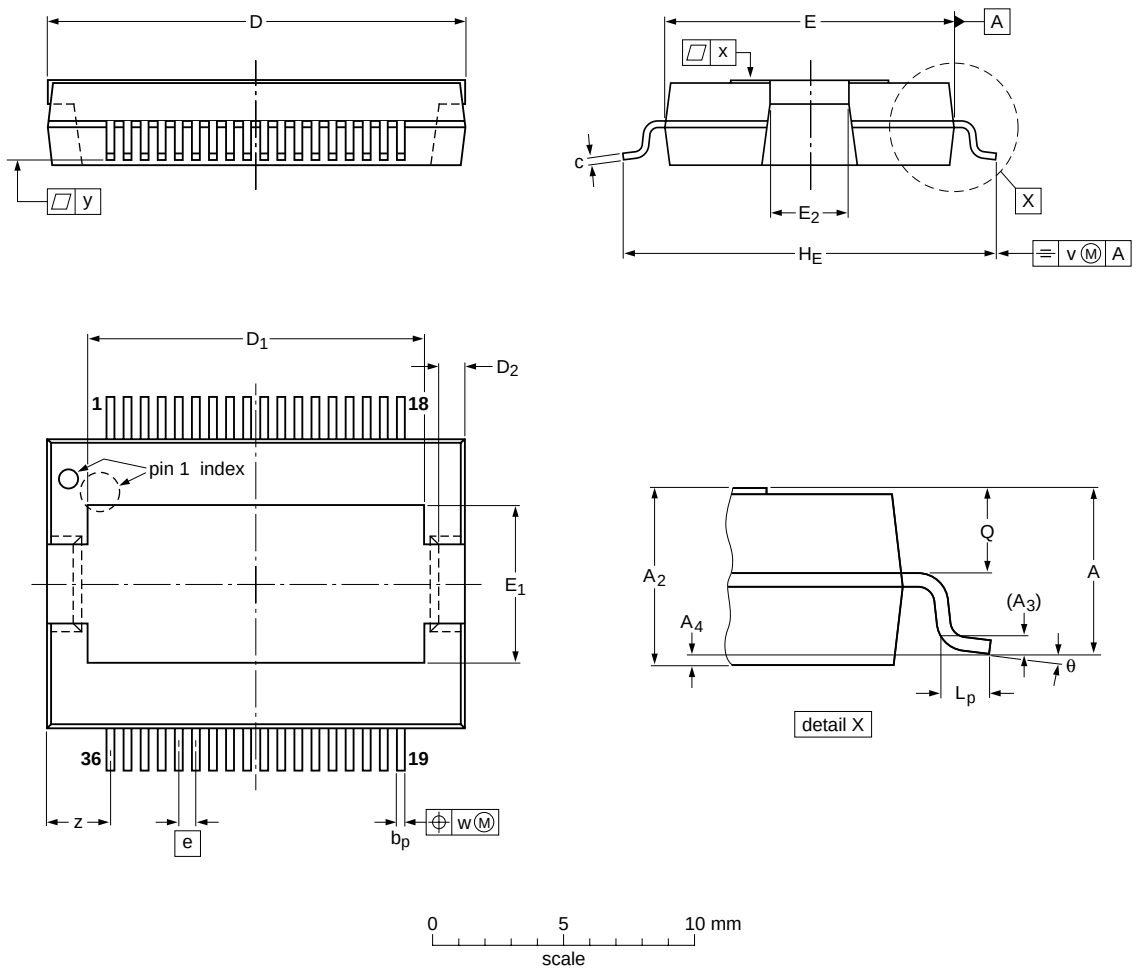
14. Test information

14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15. Package outline

HSOP36: plastic, heatsink small outline package; 36 leads; low stand-off height **SOT851-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4[1]	b_p	c	D[2]	D_1	D_2	E[2]	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 −0.04	0.38 0.25	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	0.65	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.12	0.03	0.07	2.55 2.20	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT851-2						04-05-04

Fig 34. Package outline SOT851-2 (HSOP36)

16. Abbreviations

Table 18. Abbreviations

Acronym	Description
BCDMOS	Bipolar CMOS/DMOS
CMOS	Complementary Metal-Oxide Semiconductor
DMOS	Double-diffused Metal-Oxide Semiconductor
DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
NMOS	Negative-channel Metal-Oxide Semiconductor
NMOST	Negative-channel Metal-Oxide Semiconductor Transistor
PMOS	Positive-channel Metal-Oxide Semiconductor
PMOST	Positive-channel Metal-Oxide Semiconductor Transistor
SOAR	Safe Operating ARea

17. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8596_2	20071108	Product data sheet	-	TDA8596_1
Modifications:	• Figure 30: Value of base-emitter resistor changed from 10 kΩ to 5.6 kΩ • Section 14: Quality information reference updated			
TDA8596_1	20070705	Preliminary data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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