Standard Products

# UT82CRH51A USART

Preliminary Data Sheet

July, 1999

## FEATURES

- Synchronous and asynchronous operation
- Synchronous 5-8 bit characters; internal or external character synchronization; automatic synchronization insertion
- Asynchronous 5-8 bit characters; Clock Rate - 1, 16, or 64 Times Baud Rate; break character generation; 1, 1.5, or 2 stop bits; false start bit detection; automatic break detect and handling
- Synchronous baud rate - 1 to 64K baud
- Asynchronous baud rate - DC to 19.2K baud
- Full-Duplex, double-buffered transmitter and receiver
- Error detection - parity, overrun and framing errors
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300K rads(Si)
  - SEL LET threshold: greater than 120MeV-cm$^2$/mg
  - Neutron Fluence: 3.0E14n/cm$^2$
- QML Q and V compliant part
- Packaging options:
  - 36-lead Flatpack
  - 68-lead Flatpack
- 5.0 volt operation
- Standard Microcircuit Drawing pending
- Available as core IP for ASIC applications

## INTRODUCTION

The UT82CRH51A is an enhanced version of the industry standard, Universal Synchronous/Asynchronous Receiver Transmitter (USART), designed to provide data communications between subsytems. The UT82CRH51A USART is built using UTMC's Commercial RadHard$^{TM}$ epitaxial CMOS technology and is ideal for space applications. In a communication environment an interface device converts parallel format system data into serial format for transmission, and converts incoming serial format data into parallel system data for reception. The UT82CRH51A is used as a peripheral device and is programmed by a host CPU to operate using virtually any serial data transmission technique. The USART accepts data characters from the CPU in a parallel format and then converts the data into a continuous serial data stream for transmission. Simultaneously, the UT82CRH51A receives serial data streams and converts the data into a parallel data character for the host CPU. The USART signals the CPU whenever it accepts a new character for transmission or whenever it has received a character for the CPU. The CPU reads the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET/BRKDET, TxEMPTY.

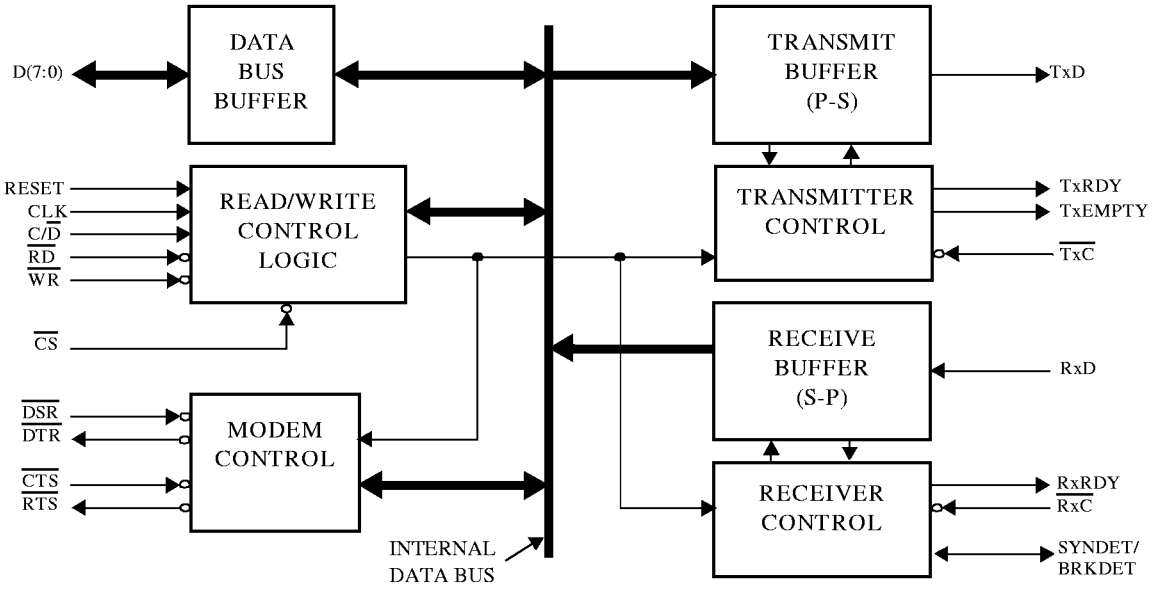


Figure 1. UT82CRH51A USART Block Diagram