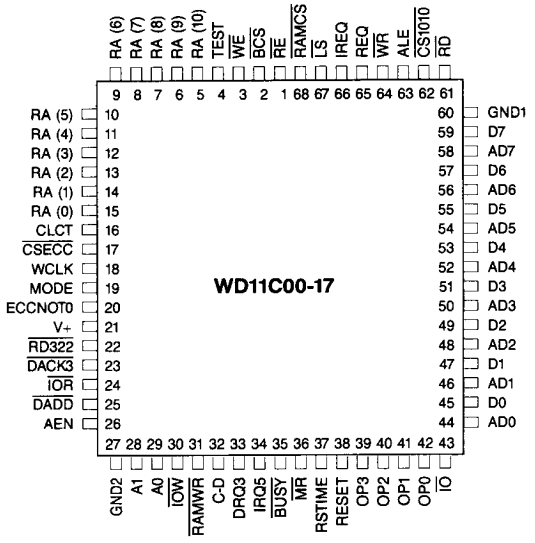
WESTERN DIGITAL
CORPORATION

WD11C00-17 PC/XT HOST INTERFACE LOGIC DEVICE

FEATURES

- 8-BIT HOST INTERFACE
- 3 MICRON CMOS TECHNOLOGY
- COMBINES RANDOM LOGIC AND SPECIALIZED CIRCUITS
- FAST SWITCHING SPEEDS
- LOW POWER DISSIPATION
- STATIC PROTECTION ON ALL I/Os
- PROPAGATION DELAYS OF 1.4 NANOSECONDS
- 68 PIN SURFACE MOUNTABLE PACKAGE
- SINGLE +5 VOLT POWER SUPPLY
- HIGH CURRENT BUS DRIVERS
- INTERFACE LOGIC CONTROL FOR PC BUS



PIN DESIGNATION

DESCRIPTION

The WD11C00-17 PC/XT Host Interface Logic Device combines the necessary random logic and specialized circuitry to interface the Western Digital chip set to the IBM PC/XT interface for Winchester Disk control. The chip contains integrated: Status Ports, Read/Write Ports, Sector Buffer Control, ECC Generation and Detection Logic, Reset Timing Logic, and Host Interface Logic. These features greatly simplify hardware requirements for the Design Engineer when using the WD chip set consisting of the: WD1015, WD1010A-05, and WD10C20-A. With appropriate decode logic, the WD11C00-17 appears to the Host as four contiguous I/O locations XX0-XX3. The 32-bit ECC Generation and Detection circuitry allows for realtime ECC check byte generation and error checking; ECC correction is via the WD1015. The WD11C00-17 also contains all the handshaking logic required for polled I/O and DMA transfers with the Host.

HOST INTERFACE

The WD11C00-17 PC/XT Host Interface Logic Device interfaces directly to the Host Data Bus via bi-directional high current bus drivers on the DO-D7 pins and high current drivers on the DRQ3 and DRQ5 pins.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature . . . . . 0°C (32°F) to 55°C (131°F)

Voltage on any pin with respect to Ground (Vss) . . . . . -0.5 to 7.0V

Power Dissipation 1W

Storage Temperature Plastic . . . . . -55°C (-67°F) to + 125°C (257°F)

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the AC/DC Electrical Characteristics.

AC/DC ELECTRICAL CHARACTERISTICS

T_A = 0 to 70°C; V_{CC} = 5.0V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
V_{IL}	TTL Low Level Input Voltage			0.8	V	Pins: 1, 2, 3, 4, 16, 17, 18, 19, 25, 32, 39, 40, 41, 42, 43, 44, 46, 48, 50, 52, 54, 56, 58, 61, 63, 64, 66, 67
V_{IH}	TTL High Level Input Voltage	2.4			V	Pins: Same as V_{IL}
V_{TL}	Schmitt Threshold Voltage Low	0.9			V	Pins: 23, 24, 26, 28, 29, 30, 37, 38, 45, 47, 49, 51, 53, 55, 57, 59
V_{TH}	Schmitt Treshold (High)			2.4	V	Pins: Same as V_{TL}
V_{HY}	Hysteresis	0.35			V	Pins: Same as V_{TL}
I_{OL}	Low Level Output Current Single Buffer	5.0			mA	V_{DL} = 0.4V Pins: 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 20, 22, 31, 35, 62, 65, 68
	TriState, Single Buffer	5.0			mA	Pins: 44, 46, 48, 50, 52, 54, 56, 58
	Tri-State, Double Buffer	10.0			mA	Pins: 1, 3, 33, 34, 45, 47, 49, 51, 53, 55
	Open Drain N-Channel	5.0			mA	Pins: 36, 37
I_{OH}	High Level Output Current Single Buffer	−5.0			mA	V_{OH} = 2.4V Pins: Same as I_{OL}
	Tri-State, Single Buffer	−5.0			mA	Pins: Same as I_{OL}
	Tri-State, Double Buffer	−10.0			mA	Pins: Same as I_{OL}
I_{DD}	Supply Current			15	mA	Pins: Same as I_{OL}
I_I	Input Leakage	−10.0		10	uA	Vin = 0 or 5.5V
I_Z	Tri-State Leakage	−10.0		10	uA	Vo = 0 or 5.5V

PIN DESCRIPTIONS

Pin descriptions are listed in Table 1.

TABLE 1. PIN DESCRIPTIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	Read Enable	$\overline{RE}$	Input when $\overline{BCS}$ is low. Read strobe is bidirectional, for Sector Buffer Address. Output when $\overline{BCS}$ is high, follows $\overline{RD}$ Pin 61.
2	Buffer Chip Select	$\overline{BCS}$	Controls direction of bidirectional $\overline{RE}$, $\overline{WE}$ lines. Enables $\overline{RAMCS}$ for WD1010 access.
3	Write Enable	$\overline{WE}$	Input when $\overline{BCS}$ is low. Write strobe is bidirectional for Sector Buffer Address. Output when $\overline{BCS}$ is high, follows $\overline{WR}$ Pin 64.
4	Test	TEST	Input active high, used for test only, controls state of internal RA10 (end of data) during ECC test. TEST = LOW DATA TEST = HIGH END OF DATA
5-15	RAM Address	$\overline{RA10}$ RAO	Outputs active high, address Sector Buffer RAM and WD1010.
16	Clear Count	CLCT	Input active high clears lower RAM address counter outputs RA - RA7.
17	Chip Select ECC	$\overline{CSECC}$	Input active low enables the ECC function.
18	Write Clock	WCLK	Input 5 MHz clock for the ECC function.
19	Mode	MODE	Input when high selects normal mode of the ECC function (i.e., check bytes are generated after end of data). When low selects long mode and inhibits preset function of ECC logic (i.e., check bytes are not generated after end of data and logic passes check bytes transparently from Host to disk).
20	ECC Not Zero	ECC NOT 0	Output active high indicates to WD1015 that an error has been detected while comparing check bytes at end of data stream with check bytes generated internally.

TABLE 1. PIN DESCRIPTIONS (continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
21	+5 VDC	VCC	Input supply voltage.
22	Read Port 322	$\overline{RD322}$	Output active low when Host reads status Port 322.
23	DMA Acknowledge 3	$\overline{DACK3}$	Input active low acknowledges DMA request 3 (DRQ3).
24	I/O Read	IOR	Input active low enables data onto D0-D7 outputs when Host wants to read data or status.
25	Device Address Code	$\overline{DADD}$	Input active low when address 320 thru 323 is present on the Host Address Bus.
26	Address Enable	AEN	Input active high indicates that DMA Controller (Host) has control over the address, control, and data buses. Used to enable Host to disk I/O functions.
27	Ground	GND	Ground.
28	Address Bit 1	A1	Input active when Host asserts A1 to high state. Used to enable Host to disk I/O functions.
29	Address Bit 0	A0	Input active high when Host asserts A0 to high state. Used to enable Host to disk I/O functions.
30	I/O Write	$\overline{IOW}$	Input active low strobes data from the Data Bus into internal devices or into the Sector Buffer RAM when Host performs a write function.
31	RAM Write	$\overline{RAMWR}$	Output active low when either Host, WD1010 or WD1015 wants to write to Sector Buffer RAM.
32	Control/Data	$\overline{C}/D$	Input when low indicates that Controller expects either a command or status block transfer. When high, indicates that Controller expects a data block transfer. Used to enable a data block transfer. Used to enable disk I/O control section.
33	DMA Request 3	DRQ3	Output active high requests DMA service from the Host. Remains high until $\overline{DACK\ 3}$ goes low. Asserted when the Controller is ready to accept data or data is ready to be read.
34	Interrupt Request 5	IRQ5	Output active high signals to Host that service is required. Remains high until Host interrupt service routine resets it. Activated when the Controller has completed disk operation.
35	Busy	$\overline{BUSY}$	Output active low indicates Host has selected controller and is about to perform an I/O operation.
36	Master Reset	$\overline{MR}$	Bidirectional input active low when external Power UP Reset detects dropping VCO level. Clears all internal registers. Output active low when Host either performs a soft reset, or handshake reset from the bus is detected via the RESET Pin 38.
37	Reset Time	RSTIME	Input threshold adjust for the duration of the $\overline{MR}$ Pin 36 active low time during soft Reset.
38	Reset	RESET	Input active high when Host performs a bus reset. Clears all internal registers and active $\overline{MR}$ Pin 36 to active low.
39-42	Option 0, 1, 2, 3	OP0, 1, 2, 3	Inputs normally high via internal pull up resisters. Can be activated low by applying GND to the input. Disk configuration readable on Data Bus by Host via status read to Port 322. OP0 - D0, OP1 - D1, OP2 - D2, OP3 - D3.
43	Input/Output	$I/\overline{O}$	Input controls direction on Internal Data Bus Buffer from Host's point of view. High = input to Host. The ADX Bus is driven onto the DX Bus. Low = output from Host. DX Bus is received and driven to the ADX Bus.

TABLE 1. PIN DESCRIPTIONS (continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
44, 46 48, 50 52, 54 56, 58	Address/Data Bus	AD0-AD7	Bi-directional Bus carries address information to Internal RAM Address Counter and control de-muliplexer. Carries data to and from the internal ECC function and the external Sector Buffer RAM.
45	$\overline{\text{Data Bus 0}}$	$\overline{\text{D0}}$	Bi-directional Bus interfaces Controller to Host Data Bus. ($\overline{\text{D0}}$ through $\overline{\text{D7}}$).
47	$\overline{\text{Data Bus 1}}$	$\overline{\text{D1}}$	
49	$\overline{\text{Data Bus 2}}$	$\overline{\text{D2}}$	
51	$\overline{\text{Data Bus 3}}$	$\overline{\text{D3}}$	
53	$\overline{\text{Data Bus 4}}$	$\overline{\text{D4}}$	
55	$\overline{\text{Data Bus 5}}$	$\overline{\text{D5}}$	
57	$\overline{\text{Data Bus 6}}$	$\overline{\text{D6}}$	
59	$\overline{\text{Data Bus 7}}$	$\overline{\text{D7}}$	
60	Ground	GND	Ground.
61	$\overline{\text{Read}}$	$\overline{\text{RD}}$	Input active low when WD1015 performs a read operation.
62	$\overline{\text{Chip Select 1010}}$	$\overline{\text{CS1010}}$	Output active low when WD1015 performs a read or write operation to the WD1010.
63	Address Latch Enable	ALE	Input active high when WD1015 asserts ALE. Used internally to select and latch the control demultiplexer.
64	$\overline{\text{Write}}$	$\overline{\text{WR}}$	Input active low when WD1015 performs a write operation.
65	Request	REQ	Output active high indicates to the Host that Controller is ready to accept data from or transfer data to the Host. Handshake signal for transfers between Host and Controller. The state of this output is read on $\overline{\text{D0}}$ by the Host via a status read to Port 321.
66	Interrupt Request	IREQ	Input when asserted enables REQ. When low, it indicates to the Host that the operation is complete.
67	Long/Short	L/S	Input signal is high during a Host Controller transfer. The Controller is in the long mode (Data Transfer) when high. When this signal is low during Host Controller transfer, the Controller is in the short mode (Command Transfer).
68	$\overline{\text{RAM Chip Select}}$	$\overline{\text{RAMCS}}$	Output active low enables the external Sector Buffer RAM for read/write operations by the Host, WD1015 or WD1010.

FUNCTIONAL DESCRIPTION

The WD11C00-17 PC/XT Host Interface Logic Device combines random logic and specialized circuits into one device. The internal architecture of the WD11C00-17 is shown in block diagram format and illustrated in Figure 1.

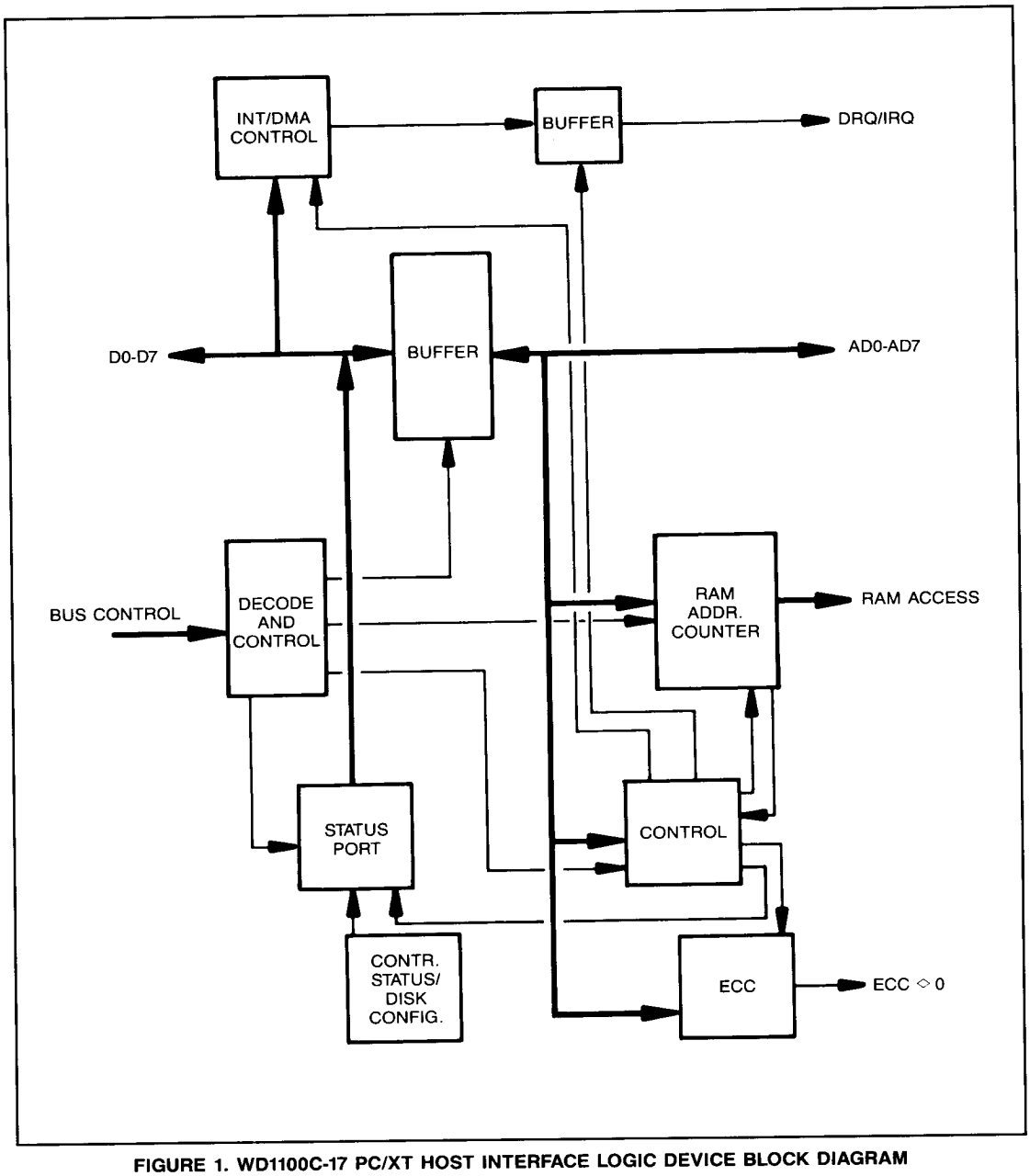


FIGURE 1. WD1100C-17 PC/XT HOST INTERFACE LOGIC DEVICE BLOCK DIAGRAM

STATUS PORTS

All port address decoding is done internally in the WD11C00-17. This is done via the A0 and A1, and $\overline{DADD}$ inputs. The board's hardware status register and INT/DRQ latches are contained within the WD11C00-17. The board's hardware status is available to the Host via a read to Port 321. This is a read only function. The bits are defined as follows:

Bit 7 – Unused

Bit 6 – Unused

Bit 5 – Interrupt Request (IRQ)

Bit 4 – Data Request (DRQ)

Bit 3 – Busy (BUSY)

Bit 2 – Command/$\overline{Data}$ (C/$\overline{D}$

Bit 1 – Input/$\overline{Output}$ (I/$\overline{O}$)

Bit 0 – Request (REQ)

The four lower order bits (OP0-OP3) of the drive configuration information are readable on the Data Bus by the Host via read operation to Port 322. This is a read function only. OP0-OP3 are input signals to the WD11C00-17, and are normally high due to internal pull-up resistors. OP0-OP3 are written directly to the Data Bus via D0-D3 outputs from the WD11C00-17.

RD322 output is generated by the WD11C00-17 so that external 74LS244 can be used to read the four high order bits (OP4-OP7) of the drive configuration information. These bits are pulled up by external 4.7K pullup resistors.

Port 323 contains two bits which enable or disable the interrupt and DMA request lines to the Host. This is a write function only. The bits are defined as follows:

Bits 7-2 – Unused

Bit 1 – Interrupt Request Enable

Bit 0 – DMA Request Enable

READ/WRITE PORTS

All port address decoding is done internally in the WD11C00-17. This is done via the A0 and A1, and $\overline{DADD}$ inputs. A complete port summary is defined in Table 2.

All reads and writes to Port 320 result in data being transferred from the Sector Buffer and the Sector Buffer Counter being incremented.

Write to Port 321 results in a software reset. This has the same effect as a hardware reset.

Write to Port 322 results in a board selection. This must be done prior to each command.

The primary/secondary port selection is made by jumper W4 and when the $\overline{DADD}$ input is modified, not the WD11C00-17.

SECTOR BUFFER CONTROL

The WD11C00-17 contains all the necessary Sector Buffer address counters and generates Sector Buffer chip select and Sector Buffer read/write signals.

The RA0 through RA9 outputs are used to control the Sector Buffer. A 2K by 8 RAM is used but only 1K of it is necessary so only the lower 1K is used. This 1K is divided into four 256 byte pages.

The RA8-RA10 outputs are resetable by the WD1015. This allows the WD1010 to access the WD1010 tasks files.

The RA10 output is used to de-assert DRQ3, informing the Host that the Sector Buffer is either empty or full, and signals the end of the data field or the start of the ECC field to the ECC logic in the WD11C00-17.

The lower two pages of the Sector Buffer are used to store the 512 bytes of sector data. The lower page is also used to store command information prior to passing it along to the WD1015 and, to store ECC bytes.

The $\overline{RAMCS}$ and $\overline{RAMWR}$ outputs are used to select the Sector Buffer and Read/Write to the RAM.

The WD1015 outputs the $\overline{CLCT}$ signal to the WD11C00-17. This results in the Address Counter outputs RA0-RA7 to be cleared.

DISK, HOST, AND WD1015 I/O CONTROL

The WD11C00-17 is used in conjunction with the WD1015 and the Sector Buffer in controlling the WD1010 and performing Host transfers.

Commands are transferred by the Host into the first 256 byte page within the Sector Buffer. The WD1015 then reads these commands and loads the WD1010's task file registers with the appropriate information.

The WD1010's task file registers are selected via the RA8-RA10 outputs together with the $\overline{CS1010}$ output.

The WD11C00-17 inputs $\overline{BCS}$, $\overline{RE}$, and $\overline{WE}$, are asserted by the WD1010 when it wants to read the Sector Buffer. A read or write by the WD1015 to the WD1010's task file registers results in the $\overline{RE}$ or $\overline{WE}$ outputs to be asserted. The $\overline{RE}$ and $\overline{WE}$ line are bi-directional and are inputs when $\overline{BCS}$ is low.

The WD11C00-17 inputs $\overline{RD}$ and $\overline{WR}$ are used by the WD1015 when it wants to read or write either the Sector Buffer or the WD1010.

TABLE 2. READ/WRITE PORTS

ADDRESS	READ FUNCTION	WRITE FUNCTION
320/324	Read Data, Board to Host	Write Data, Host to Board
321/325	Read Board Hardware Status	Board Software Reset
322/326	Read Drive Configuration Information	Board Select
323/327	Not Used	Set/Reset DMA, IRQ Masks

The Host Data Bus (D0-D7) interfaces directly to the WD11C00-17 and is driven via bi-directional high current bus drives the chip.

The bus signals DRQ3 and IRQ5 are driven by internal high current drivers.

The A0, A1, $\overline{DACK3}$, $\overline{IOR}$, $\overline{IOW}$ and $\overline{RESET}$ inputs to the WD11C00-17 all feature Schmitt trigger inputs to ensure noise immunity.

The WD1015 outputs the $\overline{CLCT}$ signal to the WD11C00-17. This results in the Address Counter outputs RA0-RA7 to be cleared.

The $\overline{DADD}$ input to the WD11C00-17 is generated by the external address decode logic. The WD11C00-17 will decode which of the four ports is being selected, but the external circuitry must decode the proper port address range of 320 through 323.

The AEN input to the WD11C00-17 is asserted when the DMA controller has control over the bus. AEN's assertion de-gates the Host Processor and other devices from the I/O channel.

The $\overline{BUSY}$, $\overline{CD}$, and I/O inputs to the WD11C00-17 are all generated by the WD1015 and passed to the WD11C00-17 so that they may read in the board's hardware status register.

ECC GENERATION AND DETECTION

The WD11C00-17 generates and appends the four byte ECC to the data stream. Proper placement of the ECC requires determination of the end of the data stream. Assertion of RA10 by the WD11C00-17 Address Counter indicates RAM overflow and the end of the data stream. After writing the four ECC bytes to the disk, the WD11C00-17 ECC circuitry supplies all zero bytes to the AD0 through AD7 Bus as long as the ECC function is selected.

During a read operation, the ECC circuitry recomputes the ECC. Comparison of the previously written ECC and computed ECC occurs at the end of the data stream. The ECC circuitry records the results of the comparison. Any additional writes to the Sector Buffer are ignored. If the results of the comparison is non-zero, then the WD11C00-17 asserts a ECC NOT 0 signal. Assertion of ECC NOT 0 enables the disk controller to attempt error correction.

During Writelong and Readlong commands, the ECC generations and checking is disabled. A Writelong command caused the WD11C00-17 to accept any four bytes from the Host, and stores them internally. These bytes are written to the disk unaltered.

A Readlong command causes the WD11C00-17 to accept the four bytes written on the disk. These bytes are passed to the Host unaltered. This allows the Host to induce errors anywhere in the data stream and check for predictable results.

The ECC circuitry requires a 5 MHz input clock which is derived from the WD10C20's Write Clock output.

The polynomial $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$ is the same as that used in other Western Digital devices.

RESET TIMING

When asserted, RST places the board in its initial power-up condition, setting the internal parameters and initializing on-board circuitry properly. The WD11C00-17 has an internal one-shot that handles the reset pulse width. The input RSTIME controls the duration of the active low reset pulse that originates from the $\overline{MR}$ output.

The WD1002S-WX2 Winchester Disk Controller uses a 1.3 Mohm resistor to nominally set the reset pulse width to 1.4 ms.

The RESET input is hard wired to the bus interface reset input. A reset on this pin clears all internal registers and forces the $\overline{MR}$ output low.

The $\overline{MR}$ pin is bi-directional and acts as an input when the external VCC detect circuit forces the board into a reset condition. When this occurs, the internal registers are reset.

Figure 2 illustrates the WD11C00-17 PC/XT Host Interface Logic Device incorporated into the WD1002S-WX2 Winchester Disk Controller Board's architecture.

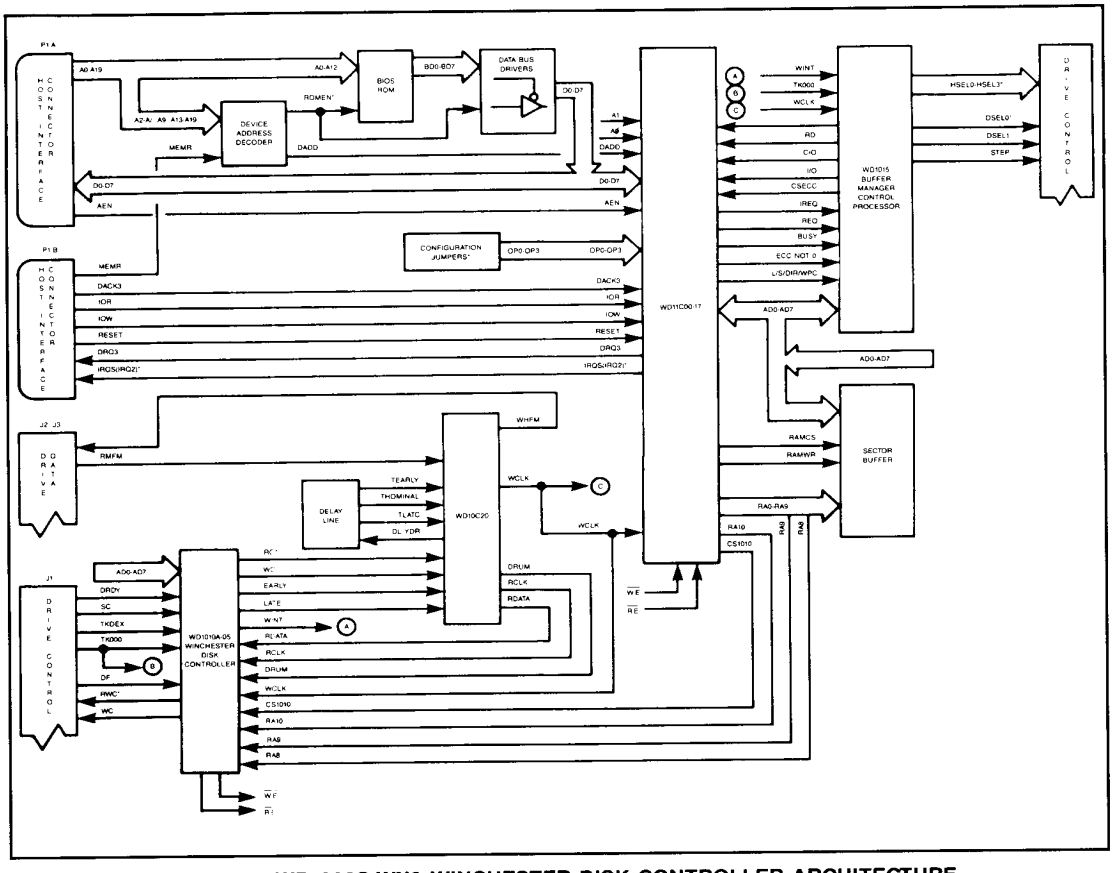


FIGURE 2. WD1002S-WX2 WINCHESTER DISK CONTROLLER ARCHITECTURE

WESTERN DIGITAL CORPORATION
2445 McCABE WAY
IRVINE, CALIFORNIA 92714
(714) 863-0102, TWX 910-595-1139

Printed in U.S.A