

FEATURES

The ATA attenuator is a versatile two-resistor tapped chip, whose R_A/R_B ratio can be specified within the values of 1:1 to 20:1.

These chips are manufactured using state-of-the-art thin-film techniques, are 100% electrically tested and visually inspected to MIL-STD-883.

- Variable attenuation ratios
- Oxidized silicon substrate for good power dissipation
- Chip size 58 mil square
- Quick delivery
- Resistor material tantalum nitride, self-passivating

TCR VALUES AND TOLERANCES

Resistance ($R_A + R_B$)	25 k Ω
Tolerances ($R_A + R_B$)	$\pm 5\%$
Greatest ratio (R_A/R_B)	20:1
TCR	± 50 ppm/ $^{\circ}\text{C}$

ATTENUATION TABLE

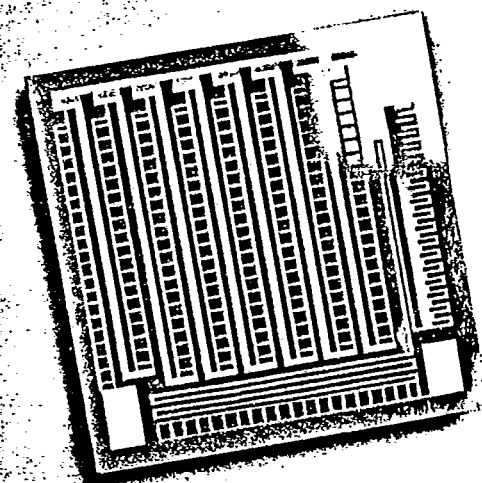
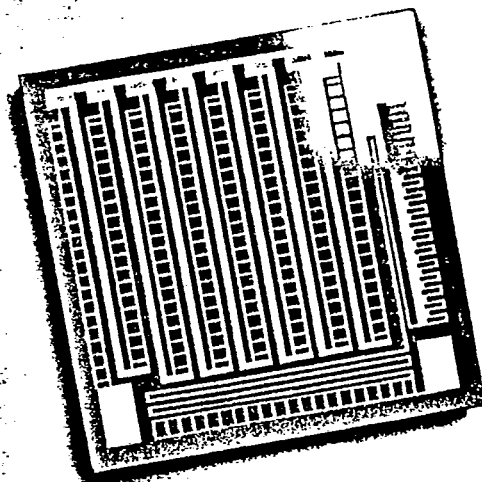
PART # ATA -	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	RATIO ACCURACY	TEMPERATURE TRACKING
RATIO R_A/R_B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	$\pm 0.05\%$	± 5 ppm/ $^{\circ}\text{C}$ MAX ± 2 ppm/ $^{\circ}\text{C}$ TYPICAL
ATTENUATOR FACTOR $R_B/R_A + R_B$	$\frac{1}{2}$	$\frac{1}{3}$	$\frac{1}{4}$	$\frac{1}{5}$	$\frac{1}{6}$	$\frac{1}{7}$	$\frac{1}{8}$	$\frac{1}{9}$	$\frac{1}{10}$	$\frac{1}{11}$	$\frac{1}{12}$	$\frac{1}{13}$	$\frac{1}{14}$	$\frac{1}{15}$	$\frac{1}{16}$	$\frac{1}{17}$	$\frac{1}{18}$	$\frac{1}{19}$	$\frac{1}{20}$	$\frac{1}{21}$	$\pm 0.025\%$ to $\pm 0.045\%$	± 2.5 ppm/ $^{\circ}\text{C}$ to ± 4.8 ppm/ $^{\circ}\text{C}$ MAX ± 1 ppm/ $^{\circ}\text{C}$ to ± 2 ppm/ $^{\circ}\text{C}$ TYPICAL
ATTENUATOR FACTOR $R_A/R_A + R_B$	$\frac{1}{2}$	$\frac{2}{3}$	$\frac{3}{4}$	$\frac{4}{5}$	$\frac{5}{6}$	$\frac{6}{7}$	$\frac{7}{8}$	$\frac{8}{9}$	$\frac{9}{10}$	$\frac{10}{11}$	$\frac{11}{12}$	$\frac{12}{13}$	$\frac{13}{14}$	$\frac{14}{15}$	$\frac{15}{16}$	$\frac{16}{17}$	$\frac{17}{18}$	$\frac{18}{19}$	$\frac{19}{20}$	$\frac{20}{21}$	$\pm 0.025\%$ to $\pm 0.0025\%$	± 2.5 ppm/ $^{\circ}\text{C}$ to ± 0.25 ppm/ $^{\circ}\text{C}$ MAX ± 1 ppm/ $^{\circ}\text{C}$ to ± 0.15 ppm/ $^{\circ}\text{C}$ TYP.

*Depends on ratio

ELECTRICAL CHARACTERISTICS

TCR tracking between R_A and R_B	± 5 ppm/ $^{\circ}\text{C}$
Noise, MIL-STD-202, Method 308	-35 dB max.
Moisture resistance, MIL-STD-202, Method 106	$\pm 0.5\%$ max. $\Delta R/R$
Stability, 1000 hr., +125 $^{\circ}\text{C}$, 25 mw	$\pm 0.5\%$ max. $\Delta R/R$
Operating temperature range	-55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$
Thermal shock, MIL-STD-202, Method 107, Test Condition F	$\pm 0.1\%$ max. $\Delta R/R$
High temperature exposure, +150 $^{\circ}\text{C}$, 100 hr.	$\pm 0.2\%$ max. $\Delta R/R$
Dielectric voltage breakdown	400 V
Insulation resistance	$10^{12} \Omega$ min.
Operating voltage	100 V max.
DC power rating at +70 $^{\circ}\text{C}$ (derated to zero at +175 $^{\circ}\text{C}$)	50 mw per resistor
5 x rated power short-time overload, +25 $^{\circ}\text{C}$, 5 seconds	$\pm 0.1\%$ max. $\Delta R/R$

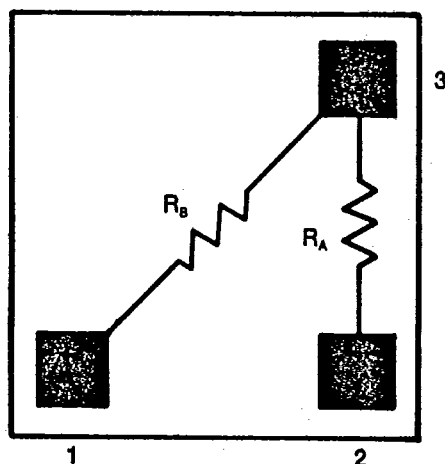
ATA THIN-FILM ATTENUATION RATIO RESISTORS



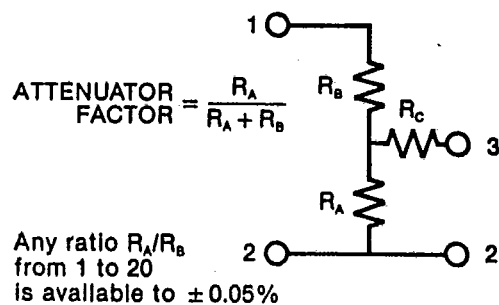
Semi  Films
Division

P.O. Box 188
West Hurley, NY 12491
Tel. (914) 338-7714
Fax (914) 338-6329

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STANDARD
CONFIGURATION

Shaded Areas
Represent
Bonding Pads.



R_C is a parasitic resistor approximately 5Ω in value, which does not affect the performance of the device when it is used into a high impedance load.

MECHANICAL DATA

Chip size	58 x 58 ± 3 mil (1.47 x 1.47 ± 0.076 mm)
Chip thickness	8 ± 3 mil (0.203 ± 0.08 mm)
Chip substrate material	Oxidized silicon, 10 k Ω min. SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pads	5 x 5 mil (0.127 x 0.127 mm)
No. of pads	3
Pad material	10 k Ω min. aluminum
Backing	None, lapped semiconductor silicon

OPTION: Gold back for eutectic die attach

APPLICATIONS

These attenuation resistor-ratio chips are designed for the tight ratio tolerances generally required in amplifier feedback circuits. The great range of ratio choices makes them specially suitable for this application.

PART NUMBER DESIGNATION

Example: 100% visualled, 25k Ω $\pm 5\%$, ± 100 ppm TCR, Ratio=19.00

